

# MEMORIES







September 1990

---

## GENERAL INFORMATION

---

### MHS BACKGROUND

MATRA MHS (formerly MATRA HARRIS S/C) was formed in 1979. Its charter was to develop a leading CMOS design and manufacturing operation in Europe. In the early 80's, MHS reached its objectives and became a pioneer with several novative products, especially CMOS static memories.

Then, several other agreements contributed to MHS development.

In 1981, MHS signed an agreement with Intel Corp. covering the manufacture of NMOS circuits in Nantes, France and the establishment of a joint design facility for telecom chips and video controllers (82716).

Resultingly, MHS manufactured Intel's 8086, 8088, 8051 and 8052, as well as Harris' 80C86/88.

MHS was also entitled to desing CMOS versions of the 8051 MCU family. The 80C51 and its derivates have become one of MHS major successes, while fabrication of 16 bit MPU and NMOS devices was stopped, to concentrate on CMOS MCU.

In a deal with Cypress in 1985, MHS received licensing rights to manufacture Cypress' fast 16 K and 64 K

CMOS SRAMs and utilize Cypress fast 1.2 and 0.8 micron processes for MHS designs as well. The deal has been recently extended with new products such as 128 K cahe RAMs and 256 K.

With France's national Telecom research labs (CNET), MHS developed an advanced sub-micron process, named Super-CMOS, to combine speed and low power consumption. This process has been in production at MHS since 1988.

Most new devices are designed to run on it, including products designed by the CNET, which are industrialized and marketed by Matra MHS. The collaboration with CNET has been extended to 0.7 micron lithography and below.

In 1988, MHS and NEC of Japan signed a second-source agreement covering mutual manufacture and design rights of NEC's 78312 16 bit microcontroller family.

The same year, MHS and Aspen - a subsidiary of Cypress - entered an agreement to fund development of BiCMOS technology to manufacture very high speed TTL or ECL SRAM and ASIC. These products are being introduced in 1990.

### MHS INDUSTRIAL CAPABILITY

MHS plant in Nantes (western France) includes a 2.000 m2, class 10 wafer fab which is capable to produce over 100.000 125 mm wafers per year.

Around 18 million integrated circuits are shipped every year by MHS.

The Nantes operation also has its own assembly and test lines, as well as R & D and Quality departments.

This factory has been fully qualified by all major military and space agencies according to their highest standards ; its quality has also been praised by some of the world's most demanding I.C. users.

### MHS SALES & SUPPORT NETWORK

Since 1986, MHS has its own worldwide sales and distribution network, with direct subsidiaries in Paris, Munich, London, Milan, Stockholm, Santa Clara, and

Hong Kong. Each location provides a local technical center for application support and ASIC design.

---

## MHS PRODUCT OFFERING

MHS offering includes four main product lines, all in CMOS ; most circuits are available in commercial, industrial, and military temperature ranges.

MHS is also a leading European manufacturer of Hi-Rel

devices for military, aeronautics and space applications : its factory has been certified AQAP-1 and a variety of products have been listed by the corresponding agencies.

### MICROS

- **The 8051 family in CMOS**, with a complete palette of options :
  - ROM capacity from 4 K to 32 Kbytes : 80C51, 80C52, 83C154, 83C154D.
  - Low-voltage (2.7 V), fuse-protected "secret ROM", high-speed (30 MHz) versions.
  - Quick ROM service : three weeks for ROM code customization.
- Piggy Back versions.
- **SPARC** : a complete chip set is now available :
  - 90C601, 32 bit RISC processor
  - 90C602, Floating Point Unit
  - 90C604, Cache Controller and Memory Management Unit
  - 90C611, 32 bit RISC Controller.

### MEMORIES

- **Static RAM**
  - FAST : 16 K, 64 K, 72 K and 256 K.
    - 16 K (HM-65728A/767A/768A) down to 15 ns,
    - 64 K (HM-65764/787/790) down to 15 ns,
    - 64K BICMOS (HM-65864/887/890) down to 10 ns,
    - 72 K (HM-65779, 8 K x 9) down to 25 ns,
    - 256 K (HM-65756/797/798) down to 25 ns.
  - ULTRA FAST : ECL SRAM, 256 x 4 and 1 K x 4 in BICMOS, down to 3 ns.
  - Application, Specific Memories :
- Cache RAM 8 K x 16 for 386 interface, down to 25 ns, Cache Controller 385/395, for 386/486 interface, up to 33 MHz,
- Dual Port RAM 2 K x 16 and 2 K x 8, down to 25 ns, FIFO 512 x 9 and 1 K x 9, down to 25 ns.
- Very Low Power :
  - 16 K, 6 transistor cell HM-65162/262.
- Ultimate 64 K and 256 K SRAM :
  - 64 K (HM-65664/687/688), 35 ns/1  $\mu$ A,
  - 256 K (HM-65656/697/698), 35 ns/1  $\mu$ A.

### DATA COM PRODUCTS

- a family of combo devices (HC3054/57) compatible with a market standard
- specific chips for modem applications, the 29C42 error correction circuit for V42/LAP M Modems, the HC55421 X21 interface, etc.
- MHS is introducing a range of circuits dedicated to ISDN applications : rate adaptators (29C93), HDLC and ECMA102 multiplexed controllers, video codecs...

These products can be used in Terminal Equipments or at the Network Termination end.

They are targeted for the upcoming generation of equipment requiring powerful, flexible and low-cost components.

- Video circuits are also available :

Discrete Cosine Transformer 29C80, for image transmission, with data compression.

Still Picture Decoder 29C82, according to "ADCT" standard.

Digital to Analog Video Decoder 29C84, D2 MAC, satellite receivers, still transmission at 64 K bits on ISDN videophone or multi-media terminal.

### CMOS ASIC

- Five **gate-array** families, with gate-counts from 250 up to 55,000 gates, ultra-fast CMOS arrays, proprietary and standard software tools running on VAX, SUN, or turnkey systems such as DAISY, MENTOR, VALID, HP.
- Two families of **Composite arrays** mixing optimized blocks (RAM, ROM, & others) with regular arrays of gates.
- Specific **smart software** for system analysis and logical synthesis.
- Digital and/or analog **custom designs** capabilities using standard software from Silicon Compilers Systems Corp. : GDT and genesil.
- Field technical centers in most of its subsidiaries.



## MHS DIFFERENTIATION

After having successfully proved its ability to provide the electronic market with quality CMOS standard products as well as ASICs, MHS has decided to offer additional and newer solutions for system integration.

We named it : "THE TOOLBOX".

It combines our best strengthes :

- A unique sub-micron process : the Super/CMOS.
- A proven experience in making microcontrollers, SRAM, ASIC and Telecom chips which results in our mastering several of the most frequent functionalities needed in modern electronic systems.
- A design methodology based the availability of the above functions in a building block form, and a set of advanced design tools - including silicon compilation - which allows to mix them on a single I.C. as required.
- The total flexibility of these tools, which offers the possibility to develop most specific product in gate-array, composite array, or optimized silicon, according to our customer needs, expressed in terms of time-to-market, prototype cost, and production price.
- A team of very capable system and device architects, fully dedicated to analyze and discuss our customers' needs, in order to choose with them the best suited architecture and mean of integration to completely satisfy their specific requirements.

The above concept has been working so well that we have developped privileged relations with our customers. As a result, we are able to move with them through the frontier between standard and user specific I.C. We are diluting this frontier ; our customer's experience has fertilized our tool box, and MHS's constantly richer tool box allows us to propose more and smarter solutions every day.

With our customers, we became :

A CONSULTANT IN INTEGRATION  
and  
AN EXPERT IN INTEGRATION

### ALTERNATIVES FOR SYSTEM INTEGRATION

Each of the below criteria come from one or several different departments of our customers : marketing, design, manufacturing, and purchasing or finance. Program managers will evaluate the appropriate trade-offs, depending on the context of each program, including technical, market, and other specific factors.

This will help in choosing with MHS the best suitable solution and planning, taking into account possibilities offered by MHS to shift or evolve from one solution to another one at a further program stage.

| SAMPLE OF CRITERIA     | STANDARD CIRCUITS & PLD, GATE-ARRAYS | FULL CUSTOM CIRCUITS | COMPOSITE ARRAYS | OPTIMIZED* PARTITION |
|------------------------|--------------------------------------|----------------------|------------------|----------------------|
| Breadboarding          | ++                                   | -                    | -                | +                    |
| Fast redesign          | ++                                   | -                    | ++               | +                    |
| Level of integration   | -                                    | ++                   | +                | +                    |
| Complex systems        | -                                    | +                    | +/-              | ++                   |
| Flexibility            | ++                                   | -                    | +                | ++                   |
| Technical risks        | +                                    | -                    | +                | +                    |
| Test & emulation       | ++                                   | -                    | +                | ++                   |
| Development cost       | ++                                   | -                    | +                | +                    |
| First production cost  | -                                    | -/+                  | +                | +                    |
| Mature production cost | -                                    | ++                   | +                | +                    |
| Second source          | ++                                   | -                    | +                | +                    |
| Confidentiality        | -/+                                  | ++                   | +                | +                    |

(+ = satisfactory ; - = poor)

\* **Note** : the optimized partition is a multi-chip solution based on standard circuits and composite arrays, for which the balance of criteria is often more favorable than solutions using custom circuits.

---

# MHS SCMOS PROCESS

## 1. MHS COMMITMENT TO CMOS

For development and fabrication of the most advanced integrated circuits in both the ASIC and standard product fields MHS has made and stick to the choice of CMOS technology. A lot of developments and progress have been made from the initial 4  $\mu\text{m}$  CMOS process, back in 1980, to the most recent processes bearing on materials, device physics or lithography which allow now the new technology to provide speed and high integration density on top of the traditional virtues of CMOS : low power consumption, wide voltage and temperature operating range or high noise immunity.

These continuous efforts made by the company in a very focused way around CMOS led MHS to the introduction in 1988 of the Super CMOS (SCMOS) technology on which most of the new MHS integrated circuits are now built or developed.

One single process however cannot fulfill all product requirements, and for this purpose complementary developments have been performed to derivate from a generic technology process varieties more suited to particular needs as presented below.

## 2. THE SCMOS PROCESS

Co-developed with the France's National Telecom Research Laboratory (CNET) the SCMOS goal has been to offer a generic process as described here before with submicronic minimum features to provide a very high speed potential as well as maximum integration capability. Such advantages however should not be gained against reliability characteristics which are of prime importance in highly integrated system especially for avionics or space application. For all these reasons special options have been taken in building up the process as can be viewed on the cross section of the double metal version of SCMOS. Let's review the key points of that construction :

### THE SUBSTRATE

The latch-up phenomenon has always been a major concern of CMOS technology, that triggers parasitic thyristor which can generate very high current flows resulting in circuit non functionality or destruction. By using special electrical structure on circuits I/O's and adopting careful layout rules inside the chips, accuity of the problem has been greatly reduced on MHS products. However, shrinking down the dimensions requires new solutions. Building the devices in a shallow high resistive layer epitaxially grown on very low resistivity substrate has proven its efficiency in killing the latch-up phenomenon. By using such P+ epitaxial wafers in SCMOS, voltage drops, induced by current injection in the substrate, are greatly reduced, while chance of triggering the parasitic SCR is close to zero, resulting in potential latch-up free circuits.

### THE DEVICES

To guarantee high operation frequency of products, it is necessary to move toward submicronic transistor size in new processes. SCMOS emphasizes this trend as 0.8 micron drawn devices reach electrical channel length as low as 0.65 micron for the N channel transistor thus conferring high speed potential to the circuits.

Short channels - however - have several drawbacks that needed to be considered in SCMOS to guarantee reliable operation and keep high performance :

- To prevent punchthrough effects, such as voltage limitations and subthreshold currents degrading the circuit standby power consumption, in-depth study and optimization of transistor ion implant have been carried out.
- When going to short channel length, very high electrical fields are applied to electrons in the devices and the chance for those carriers to get enough energy to be injected in gate oxide becomes significant. This "hot electron" effect creates voltage and transconductance shifts that degrade device and circuit reliability. To counter this threat on SCMOS, both P and N channel transistors are built with LDD structures. This "Lightly Doped Drain" structure reduces the electrical fields in the devices drain vicinity thus lowering the probability of hot electron emission.

These two examples illustrate, among other actions, the particular care that was taken in designing the SCMOS devices to get the best performances without giving up any in reliability.

### THE GATE MATERIAL

Used to build the transistor gates and being the first interconnection layer, this level has to have as low resistivity as possible. The SCMOS technology achieves that goal by replacing the polysilicon material by a bi-layer of polysilicon which keeps the transistor threshold voltage characteristics, and Titanium Silicide which provides the low resistance. A tenfold improvement has been obtained through this solution, lowering typical value of this layer from 30 ohm/square down to 3 ohm/square. A great benefit results for all product performances and especially for memory, for which long word lines use to be realized with the gate level.

### THE DOUBLE METAL SYSTEM

More and more circuits now require an enhanced routing capability, either to achieve higher integration density (memories), or to allow automation in placement and routing tasks (ASIC). If multilayer interconnection is a necessity, several limitations however have to be overcome to implement it efficiently in very dense technology. Among the concerns of double metal systems let us mention the silicon metal interface, the metal step coverage, the risk of hillock formation generating shorts

between metal layers, contact filling, intermetal dielectric planarization, via-contact stacking constrain, and electromigration.

Here again, with SCMOS, an innovative solution has been chosen to address most of these problems : it stands in the utilization of Tungsten as the first metal material, followed by a planarized intermetal dielectric before deposition of the 2nd metal layer using aluminium material.

Among other properties, Tungsten can be deposited by chemical vapor deposition technique which leads to better topology coverage, and offers the possibility of contact filling by an autoplanarization mechanism. Advantage is taken of this characteristic in allowing the stacking of vias and contact to interconnect the 2 metal layers. Such a possibility autorizes tighter metal pitches thus saving area in repetitive structures and interconnections.

Other advantages come with tungsten utilization, including better reliability resulting from the very good electromigration endurance of this material.

Through these specific developments, adding to the basic works in new techniques around lithography (direct stepping on wafers) or material deposition and etching as well as manufacturing engineering works, MHS as been able to master this advanced CMOS process.

With its characteristics, of which an abstract is given in *table 1*, the SCMOS appears as a key technology for the next 5 years. Thanks to innovative options that were made, it also bears the basics for future enhance-

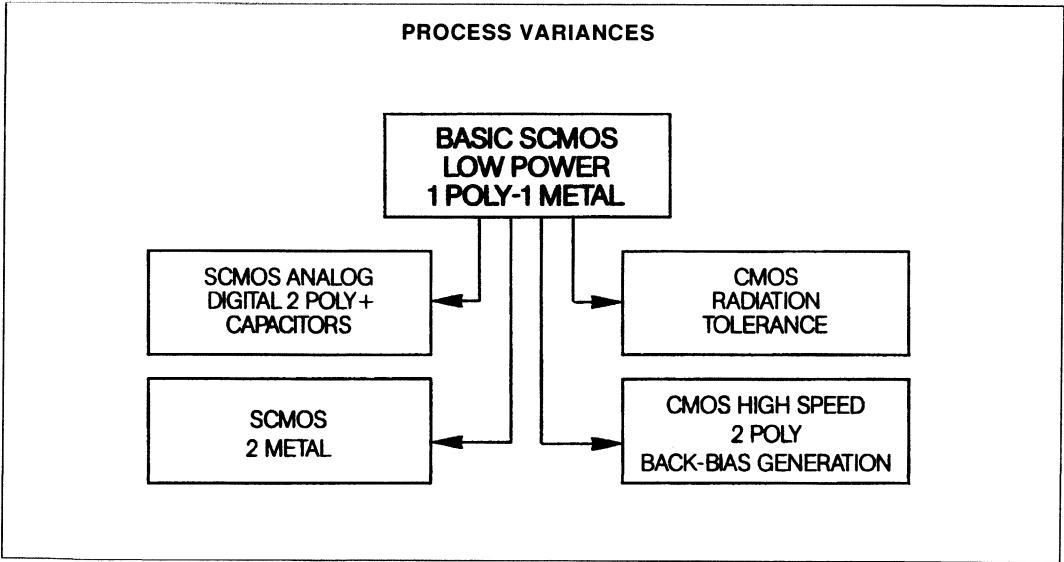
ments : it is already prepared for an analog version of the same process and for even smaller lithographies (0.7 and 0.5  $\mu\text{m}$ ).

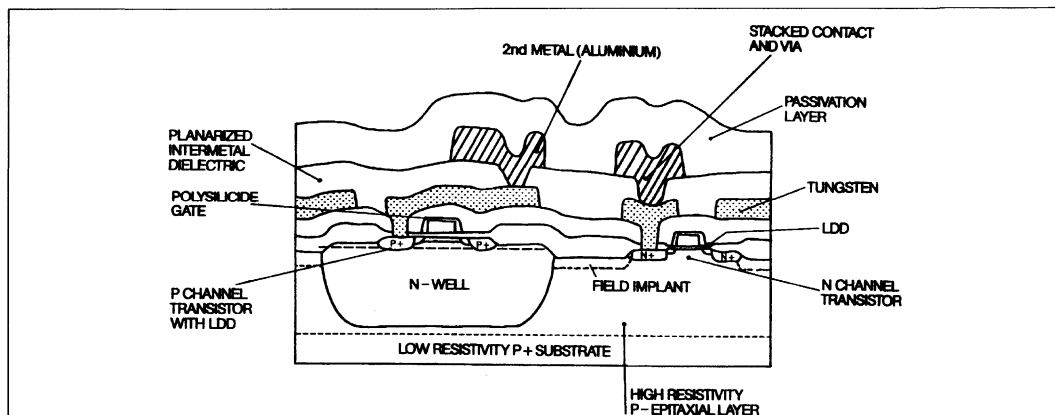
|                                                                                                                       |                                           |
|-----------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| Gate oxide thickness                                                                                                  | 200 Å                                     |
| Electrical channel length <ul style="list-style-type: none"><li>• NMOS transistor</li><li>• PMOS transistor</li></ul> | 0.65 $\mu\text{m}$<br>0.9 $\mu\text{m}$   |
| Minimum drawn features                                                                                                | 0.8 $\mu\text{m}$                         |
| Metal 1 pitch                                                                                                         | 2.9 $\mu\text{m}$                         |
| Metal 2 pitch                                                                                                         | 3.4 $\mu\text{m}$                         |
| Propagation delay                                                                                                     | 120 ps/gate                               |
| Integration density                                                                                                   | 25000 transistor/mm <sup>2</sup><br>(RAM) |

Table 1.

PRODUCT REQUIREMENTS

| PRODUCTS                         | NEEDS                       | PROCESS            |
|----------------------------------|-----------------------------|--------------------|
| MICROCONTROLLER OR COMPLEX LOGIC | Digital<br>high density     | CMOS               |
| DATACOM                          | Mixed analog<br>digital     | CMOS<br>analog     |
| MEMORIES                         | High density<br>High speed  | CMOS<br>High speed |
| ASIC                             | Flexibility<br>routeability | CMOS<br>multilayer |





## MHS LITERATURE

In order to provide our customers with a more exhaustive and regularly updated information, MHS has now split its data book into several handbooks.

Following volumes are available :

MICROS - MEMORIES - DATACOM - ASIC - GRAPHIC - HI-REL.

Each volume includes all data pertinent to its topic : data-sheets, application and technical notes, soft-

ware/programming manuals, as well as a cross-reference guide to common industry equivalents, if any.

Last chapters deal with general information : quality and reliability, dice/wafer form products, dice geometry index, package selection & dimensions guides, and sales network.

Separate documents, as well as updated information, can be obtained through MHS sales network.

## DATA SHEET CLASSIFICATION

| CLASSIFICATION      | PRODUCT STAGE              | DISCLAIMERS                                                                                                                                                                  |
|---------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preview             | Formative or design        | This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.                                  |
| Advance Information | Sampling or pre-production | This is advanced information, and specifications are subject to change without notice.                                                                                       |
| Preliminary         | First production           | Additional data may be published at a later date. MHS reserves the right to make changes at any time without notice, to improve design and supply the best possible product. |







|                                  |           |
|----------------------------------|-----------|
| <b>Product index</b>             | <b>1</b>  |
| <b>Cross reference</b>           | <b>2</b>  |
| <b>Ultimate SRAM</b>             | <b>3</b>  |
| <b>High speed CMOS SRAM</b>      | <b>4</b>  |
| <b>High speed BICMOS SRAM</b>    | <b>5</b>  |
| <b>ECL SRAM</b>                  | <b>6</b>  |
| <b>CACHE RAM</b>                 | <b>7</b>  |
| <b>Very low power CMOS SRAM</b>  | <b>8</b>  |
| <b>General purpose CMOS SRAM</b> | <b>9</b>  |
| <b>Smart memories</b>            | <b>10</b> |
| <b>Cache controllers</b>         | <b>11</b> |
| <b>Application notes</b>         | <b>12</b> |
| <b>Packaging</b>                 | <b>13</b> |
| <b>Quality</b>                   | <b>14</b> |
| <b>MHS Locations</b>             | <b>15</b> |





# PRODUCT INDEX





## MEMORIES

### PRODUCT INDEX

#### ULTIMATE CMOS SRAM (high speed & low power)

| FORMAT    | PART NUMBER | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE |
|-----------|-------------|------------|------------|----------|------|
| 64 K x 1  | HM 65687    | 35-45 ns   | 45-55 ns   | 45-55 ns | 3-3  |
| 16 K x 4  | HM 65688    | 35-45 ns   | 45-55 ns   | 45-55 ns | 3-13 |
| 8 K x 8   | HM 65664    | 25-55 ns   | 35-55 ns   | 45-55 ns | 3-23 |
| 256 K x 1 | M 65697     | 35-45 ns   | 45-55 ns   | 45-55 ns | 3-33 |
| 64 K x 4  | M 65698     | 35-45 ns   | 35-45 ns   | 35-45 ns | 3-41 |
| 32 K x 8  | M 65656     | 35-45 ns   | 45-55 ns   | 45-55 ns | 3-49 |

#### HIGH SPEED CMOS SRAM

| FORMAT                                       | PART NUMBER  | ACCESS TIME/GRADE      |                            |                           | PAGE  |
|----------------------------------------------|--------------|------------------------|----------------------------|---------------------------|-------|
|                                              |              | COMMERCIAL<br>0 – 70°C | INDUSTRIAL<br>– 40, + 85°C | MILITARY<br>– 55, + 125°C |       |
| 16 K x 1                                     | HM 65767 (A) | 20-55 ns               | –                          | 25-55 ns                  | 4-3   |
| 4 K x 4                                      | HM 65768 (A) | 20-55 ns               | –                          | 25-55 ns                  | 4-11  |
| 4 K x 4 with $\overline{OE}$                 | HM 65770     | 20-45 ns               | –                          | 25-45 ns                  | 4-21  |
| 4 K x 4 with Sep I/O                         | HM 65772     | 20-45 ns               | –                          | 25-45 ns                  | 4-29  |
| 2 K x 8                                      | HM 65728 (A) | 20-55 ns               | –                          | 35-55 ns                  | 4-37  |
| 64 K x 1                                     | HM 65787     | 15-45 ns               | 25-45 ns                   | 35-45 ns                  | 4-47  |
| 16 K x 4                                     | HM 65788     | 15-45 ns               | 25-45 ns                   | 35-45 ns                  | 4-57  |
| 16 K x 4 with $\overline{OE}$                | HM 65789     | 15-45 ns               | 25-45 ns                   | 35-45 ns                  | 4-65  |
| 16 K x 4 with Sep I/O                        | HM 65790     | 15-45 ns               | 25-45 ns                   | 35-45 ns                  | 4-75  |
| 16 K x 4 with Sep I/O<br>& Transparent Write | HM 65791     | 15-45 ns               | 25-45 ns                   | 35-45 ns                  | 4-85  |
| 8 K x 8                                      | HM 65764     | 15-55 ns               | 25-45 ns                   | 45-55 ns                  | 4-95  |
| 8 K x 9                                      | HM 65779     | 25-55 ns               | 35-45 ns                   |                           | 4-105 |
| 256 K x 1                                    | HM 65797     | 25-45 ns               | 35-45 ns                   | 35-55 ns                  | 4-115 |
| 64 K x 4                                     | HM 65798     | 25-45 ns               | 35-45 ns                   | 35-55 ns                  | 4-123 |
| 64 K x 4 with $\overline{OE}$                | HM 65799     | 25-45 ns               | 35-45 ns                   | 35-55 ns                  | 4-131 |
| 64 K x 4 with Sep I/O                        | HM 65795     | 25-45 ns               | 35-45 ns                   | 35-55 ns                  | 4-139 |
| 64 K x 4 with Sep I/O<br>& Transparent Write | HM 65796     | 25-45 ns               | 35-45 ns                   | 35-55 ns                  | 4-141 |
| 32 K x 8                                     | HM 65756     | 25-55 ns               | 35-55 ns                   | 45-55 ns                  | 4-143 |

#### HIGH SPEED BICMOS SRAM

| FORMAT                        | PART NUMBER | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE |
|-------------------------------|-------------|------------|------------|----------|------|
| 8 K x 8                       | M-65864     | 12-15 ns   | -          | 15-15 ns | 5-3  |
| 16 K x 4                      | M-65888     | 10-15 ns   | -          | 10-15 ns | 5-9  |
| 16 K x 4 with $\overline{OE}$ | M-65889     | 10-15 ns   | -          | 10-15 ns | 5-9  |

## MEMORIES

### ECL SRAM

| FORMAT   | PART NUMBER   | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE |
|----------|---------------|------------|------------|----------|------|
| 256 X 4  | M 10E422 (L)  | 3-7 ns     | -          | -        | 6-3  |
| 256 X 4  | M 100E422 (L) | 3-7 ns     | -          | -        | 6-3  |
| 1024 X 4 | M 10E474 (L)  | 3-7 ns     | -          | -        | 6-9  |
| 1024 X 4 | M 100E474 (L) | 3-7 ns     | -          | -        | 6-9  |

### CACHE RAM

| FORMAT       | PART NUMBER | ACCESS TIME/GRADE | PAGE |
|--------------|-------------|-------------------|------|
|              |             | COMMERCIAL        |      |
| 2 x 4 K x 16 | M-65783     | 25 ns/45 ns       | 7-3  |
| or 8 K x 16  | M-65784     | 25 ns/45 ns       | 7-3  |

### VERY LOW POWER CMOS SRAM

| FORMAT   | PART NUMBER | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE |
|----------|-------------|------------|------------|----------|------|
| 2 K x 8  | HM 65162    | 55-70 ns   | 70-85 ns   | -        | 8-3  |
| 16 K x 1 | HM 65262    | 55-70 ns   | 70-85 ns   | -        | 8-13 |

### GENERAL PURPOSE CMOS SRAM

| FORMAT  | PART NUMBER | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE |
|---------|-------------|------------|------------|----------|------|
| 2 K x 8 | HM 6116     | 120 ns     | 120 ns     | 120 ns   | 9-3  |

\* Consult sales.

### SMART MEMORIES

| FORMAT                      | PART NUMBER | COMMERCIAL | INDUSTRIAL | MILITARY | PAGE  |
|-----------------------------|-------------|------------|------------|----------|-------|
| Dual Port<br>Ram Controller | HMC 6207    | -          | -          | -        | 10-3  |
| Dual Port ram               | HM 65231    | 80 ns      | 100 ns     | 120 ns   | 10-5  |
| DPR 2 K x 8 Master          | M 67132     | 25-55 ns   | -          | 35-55 ns | 10-9  |
| DPR 2K x 8 Slave            | M 67142     | 25-55 ns   | -          | 35-55 ns | 10-9  |
| DPR 2K x 16 Master          | M 67133     | 25-55 ns   | -          | 35-55 ns | 10-13 |
| DPR 2K x 16 Slave           | M 67143     | 25-55 ns   | -          | 35-55 ns | 10-13 |
| DPR 8K x 8                  | M 67005     | 25-55 ns   | -          | 35-55 ns | 10-19 |
| DPR 4K x 16                 | M 67024     | 25-55 ns   | -          | 35-55 ns | 10-3  |
| FiFo 512 x 9                | M 67201     | 25-55 ns   | -          | 35-55 ns | 10-27 |
| FiFo 1K x 9                 | M 67202     | 25-55 ns   | -          | 35-55 ns | 10-37 |

### CACHE CONTROLLERS

| SYSTEM            | PART NUMBER | COMMERCIAL   | PAGE |
|-------------------|-------------|--------------|------|
| 386               | M-82 C 385  | 20-25-33 MHz | 11-3 |
| 386               | M-82 C 395  | 20-25-33 MHz | 11-5 |
| 486 with 82 C 395 | M-82 C 415  | 20-25-33 MHz | 11-7 |

# CROSS REFERENCE





## MEMORIES

2

| <b>MHS</b><br><b>Prefix : HM</b><br><b>or M</b> | <b>CYPRESS</b><br><b>CY</b><br><b>CY</b> |
|-------------------------------------------------|------------------------------------------|
| 65728                                           | 7C128                                    |
| 65767                                           | 7C167                                    |
| 65768                                           | 7C168                                    |
| 65770                                           | 7C170                                    |
| 65772                                           | 7C172                                    |
| 65764                                           | 7C185 (A)                                |
| 65764                                           | 7C186 (A)                                |
| 65788                                           | 7C164 (A)                                |
| 65789                                           | 7C166 (A)                                |
| 65790                                           | 7C162 (A)                                |
| 65787                                           | 7C187 (A)                                |
| 65795                                           | 7C192                                    |
| 65796                                           | 7C191                                    |
| 65798                                           | 7C194                                    |
| 65797                                           | 7C196                                    |
| 65797                                           | 7C197                                    |
| 65756                                           | 7C198                                    |
| 65756                                           | 7C199                                    |
| 65783                                           | 7C183                                    |
| 65784                                           | 7C184                                    |
| 65779                                           | 7C182                                    |
| 65864                                           | 7B185                                    |
| 65864                                           | 7B186                                    |
| 65888                                           | 7B164                                    |
| 65889                                           | 7B166                                    |
| 65890                                           | 7B162                                    |

| <b>MHS</b><br><b>Prefix : HM or M</b> | <b>FAIRCHILD</b><br><b>F</b> |
|---------------------------------------|------------------------------|
| 100E422                               | 100E422                      |
| 100E474                               | 100E474                      |
| 10E422                                | 10E422                       |
| 10E477                                | 10E474                       |
| 65787                                 | 1600                         |
| 65787                                 | 1601                         |
| 65788                                 | 1620                         |
| 65788                                 | 1621                         |
| 65789                                 | 1622                         |

| <b>MHS</b><br><b>Prefix : HM</b><br><b>or M</b> | <b>FUJITSU</b><br><b>MBM</b><br><b>MB</b> |
|-------------------------------------------------|-------------------------------------------|
| 100E422                                         | 100422A                                   |
| 100E474                                         | 100474A                                   |
| 10E422                                          | 10422A                                    |
| 10E474                                          | 10474A                                    |
| 65728                                           | 8128                                      |
| 65767                                           | 8167                                      |
| 65768                                           | 8168                                      |
| 65767                                           | 81C67                                     |
| 65768                                           | 81C68                                     |
| 65787                                           | 8171                                      |
| 65787                                           | 81C71                                     |
| 65788                                           | 81C74                                     |
| 65789                                           | 81C75                                     |
| 65764                                           | 81C78                                     |
| 65764                                           | 8464L                                     |
| 65797                                           | 81C81                                     |
| 65798                                           | 81C84                                     |
| 65795                                           | 81C86                                     |

| <b>MHS</b><br><b>Prefix : HM</b> | <b>AMD</b><br><b>Am</b> |
|----------------------------------|-------------------------|
| 65767                            | 2167                    |
| 65768                            | 2168                    |
| 65768                            | 99C68                   |
| 65768                            | 99CL68                  |
| 65788                            | 99C164                  |
| 65789                            | 99C165                  |
| 65787                            | 99C641                  |
| 65764                            | 99C884H                 |

## MEMORIES

2

| <b>MHS</b><br><b>Prefix : HM</b> | <b>INMOS</b><br><b>IMS</b> |
|----------------------------------|----------------------------|
| 65767                            | 1400                       |
| 65767                            | 1403                       |
| 65767                            | 1403L                      |
| 65768                            | 1420                       |
| 65768                            | 1423                       |
| 65728                            | 1433                       |
| 65787                            | 1600                       |
| 65787                            | 1601L                      |
| 65788                            | 1620                       |
| 65789                            | 1624                       |
| 65788                            | 1625                       |
| 65764                            | 1630                       |
| 65797                            | 1800                       |
| 65798                            | 1820                       |

| <b>MHS</b><br><b>Prefix : HM</b> | <b>HARRIS</b><br><b>HM</b> |
|----------------------------------|----------------------------|
| 65162                            | 65162                      |
| 65262                            | 65262                      |

| <b>MHS</b><br><b>Prefix : HM</b><br><b>or M</b> | <b>HITACHI</b><br><b>HM</b><br><b>HM</b> |
|-------------------------------------------------|------------------------------------------|
| 100E422                                         | 100422                                   |
| 100E474                                         | 100474                                   |
| 10E422                                          | 10422                                    |
| 100E474                                         | 10474                                    |
| 6116L                                           | 6116ALS                                  |
| 6116                                            | 6116AS                                   |
| 65728                                           | 6716                                     |
| 65767                                           | 6167                                     |
| 65767                                           | 6167H                                    |
| 65767                                           | 6167HL                                   |
| 65767                                           | 6167L                                    |
| 65767                                           | 6267                                     |
| 65768                                           | 6268                                     |
| 65768                                           | 6168H                                    |
| 65768                                           | 6168HL                                   |
| 65764                                           | 6264                                     |
| 65787                                           | 6287                                     |
| 65788                                           | 6288                                     |
| 65787                                           | 6787                                     |
| 65788                                           | 6788                                     |

| <b>MHS</b><br><b>Prefix : HM or</b><br><b>M</b> | <b>IDT</b><br><b>IDT</b> |
|-------------------------------------------------|--------------------------|
| 6116L                                           | 6116LA                   |
| 65728                                           | 6116SA                   |
| 65767                                           | 6167L                    |
| 65767                                           | 6167LA                   |
| 65767                                           | 6167S                    |
| 65768                                           | 6168LA                   |
| 65768                                           | 6168SA                   |
| 65770                                           | 61970S                   |
| 65772                                           | 71682L                   |
| 65799                                           | 61298                    |
| 65756                                           | 71256S                   |
| 65797                                           | 71257S                   |
| 65797                                           | 71257                    |
| 65798                                           | 71258                    |
| 67130                                           | 7130L                    |
| 67130                                           | 7130S                    |
| 67132                                           | 7132L                    |
| 67132                                           | 7132S100                 |
| 67140                                           | 7140S                    |
| 67142                                           | 7142S                    |
| 65764                                           | 7164S                    |
| 65787                                           | 7187S                    |
| 65788                                           | 7188S                    |
| 65796                                           | 71981S                   |
| 65795                                           | 71982S                   |

| <b>MHS</b> | <b>INTEL</b> |
|------------|--------------|
| 65767      | 51C66        |
| 65767      | 51C67        |
| 65768      | 51C68        |

| <b>MHS</b><br><b>Prefix : HM</b> | <b>LATTICE</b><br><b>ST</b> |
|----------------------------------|-----------------------------|
| 65768                            | 16K4                        |
| 65728                            | 16K8                        |
| 65789                            | 64E4                        |
| 65787                            | 64K1                        |
| 65788                            | 64K4                        |
| 65764                            | 64K8                        |



## MEMORIES

2

| <b>MHS</b><br>Prefix : HM or M | <b>MICRON</b><br>MT |
|--------------------------------|---------------------|
| 65767                          | 5C1601              |
| 65768                          | 5C1604              |
| 65770                          | 5C1604              |
| 65772                          | 5C1607              |
| 65728                          | 5C1608              |
| 65787                          | 5C6401              |
| 65788                          | 5C6404              |
| 65789                          | 5C6405              |
| 65790                          | 5C6407              |
| 65764                          | 5C6408              |
| 65764                          | 5C6408W             |
| 65783                          | 56C01816            |
| 65784                          | 56C01816            |
| 65756                          | 5C2568              |
| 65797                          | 5C2561              |
| 65788                          | 5C2564              |

| <b>MHS</b><br>Prefix : HM | <b>MISUBISHI</b><br>M5M |
|---------------------------|-------------------------|
| 65767                     | 21C67P                  |
| 65768                     | 21C68P                  |
| 65764                     | 5165L                   |
| 65764                     | 5178P                   |
| 65787                     | 5187P                   |
| 65788                     | 5188P                   |

| <b>MHS</b><br>Prefix : HM or M | <b>MOTOROLA</b><br>MCM |
|--------------------------------|------------------------|
| 10E422                         | 10E422                 |
| 65768                          | 1423                   |
| 6116                           | 2016                   |
| 65728                          | 2018                   |
| 65767                          | 2167                   |
| 65768                          | 6168                   |
| 65768                          | 6268                   |
| 65770                          | 6270                   |
| 65764                          | 6164                   |
| 65764                          | 61L64                  |
| 65787                          | 6287                   |
| 65787                          | 62L87                  |
| 65788                          | 6288                   |

| <b>MHS</b><br>Prefix : HM or M | <b>NEC</b><br>uPD |
|--------------------------------|-------------------|
| 100E422                        | 100422            |
| 100E474                        | 100474            |
| 10E422                         | 10422             |
| 10E474                         | 10474             |
| 65767                          | 2167              |
| 65767                          | 4311              |
| 65787                          | 4361              |
| 65788                          | 4362              |
| 65789                          | 4363              |

| <b>MHS MOSTEK</b><br>Prefix : HM | <b>MK</b> |
|----------------------------------|-----------|
| 65767                            | 41L67     |
| 65767                            | 41H67     |
| 65768                            | 41H68     |

| <b>MHS</b><br>Prefix : M | <b>NATIONAL</b><br>M |
|--------------------------|----------------------|
| 100E422                  | 100422A              |
| 100E474                  | 100474A              |
| 10E422                   | 10422A               |
| 10E474                   | 10474A               |

| <b>MHS</b><br>Prefix : HM | <b>PERFORMANCE</b><br>P |
|---------------------------|-------------------------|
| 65772                     | 4C1682                  |
| 65764                     | 4C164                   |
| 65787                     | 4C187                   |
| 65788                     | 4C188                   |
| 65790                     | 4C1982                  |
| 65789                     | 4C198                   |

| <b>MHS</b><br>Prefix : M | <b>SIGNETICS</b><br>N |
|--------------------------|-----------------------|
| 100E422                  | 100422B               |
| 100E474                  | 100474A               |
| 10E422                   | 10422B                |
| 10E422                   | 10422C                |
| 10E474                   | 10474A                |

MEMORIES

| MHS<br>Prefix : HM | TOSHIBA<br>TMM |
|--------------------|----------------|
| 65728              | 2015A          |
| 65728              | 2018           |
| 65768              | 2068           |
| 65770              | 2078           |
| 65764              | 2088           |
| 65788              | 55416          |
| 65789              | 55417          |
| 65787              | 5561           |
| 62787              | 5562           |

| MHS   | VTI     |
|-------|---------|
| 65728 | 20C18   |
| 65728 | 20C19   |
| 65768 | 20C68   |
| 65770 | 20C78   |
| 65764 | 20C98   |
| 65764 | 20C99   |
| 65788 | VT64KS4 |
| 65789 | VT65KS4 |

# ULTIMATE STATIC RAM

**High Speed and Low Power**





## DATA SHEET

## HM 65687

# 64 k x 1 ULTIMATE CMOS SRAM

## FEATURES

- **ACCESS TIME**  
MILITARY/INDUSTRIAL : 45/55 ns (max)  
COMMERCIAL : 35/45 ns (max)
- **VERY LOW POWER CONSUMPTION**  
ACTIVE : 175.0 mW (typ)  
STANDBY : 2.0  $\mu$ W (typ)  
DATA RETENTION : 0.8  $\mu$ W (typ)
- **WIDE TEMPERATURE RANGE :**  
– 55 TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

3

## DESCRIPTION

The HM 65687 is a very low power CMOS static RAM organized as 65536 x 1 bit. It is manufactured using the MHS high performance CMOS technology named super CMOS.

With this process, MHS is the first to bring the solution for applications where fast computing and low consumption are mandatory, such as the aerospace electronics, the portable instruments or PC's.

Utilising an array of six transistors (6T) memory cells,

the HM 65687 combines an extremely low standby supply current (typical value = 0.1  $\mu$ A) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

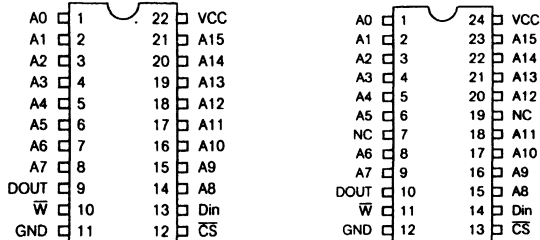
The HM 65687 is processed following the test methods of MIL STD 883C.

## PACKAGES

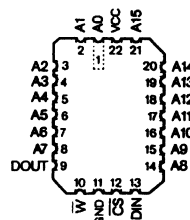
Plastic 300 mils, 22 pins, DIL.  
Ceramic 300 mils, 22 pins, DIL.

SOIC & SOJ\* 300 mils, 24 pins  
LCC, 22 pins.

Pinout DIL 22/24 pins (top view)

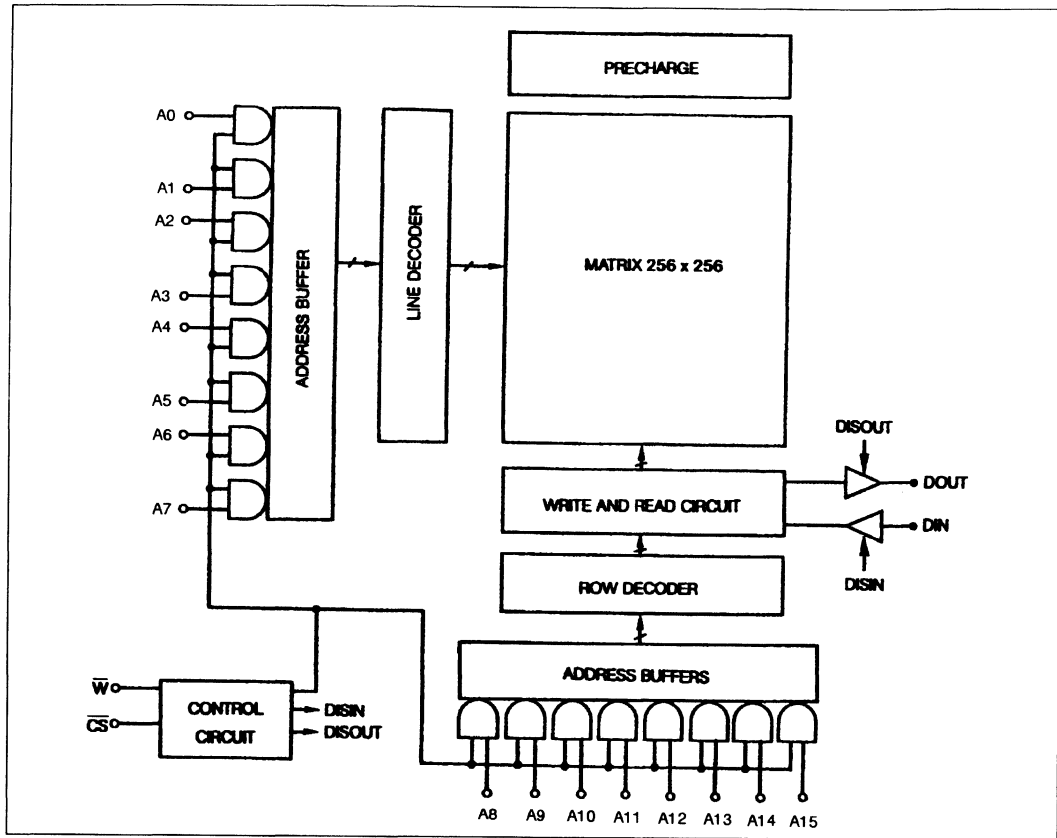


Pinout LCC 22 pins (top view)

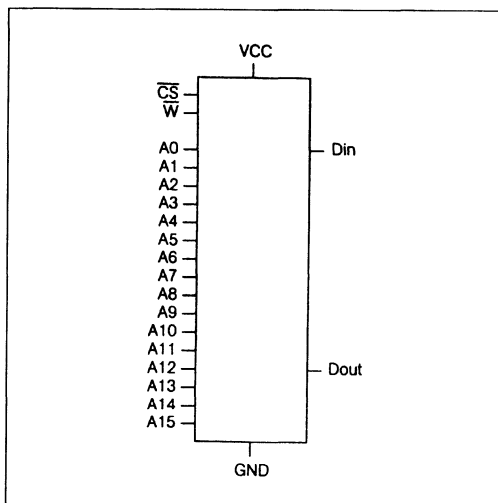


\* preliminary

## BLOCK DIAGRAM



## LOGIC SYMBOL



## PIN NAMES

|                               |                               |
|-------------------------------|-------------------------------|
| A0-A15 : Address inputs       | $\overline{W}$ : Write enable |
| Din : Input                   | $V_{CC}$ : Power              |
| Dout : Output                 | GND : Ground                  |
| $\overline{CS}$ : Chip select |                               |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = High impedance

**ABSOLUTE MAXIMUM RATINGS**Supply voltage to GND potential :  $-0.3\text{ V}$  to  $+7.0\text{ V}$ Input or Output voltage applied : (Gnd  $-0.3\text{ V}$ ) to ( $V_{CC} + 0.3\text{ V}$ )Storage temperature :  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ **OPERATING RANGE**

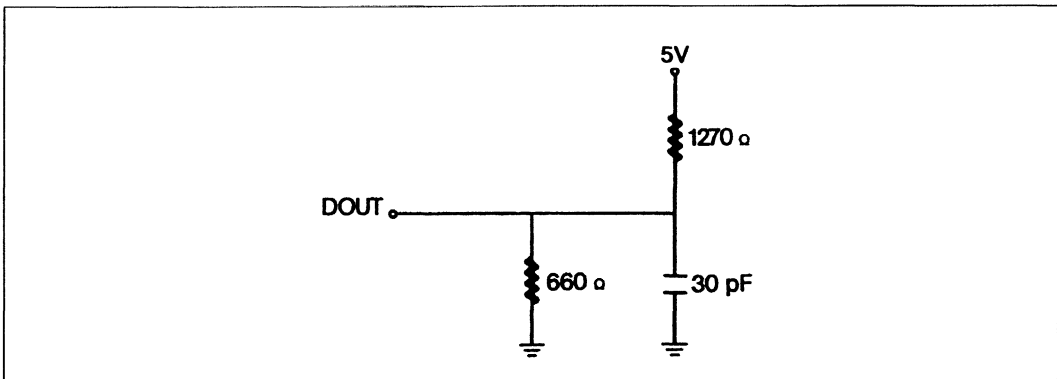
|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE                           |
|------------|-------|-------------------|-------------------------------------------------|
| Military   | (- 2) | $V_{CC} \pm 10\%$ | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $V_{CC} \pm 10\%$ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $V_{CC} \pm 10\%$ | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM                 | UNIT |
|-----------|--------------------|---------|---------|-------------------------|------|
| Vcc       | Supply Voltage     | 4.5     | 5.0     | 5.5                     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0                     | V    |
| VIL (1)   | Input Low Voltage  | $-0.3$  | 0.0     | 0.8                     | V    |
| VIH       | Input High Voltage | 2.2     | —       | $V_{CC} + 0.3\text{ V}$ | V    |

Note : 1. VIL min =  $-0.3\text{ V}$  or  $-1.0\text{ V}$  pulse width 50 ns.**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (2)  | Output capacitance | —       | —       | 7       | pF   |

Note : 2. TA =  $25^{\circ}\text{C}$ , f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.**OUTPUT LOAD**

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------|---------|---------|---------|---------|
| IIX       | (3) | Input leakage current  | - 1.0   | -       | 1.0     | $\mu$ A |
| IOZ       | (3) | Output leakage current | - 1.0   | -       | 1.0     | $\mu$ A |
| VOL       | (4) | Output low voltage     | -       | -       | 0.4     | V       |
| VOH       | (4) | Output high voltage    | 2.4     | -       | -       | V       |

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.

4. Vcc min, IOL = 4.0 mA, IOH = - 1.0 mA.

**Consumption for Commercial specification (- 5) :**

| SYMBOL |     | PARAMETER                | 65687<br>B-5 | 65687<br>S-5 | 65687<br>-5 | 65687<br>C-5 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 10           | 15           | 10          | 15           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 1.0          | 75           | 1.0         | 75           | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 10           | 15           | 10          | 15           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 65           | 75           | 65          | 75           | mA      | max   |

**Consumption for Industrial specification (- 9) :**

| SYMBOL |     | PARAMETER                | 65687<br>B-9 | 65687<br>S-9 | 65687<br>-9 | 65687<br>C-9 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 5.0          | 100.0        | 5.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 75           | 100          | 75          | 100          | mA      | max   |

**Consumption for Military specification (- 2) :**

| SYMBOL |     | PARAMETER                | 65687<br>B-2 | 65687<br>S-2 | 65687<br>-2 | 65687<br>C-2 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 50.0         | 500.0        | 50.0        | 500.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 75           | 100          | 75          | 100          | mA      | max   |

Notes : 5. CS  $\geq$  VIH.

6. CS  $\geq$  Vcc - 0.3 V, Iout = 0 mA.

7. CS  $\leq$  VIL, Iout = 0 mA, Vin = Gnd/Vcc.

8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.



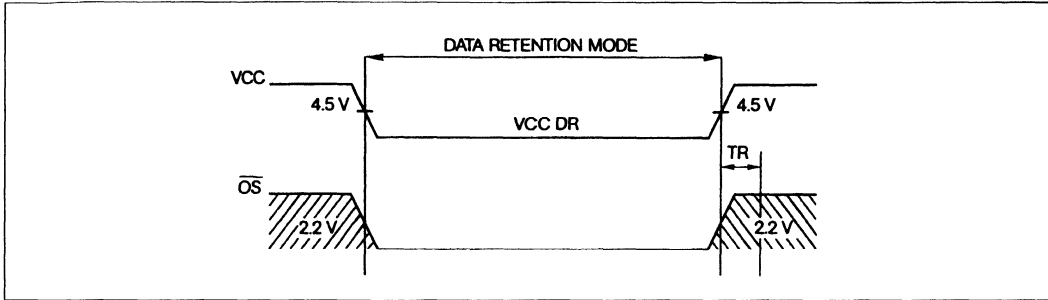
### DATA RETENTION MODE

MHS CMOS RAMs are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V

2.  $\overline{CS}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions
3. The RAM can begin operation > 35 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

### TIMING



3

### DATA RETENTION CHARACTERISTICS

| PARAMETER   | DESCRIPTION                                        | MINIMUM    | TYPICAL<br>(9) | MAXIMUM | UNIT    |
|-------------|----------------------------------------------------|------------|----------------|---------|---------|
| VCCDR       | $V_{CC}$ for data retention                        | 2.0        | —              | —       | V       |
| TCDR        | Chip deselected to data retention time             | 0.0        | —              | —       | ns      |
| TR          | Operation recovery time                            | TAVAV (10) | —              | —       | ns      |
| ICCDR1 (11) | Data retention current<br>@ 2.0 V : HM-65687 (B)-5 | —          | 0.1            | 0.5     | $\mu A$ |
|             | HM-65687 (B)-9                                     | —          | 0.1            | 2.0     | $\mu A$ |
|             | HM-65687 (B)-2                                     | —          | 0.1            | 20.0    | $\mu A$ |
|             | HM-65687S/C-5                                      | —          | 0.1            | 30.0    | $\mu A$ |
|             | HM-65687S/C-9                                      | —          | 0.1            | 30.0    | $\mu A$ |
|             | HM-65687S/C-2                                      | —          | 0.1            | 200.0   | $\mu A$ |
| ICCDR2 (11) | Data retention current<br>@ 3.0 V : HM-65687 (B)-5 | —          | 0.3            | 1.0     | $\mu A$ |
|             | HM-65687 (B)-9                                     | —          | 0.3            | 3.0     | $\mu A$ |
|             | HM-65687 (B)-2                                     | —          | 0.3            | 30.0    | $\mu A$ |
|             | HM-65687S/C-5                                      | —          | 0.3            | 50.0    | $\mu A$ |
|             | HM-65687S/C-9                                      | —          | 0.3            | 50.0    | $\mu A$ |
|             | HM-65687S/C-2                                      | —          | 0.3            | 300.0   | $\mu A$ |

Notes : 9.  $T_A = 25^\circ C$ .

10. TAVAV = Read cycle time.

11.  $\overline{CS} = V_{CC}$ ,  $V_{in} = Gnd/V_{CC}$ , this parameter is only tested to  $V_{CC} = 2$  V.

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output load : 1 TTL gate + 30 pF

**WRITE CYCLE : Commercial specification**

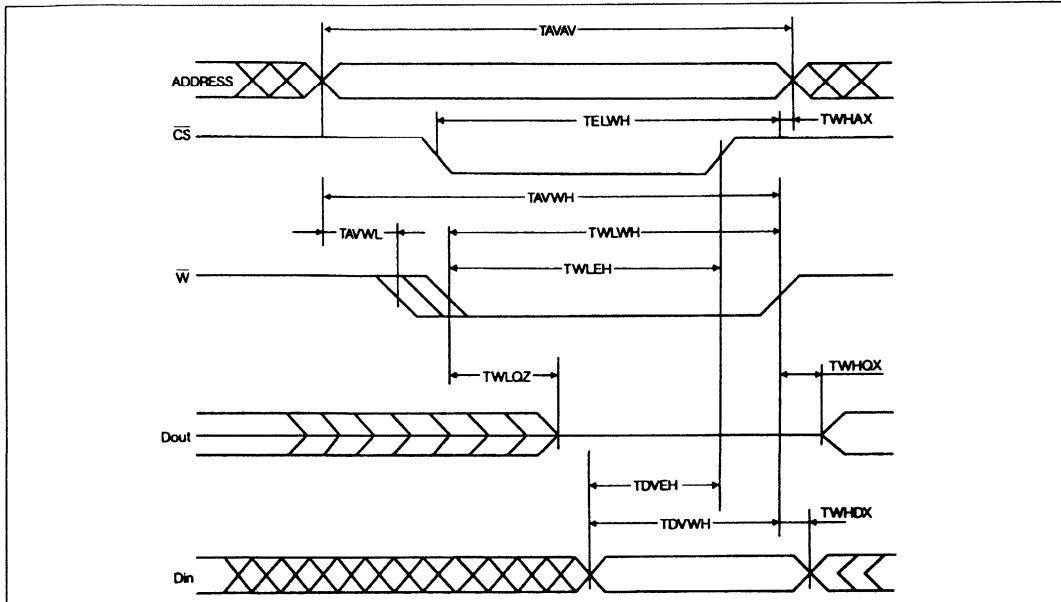
| SYMBOL     | PARAMETER                     | 65687<br>B-5 | 65687<br>S-5 | 65687<br>-5 | 65687<br>C-5 | UNIT | VALUE |
|------------|-------------------------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV      | Write cycle time              | 35           | 35           | 45          | 45           | ns   | min   |
| TAVWL      | Address set-up time           | 0            | 0            | 0           | 0            | ns   | min   |
| TAVWH      | Address valid to end of write | 35           | 35           | 45          | 45           | ns   | min   |
| TDVWH      | Data set-up time              | 20           | 20           | 25          | 25           | ns   | min   |
| TELWH      | CS low to write end           | 35           | 35           | 45          | 45           | ns   | min   |
| TWLQZ (12) | Write low to high Z           | 15           | 15           | 20          | 20           | ns   | max   |
| TWLWH      | Write pulse width             | 30           | 30           | 40          | 40           | ns   | min   |
| TWHAX      | Address hold to end of write  | 5            | 5            | 5           | 5            | ns   | min   |
| TWHDX      | Data hold time                | 3            | 3            | 3           | 3            | ns   | min   |
| TWHQX (12) | Write high to low Z           | 0            | 0            | 0           | 0            | ns   | min   |

**WRITE CYCLE : Industrial and military specification**

| SYMBOL     | PARAMETER                     | 65687<br>B-9/2 | 65687<br>S-9/2 | 65687<br>-9/2 | 65687<br>C-9/2 | UNIT | VALUE |
|------------|-------------------------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV      | Write cycle time              | 45             | 45             | 55            | 55             | ns   | min   |
| TAVWL      | Address set-up time           | 0              | 0              | 0             | 0              | ns   | min   |
| TAVWH      | Address valid to end of write | 45             | 45             | 55            | 55             | ns   | min   |
| TDVWH      | Data set-up time              | 20             | 20             | 25            | 25             | ns   | min   |
| TELWH      | CS low to write end           | 45             | 45             | 55            | 55             | ns   | min   |
| TWLQZ (12) | Write low to high Z           | 15             | 15             | 20            | 20             | ns   | max   |
| TWLWH      | Write pulse width             | 40             | 40             | 50            | 50             | ns   | min   |
| TWHAX      | Address hold to end of write  | 5              | 5              | 5             | 5              | ns   | min   |
| TWHDX      | Data hold time                | 3              | 3              | 3             | 3              | ns   | min   |
| TWHQX (12) | Write high to low Z           | 0              | 0              | 0             | 0              | ns   | min   |

**Note :** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## WRITE CYCLE



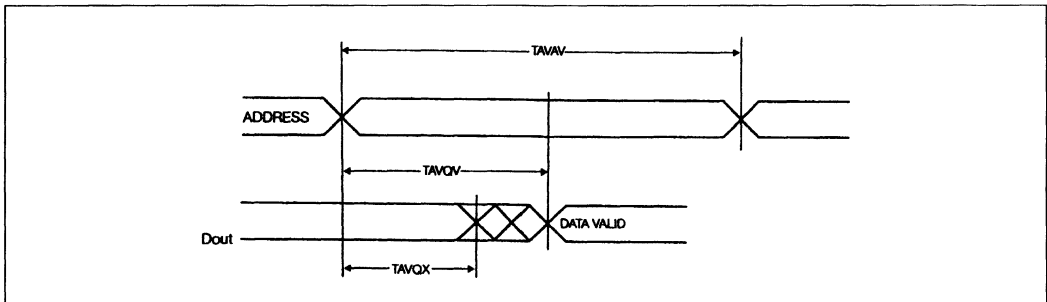
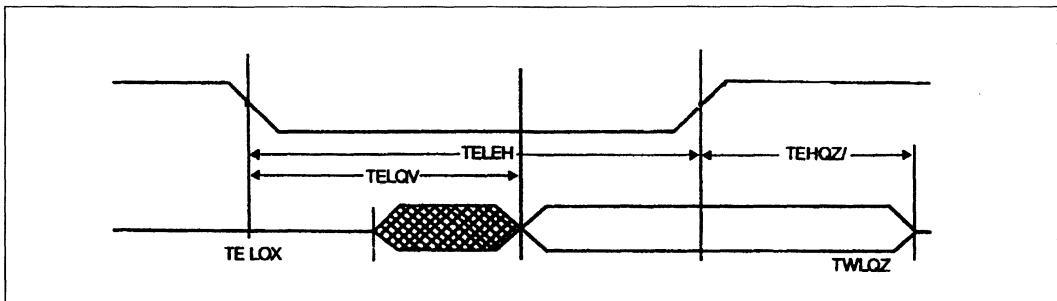
**Note :** The internal write time of the memory is defined by the overlap of CS LOW and W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER                      | 65687<br>B-5 | 65687<br>S-5 | 65687<br>-5 | 65687<br>C-5 | UNIT | VALUE |
|--------|--------------------------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV  | Read cycle time                | 35           | 35           | 45          | 45           | ns   | min   |
| TAVQV  | Address access time            | 35           | 35           | 45          | 45           | ns   | max   |
| TAVQX  | Address Valid to low Z         | 3            | 3            | 3           | 3            | ns   | min   |
| TELQV  | Chip-select access time        | 35           | 35           | 45          | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 5            | 5            | 5           | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z | 35           | 35           | 45          | 45           | ns   | max   |

**READ CYCLE : Industrial and military specification**

| SYMBOL | PARAMETER                      | 65687<br>B-9/2 | 65687<br>S-9/2 | 65687<br>-9/2 | 65687<br>C-9/2 | UNIT | VALUE |
|--------|--------------------------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV  | Read cycle time                | 45             | 45             | 55            | 55             | ns   | min   |
| TAVQV  | Address access time            | 45             | 45             | 55            | 55             | ns   | max   |
| TAVQX  | Address Valid to low Z         | 3              | 3              | 3             | 3              | ns   | min   |
| TELQV  | Chip-select access time        | 45             | 45             | 55            | 55             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 5              | 5              | 5             | 5              | ns   | max   |
| TEHQZ  | $\overline{CS}$ high to high Z | 45             | 45             | 55            | 55             | ns   | max   |

**READ CYCLE nb 1 (notes 13, 14)****READ CYCLE nb 2 (notes 13, 15)**

**Notes :** 13. W is high for read cycle.

14. Device is continuously selected,  $\overline{CS} = V_{IL}$ .

15. Address valid prior to or coincident with CS transitive.

### ORDERING INFORMATION

| Package                                                                                                                             | Device Type                       | Grade                                                                                                               | Level                                                                                                  |
|-------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| HM1                                                                                                                                 | 65687                             | B                                                                                                                   | - 5                                                                                                    |
| 0 - Chip form<br>1 - Ceramic 22 pins<br>3 - Plastic 22 pins - 300 mils<br>4* - LCC 22 pins<br>T* - SOIC 24 pins<br>U* - SOJ 24 pins | 64 k x 1 Ultimate CMOS static RAM | B - high speed/low current<br>S : high speed/standard current<br>Blank : standard speed/low current<br>C : standard | - 5 : Commercial<br>- 9 : Industrial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

\* preliminary

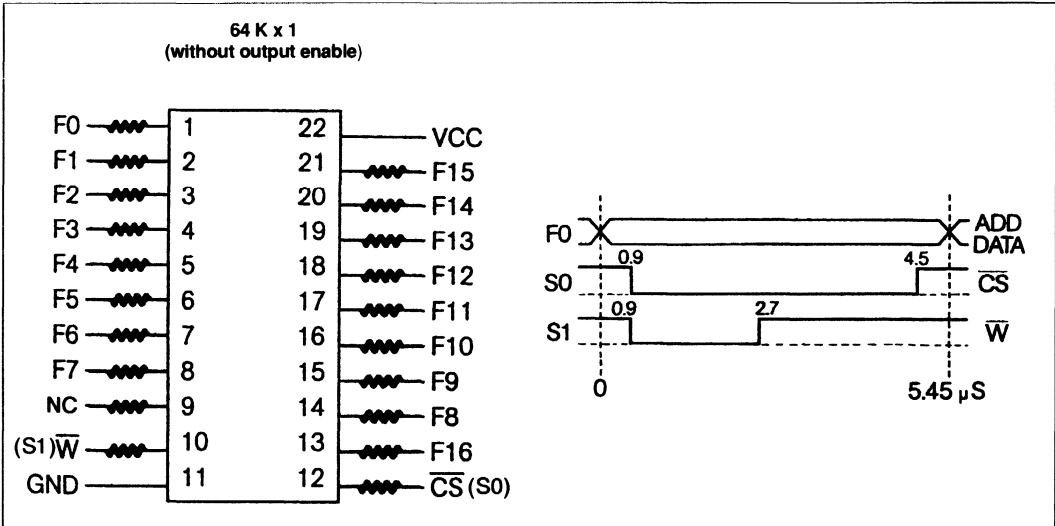
3

### PACKAGE OUTLINE

For the packaging information, refer to chapter 10

Package reference : Plastic DIL, 300 mils, 22 pins  
Ceramic DIL, 300 mils, 22 pins  
SOIC DIL, 300 mils, 24 pins  
LCC rectangular, 22 pins

### BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)

R = 1 KΩ per pin

F0 = 91.6 KHz ± 20 %

Fn = 1/2 F n-1

S0 & S1 : programmable signals for write / read cycles

NC = Non connected.



## DATA SHEET

## HM 65688

# 16 k x 4 ULTIMATE CMOS SRAM

## FEATURES

- ACCESS TIME
  - MILITARY/INDUSTRIAL : 45/55 ns (max)
  - COMMERCIAL : 35/45 ns (max)
- VERY LOW POWER CONSUMPTION
  - ACTIVE : 175.0 mW (typ)
  - STANDBY : 2.0  $\mu$ W (typ)
  - DATA RETENTION : 0.8  $\mu$ W (typ)
- WIDE TEMPERATURE RANGE :
  - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

## DESCRIPTION

The HM 65688 is a very low power CMOS static RAM organised as 16384 x 4 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.

With this process, MHS is the first to bring the solution such as aerospace electronics, the portable instruments or PC's.

Utilising an array of six transistors (6T) memory cells, the HM 65688 combines an extremely low standby sup-

ply current (typical value = 0.1  $\mu$ A) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.

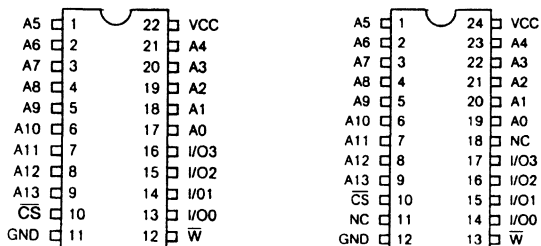
The HM-65688 is processed following the test methods of MIL STD 883C.

## PACKAGES

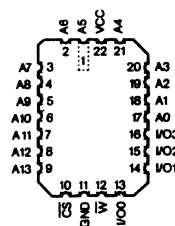
Plastic 300 mils, 22 pins, DIL  
Ceramic 300 mils, 22 pins, DIL

SOIC & SOJ\* 300 mils, 24 pins  
LCC\*, 22 pins

Pinout DIL 22/24 pins (top view)

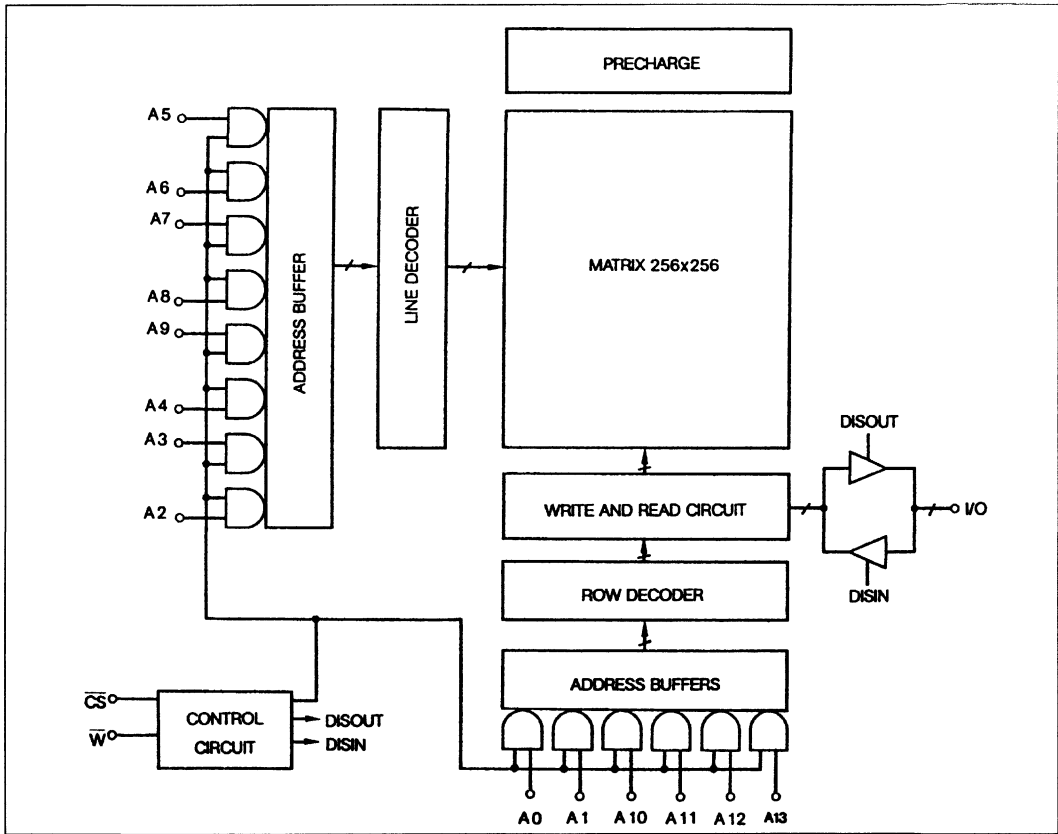


Pinout LCC 22 pins (top view)

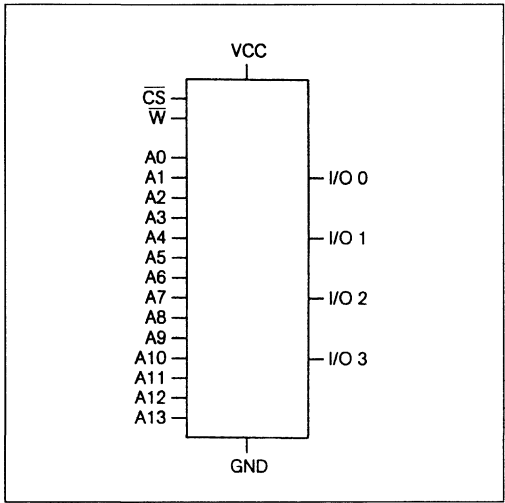


\* preliminary

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

|           |                  |                 |                |
|-----------|------------------|-----------------|----------------|
| A0-A13    | : Address inputs | GND             | : Ground       |
| I/O0-I/O3 | : Inputs/Outputs | $\overline{CS}$ | : Chip-Select  |
| Vcc       | : Power          | $\overline{W}$  | : Write Enable |

TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance



ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V  
Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)  
Storage temperature : - 65°C to + 150°C

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | Vcc ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | Vcc ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | Vcc ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM    | UNIT |
|-----------|--------------------|---------|---------|------------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5        | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0        | V    |
| VIL (1)   | Input low voltage  | - 0.3   | 0.0     | 0.8        | V    |
| VIH       | Input high voltage | 2.2     | -       | Vcc + 0.3V | V    |

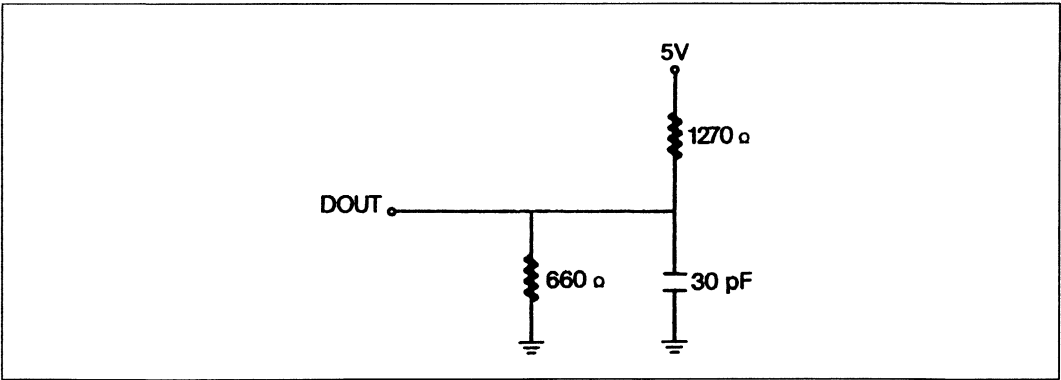
Note : 1. VIL min = - 0.3 V or - 1.0 V pulse width 50 ns.

CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (2)  | Output capacitance | -       | -       | 7       | pF   |

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

OUTPUT LOAD



## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER |     | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------|---------|---------|---------|---------|
| IIX       | (3) | Input leakage current  | - 1.0   | -       | 1.0     | $\mu$ A |
| IOZ       | (3) | Output leakage current | - 1.0   | -       | 1.0     | $\mu$ A |
| VOL       | (4) | Output low voltage     | -       | -       | 0.4     | V       |
| VOH       | (4) | Output high voltage    | 2.4     | -       | -       | V       |

Notes : 3.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  output disabled.

4.  $V_{cc}$  min,  $I_{OL} = 4.0$  mA,  $I_{OH} = - 1.0$  mA.

## Consumption for Commercial specification (- 5) :

| SYMBOL |     | PARAMETER                | 65688<br>B-5 | 65688<br>S-5 | 65688<br>-5 | 65688<br>C-5 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 10           | 15           | 10          | 15           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 1.0          | 75           | 1.0         | 75           | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 10           | 15           | 10          | 15           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 65           | 75           | 65          | 75           | mA      | max   |

## Consumption for Industrial specification (- 9) :

| SYMBOL |     | PARAMETER                | 65688<br>B-9 | 65688<br>S-9 | 65688<br>-9 | 65688<br>C-9 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 5.0          | 100.0        | 5.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 75           | 100          | 75          | 100          | mA      | max   |

## Consumption for Military specification (- 2) :

| SYMBOL |     | PARAMETER                | 65688<br>B-2 | 65688<br>S-2 | 65688<br>-2 | 65688<br>C-2 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 50.0         | 500.0        | 50.0        | 500.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP  | (8) | Operating supply current | 75           | 100          | 75          | 100          | mA      | max   |

Notes : 5.  $CS \geq V_{IH}$ .

6.  $CS \geq V_{cc} - 0.3$  V,  $I_{out} = 0$  mA.

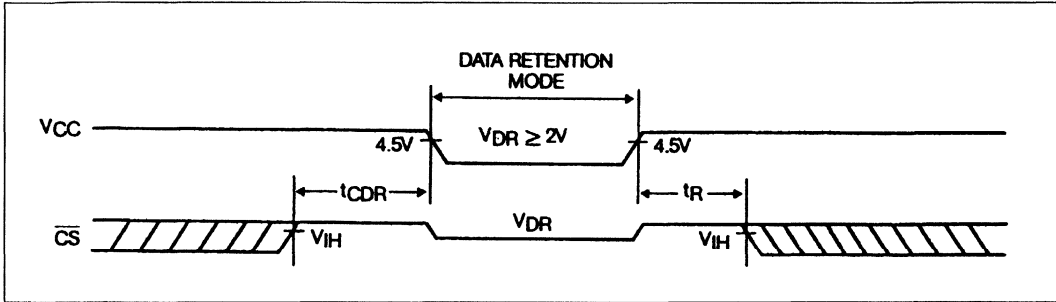
7.  $CS \leq V_{IL}$ ,  $I_{out} = 0$  mA,  $V_{in} = Gnd/V_{cc}$ .

8.  $V_{cc}$  max,  $I_{out} = 0$  mA,  $f = \text{max}$ ,  $V_{in} = Gnd/V_{cc}$ .

**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3V$ .
2.  $\overline{CS}$  must be kept between  $V_{CC} + 0.3 V$  and 70 % of  $V_{CC}$  during the power up and power down transitions.
3. The RAM can begin operation  $> 35$  ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

**TIMING****3****DATA RETENTION CHARACTERISTICS**

| PARAMETER   | DESCRIPTION                                       | MINIMUM    | TYPICAL<br>(9) | MAXIMUM | UNIT    |
|-------------|---------------------------------------------------|------------|----------------|---------|---------|
| VCCDR       | Vcc for data retention                            | 2.0        | —              | —       | V       |
| TCDR        | Chip deselect to data retention time              | 0.0        | —              | —       | ns      |
| TR          | Operation recovery time                           | TAVAV (10) | —              | —       | ns      |
| ICCDR1 (11) | Data retention current<br>@ 2.0 V : HM-65664(B)-5 | —          | 0.1            | 0.5     | $\mu A$ |
|             | HM-65664(B)-9                                     | —          | 0.1            | 2.0     | $\mu A$ |
|             | HM-65664(B)-2                                     | —          | 0.1            | 20.0    | $\mu A$ |
|             | HM-65664S/C-5                                     | —          | 0.1            | 30.0    | $\mu A$ |
|             | HM-65664S/C-9                                     | —          | 0.1            | 30.0    | $\mu A$ |
|             | HM-65664S/C-2                                     | —          | 0.1            | 200.0   | $\mu A$ |
| ICCDR2 (11) | Data retention current<br>@ 3.0 V : HM-65664(B)-5 | —          | 0.3            | 1.0     | $\mu A$ |
|             | HM-65664(B)-9                                     | —          | 0.3            | 3.0     | $\mu A$ |
|             | HM-65664(B)-2                                     | —          | 0.3            | 30.0    | $\mu A$ |
|             | HM-65664S/C-5                                     | —          | 0.3            | 50.0    | $\mu A$ |
|             | HM-65664S/C-9                                     | —          | 0.3            | 50.0    | $\mu A$ |
|             | HM-65664S/C-2                                     | —          | 0.3            | 300.0   | $\mu A$ |

Notes : 9.  $T_A = 25^\circ C$ .

10. TAVAV = Read cycle time.

11.  $CS = V_{CC}$ ,  $V_{IN} = Gnd/V_{CC}$ , this parameter is only tested to  $V_{CC} = 2 V$ .

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output load : 1 TTL gate + 30 pF

**WRITE CYCLE : Commercial specification**

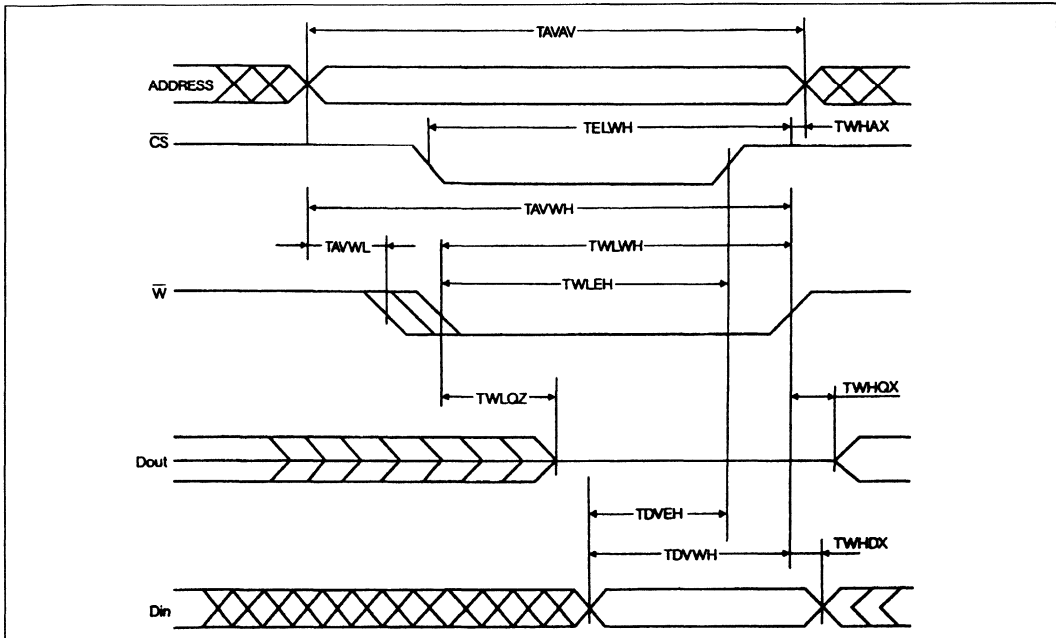
| SYMBOL     | PARAMETER                         | 65664<br>B-5 | 65664<br>S-5 | 65664<br>-5 | 65664<br>C-5 | UNIT | VALUE |
|------------|-----------------------------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV      | Write cycle time                  | 35           | 45           | 45          | 55           | ns   | min   |
| TAVWL      | Address set-up time               | 0            | 0            | 0           | 0            | ns   | min   |
| TAVWH      | Address valid to end of write     | 35           | 45           | 45          | 55           | ns   | min   |
| TDVWH      | Data set-up time                  | 15           | 20           | 20          | 25           | ns   | min   |
| TEL1WH     | $\overline{CS1}$ low to write end | 35           | 45           | 45          | 55           | ns   | min   |
| TEH2WH     | CS2 low to write end              | 35           | 45           | 45          | 55           | ns   | min   |
| TWLQZ (12) | Write low to high Z               | 12           | 15           | 15          | 20           | ns   | max   |
| TWLWH      | Write pulse width                 | 30           | 40           | 40          | 50           | ns   | min   |
| TWHAX      | Address hold to end of write      | 5            | 5            | 5           | 5            | ns   | min   |
| TWHDX      | Data hold time                    | 3            | 3            | 3           | 3            | ns   | min   |
| TWHQX (12) | Write high to low Z               | 0            | 0            | 0           | 0            | ns   | min   |

**WRITE CYCLE : Industrial and Military specification**

| SYMBOL     | PARAMETER                         | 65664<br>B-9/2 | 65664<br>S-9/2 | 65664<br>-9/2 | 65664<br>C-9/2 | UNIT | VALUE |
|------------|-----------------------------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV      | Write cycle time                  | 45             | 45             | 55            | 55             | ns   | min   |
| TAVWL      | Address set-up time               | 0              | 0              | 0             | 0              | ns   | min   |
| TAVWH      | Address valid to end of write     | 45             | 45             | 55            | 55             | ns   | min   |
| TDVWH      | Data set-up time                  | 20             | 20             | 25            | 25             | ns   | min   |
| TEL1WH     | $\overline{CS1}$ low to write end | 45             | 45             | 55            | 55             | ns   | min   |
| TEH2WH     | CS2 low to write end              | 45             | 45             | 55            | 55             | ns   | min   |
| TWLQZ (12) | Write low to high Z               | 15             | 15             | 20            | 20             | ns   | max   |
| TWLWH      | Write pulse width                 | 40             | 40             | 50            | 50             | ns   | min   |
| TWHAX      | Address hold to end of write      | 5              | 5              | 5             | 5              | ns   | min   |
| TWHDX      | Data hold time                    | 3              | 3              | 3             | 3              | ns   | min   |
| TWHQX (12) | Write high to low Z               | 0              | 0              | 0             | 0              | ns   | min   |

**Note :** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## WRITE CYCLE



**Note :** The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**READ CYCLE : Commercial specification**

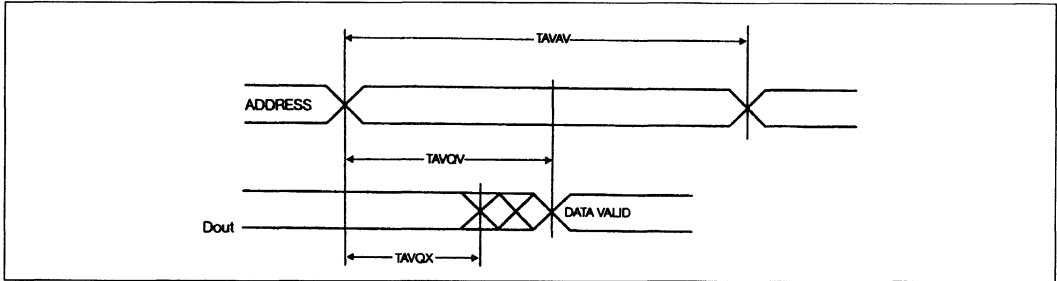
| SYMBOL | PARAMETER                      | 65688<br>B-5 | 65688<br>S-5 | 65688<br>-5 | 65688<br>C-5 | UNIT | VALUE |
|--------|--------------------------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV  | Read cycle time                | 35           | 35           | 45          | 45           | ns   | min   |
| TAVQV  | Address access time            | 35           | 35           | 45          | 45           | ns   | max   |
| TAVQX  | Address valid to low Z         | 5            | 5            | 5           | 5            | ns   | min   |
| TELQV  | Chip-select access time        | 40           | 40           | 50          | 50           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 5            | 5            | 5           | 5            | ns   | max   |
| TEHQZ  | $\overline{CS}$ high to high Z | 35           | 35           | 45          | 45           | ns   | max   |

3

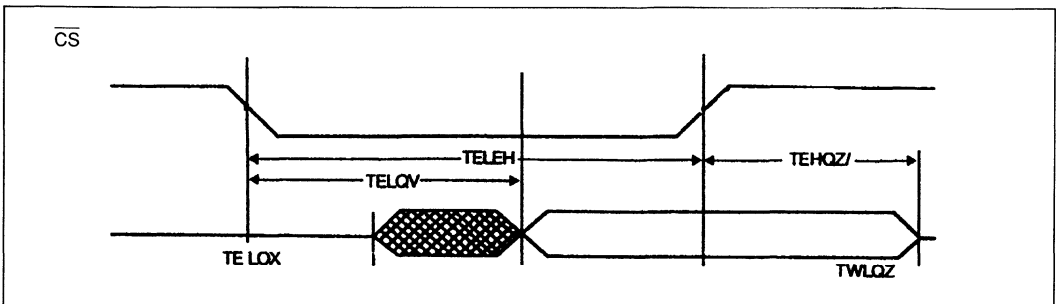
**READ CYCLE : Industrial and military specification**

| SYMBOL | PARAMETER                      | 65688<br>B-9/2 | 65688<br>S-9/2 | 65688<br>-9/2 | 65688<br>C-9/2 | UNIT | VALUE |
|--------|--------------------------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV  | Read cycle time                | 45             | 45             | 55            | 55             | ns   | min   |
| TAVQV  | Address access time            | 45             | 45             | 55            | 55             | ns   | max   |
| TAVQX  | Address Valid to low Z         | 5              | 5              | 5             | 5              | ns   | min   |
| TELQV  | Chip-select access time        | 50             | 50             | 65            | 65             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 5              | 5              | 5             | 5              | ns   | max   |
| TEHQX  | $\overline{CS}$ high to high Z | 45             | 45             | 55            | 55             | ns   | max   |

**READ CYCLE nb 1 (notes 13, 14)**



**READ CYCLE nb 2 (notes 13, 15)**



- Notes :** 13.  $\overline{W}$  is high for read cycle.  
 14. Device is continuously selected,  $\overline{CS} = \text{VIL}$ .  
 15. Address valid prior to or coincident with  $\overline{CS}$  transitive low.

### ORDERING INFORMATION

| Package                                                                                                                           | Device Type                          | Grade                                                                                                                     | Level                                                                                                  |
|-----------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| HM1                                                                                                                               | 65688                                | B                                                                                                                         | -5                                                                                                     |
| 0 - Chip form<br>1 - Ceramic 22 pins<br>3 - Plastic 22 pins 300 mils<br>4* - LCC 22 pins<br>T* - SOIC 24 pins<br>U* - SQJ 24 pins | 16 k x 4 Ultimate CMOS<br>static RAM | B - high speed/low current<br>S : high speed/standard<br>current<br>Blank : standard speed/low<br>current<br>C : standard | - 5 : Commercial<br>- 9 : Industrial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

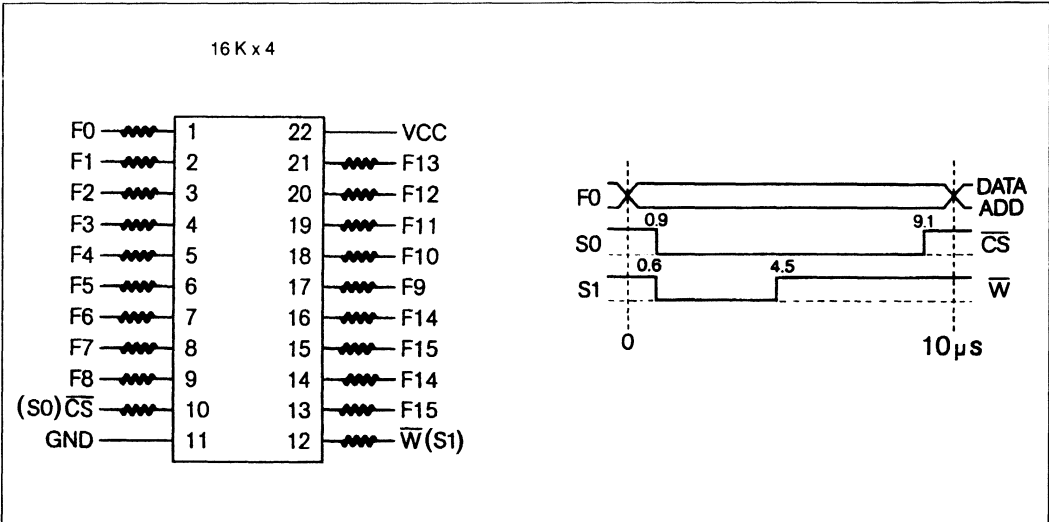
\* preliminary

### PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins  
 Ceramic DIL, 300 mils, 22 pins  
 SOIC DIL, 300 mils, 24 pins  
 LCC rectangular, 22 pins

### BURN-IN SCHEMATICS



VCC = 5 V (- 0, + 0.5)

R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %

Fn = 1/2 Fn-1

S0 et S1 : programmable signals for  
 write / read cycles







September 1990

## DATA SHEET

## HM 65664

# 8 K x 8 ULTIMATE CMOS SRAM

## FEATURES

- **ACCESS TIME**  
MILITARY : 35/45/55 ns (max)  
INDUSTRIAL/COMMERCIAL : 25\*/35/55 ns (max)
- **VERY LOW POWER CONSUMPTION**  
ACTIVE : 175.0 mW (typ)  
STANDBY : 2.0  $\mu$ W (typ)  
DATA RETENTION : 0.8  $\mu$ W (typ)
- **WIDE TEMPERATURE RANGE :**  
– 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

\* Preliminary.

## DESCRIPTION

The HM 65664 is a very low power CMOS static RAM organized as 8192 x 8 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.

With this process, MHS is the first to bring the solution such as aerospace electronics or portable instruments PC's.

Utilising an array of six transistors (6T) memory cells, the HM 65664 combines an extremely low standby

supply current (typical value = 0.1  $\mu$ A) with a fast access time at 25 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.

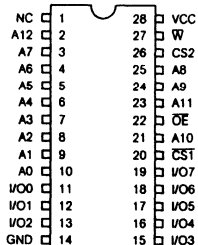
The HM 65664 is processed following the test methods of MIL STD 883C.

## PACKAGES

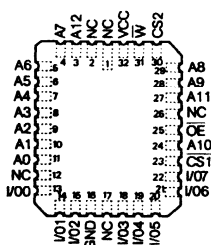
Plastic 300 & 600 mils, 28 pins, DIL.  
Ceramic 300 & 600 mils, 28 pins, DIL.

SOIC&SOJ 300 mils/330 mils, 28 pins  
LCC, 32 pins.

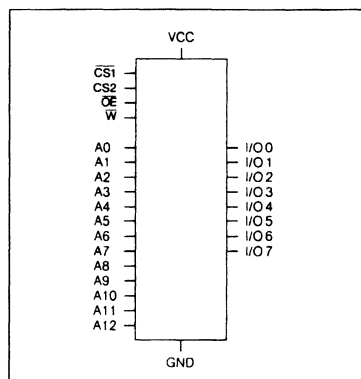
Pinout DIL 28 pins (top view)



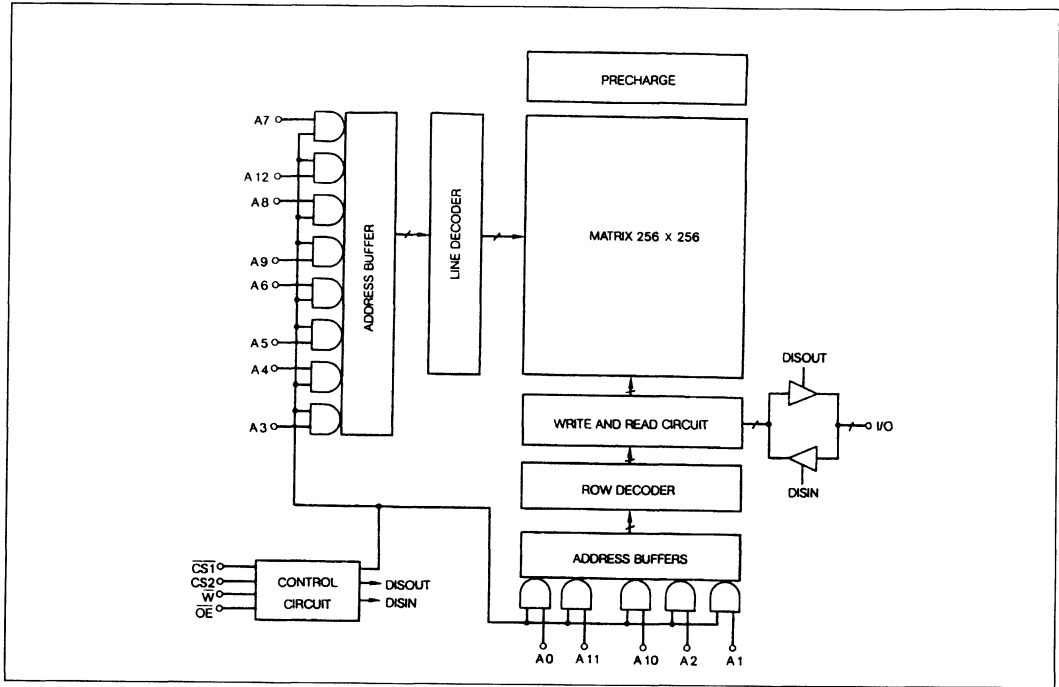
Pinout LCC 32 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                          |                                  |
|--------------------------|----------------------------------|
| A0-A12 : Address inputs  | $\overline{CS1}$ : Chip-select 1 |
| I/O0-I/O7 : Input/Output | CS2 : Chip-select 2              |
| Vcc : Power              | $\overline{OE}$ : Output Enable  |
| Gnd : Ground             | $\overline{W}$ : Write enable    |

TRUTH TABLE

| $\overline{CS1}$ | CS2 | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE           |
|------------------|-----|-----------------|----------------|---------|----------|----------------|
| H                | X   | X               | X              | Z       | Z        | Deselect       |
| L                | H   | L               | H              | Z       | Valid    | Read           |
| L                | H   | X               | L              | Valid   | Z        | Write          |
| L                | H   | H               | H              | Z       | Z        | Output disable |

L = low, H = high, X = H or L, Z = high impedance.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V}$  to  $+7.0\text{ V}$

Input or Output voltage applied :  $(\text{Gnd} - 0.3\text{ V})$  to  $(\text{Vcc} + 0.3\text{ V})$

Storage temperature :  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                           |
|------------|-------|-----------------------|-------------------------------------------------|
| Military   | (- 2) | $\text{Vcc} \pm 10\%$ | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $\text{Vcc} \pm 10\%$ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $\text{Vcc} \pm 10\%$ | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM                     | UNIT |
|-----------|--------------------|---------|---------|-----------------------------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5                         | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0                         | V    |
| VIL (1)   | Input low voltage  | - 0.3   | 0.0     | 0.8                         | V    |
| VIH       | Input high voltage | 2.2     | —       | $\text{Vcc} + 0.3\text{ V}$ | V    |

**Note :** 1. VIL min = - 0.3 V or - 1.0 V pulse width 50 ns.

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | —       | —       | 8       | pF   |
| Cout (2)  | Output capacitance | —       | —       | 8       | pF   |

**Note :** 2. TA =  $25^{\circ}\text{C}$ , f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|------------------------|---------|---------|---------|---------|
| IIX (3)   | Input leakage current  | - 1.0   | -       | 10.0    | $\mu$ A |
| IOZ (3)   | Output leakage current | - 1.0   | -       | 1.0     | $\mu$ A |
| VOL (4)   | Output low voltage     | -       | -       | 0.4     | V       |
| VOH (4)   | Output high voltage    | 2.4     | -       | -       | V       |

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.

4. Vcc min, IOL = 4.0 mA, IOH = - 1.0 mA.

## Consumption for Commercial specification ( - 5 ) :

| SYMBOL     | PARAMETER                | 65664<br>Q-5 | 65664<br>B-5 | 65664<br>S-5 | 65664<br>-5 | 65664<br>C-5 | UNIT    | VALUE |
|------------|--------------------------|--------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB (5)  | Standby supply current   | 15           | 10           | 15           | 10          | 15           | mA      | max   |
| ICCSB1 (6) | Standby supply current   | 75           | 10           | 75           | 1.0         | 75           | $\mu$ A | max   |
| ICC (7)    | Operating supply current | 15           | 10           | 15           | 10          | 15           | mA      | max   |
| ICCOP (8)  | Operating supply current | 75           | 65           | 75           | 65          | 75           | mA      | max   |

## Consumption for Industrial specification ( - 9 ) :

| SYMBOL     | PARAMETER                | 65664<br>Q-9 | 65664<br>B-9 | 65664<br>S-9 | 65664<br>-9 | 65664<br>C-9 | UNIT    | VALUE |
|------------|--------------------------|--------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB (5)  | Standby supply current   | 20           | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 (6) | Standby supply current   | 100          | 5.0          | 100.0        | 5.0         | 100.0        | $\mu$ A | max   |
| ICC (7)    | Operating supply current | 20           | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP (8)  | Operating supply current | 100          | 75           | 100          | 75          | 100          | mA      | max   |

## Consumption for Military specification ( - 2 ) :

| SYMBOL     | PARAMETER                | 65664<br>B-2 | 65664<br>S-2 | 65664<br>-2 | 65664<br>C-2 | UNIT    | VALUE |
|------------|--------------------------|--------------|--------------|-------------|--------------|---------|-------|
| ICCSB (5)  | Standby supply current   | 15           | 20           | 15          | 20           | mA      | max   |
| ICCSB1 (6) | Standby supply current   | 50.0         | 500.0        | 50.0        | 500.0        | $\mu$ A | max   |
| ICC (7)    | Operating supply current | 15           | 20           | 15          | 20           | mA      | max   |
| ICCOP (8)  | Operating supply current | 75           | 100          | 75          | 100          | mA      | max   |

Notes : 5. CS1  $\geq$  VIH, CS2  $\leq$  VIL.

6. CS1  $\geq$  Vcc - 0.3V, CS2  $\leq$  0.3 V, Iout = 0 mA.

7. CS1  $\leq$  VIL, CSE  $\geq$  VIH, Iout = 0 mA, Vin = Gnd/Vcc.

8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

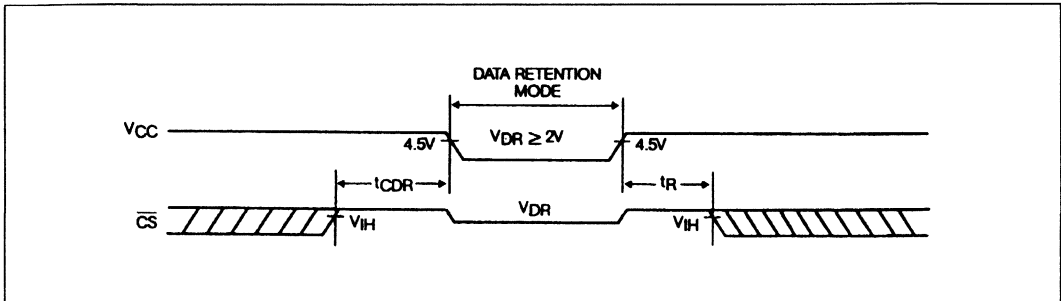
**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the

RAM outputs high impedance, minimizing power dissipation.

3.  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3$ V and 70 % of  $V_{CC}$  during the power up and power down transitions.
4. The RAM can begin operation > 45 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

**TIMING**

3

**DATA RETENTION CHARACTERISTICS**

| PARAMETER   | DESCRIPTION                                    | MINIMUM    | TYPICAL<br>(9) | MAXIMUM | UNIT    |
|-------------|------------------------------------------------|------------|----------------|---------|---------|
| VCCDR       | Vcc for data retention                         | 2.0        | —              | —       | V       |
| TCDR        | Chip deselect to data retention time           | 0.0        | —              | —       | ns      |
| TR          | Operation recovery time                        | TAVAV (10) | —              | —       | ns      |
| ICCDR1 (11) | Data retention current @ 2.0 V : HM-65664(B)-5 | —          | 0.1            | 0.5     | $\mu$ A |
|             | HM-65664(B)-9                                  | —          | 0.1            | 3.0     | $\mu$ A |
|             | HM-65664(B)-2                                  | —          | 0.1            | 20.0    | $\mu$ A |
|             | HM-65664S/C/Q-5                                | —          | 0.1            | 30.0    | $\mu$ A |
|             | HM-65664S/C/Q-9                                | —          | 0.1            | 30.0    | $\mu$ A |
|             | HM-65664S/C-2                                  | —          | 0.1            | 200.0   | $\mu$ A |
| ICCDR2 (11) | Data retention current @ 3.0 V : HM-65664(B)-5 | —          | 0.3            | 1.0     | $\mu$ A |
|             | HM-65664(B)-9                                  | —          | 0.3            | 3.0     | $\mu$ A |
|             | HM-65664(B)-2                                  | —          | 0.3            | 30.0    | $\mu$ A |
|             | HM-65664S/C/Q-5                                | —          | 0.3            | 50.0    | $\mu$ A |
|             | HM-65664S/C/Q-9                                | —          | 0.3            | 50.0    | $\mu$ A |
|             | HM-65664S/C-2                                  | —          | 0.3            | 300.0   | $\mu$ A |

Notes : 9.  $T_A = 25^\circ\text{C}$ .

10. TAVAV = Read cycle time.

11.  $\overline{CS} = V_{CC}$ ,  $V_{in} = \text{Gnd}/v_{cc}$ , this parameter is only tested to  $V_{CC} = 2$  V.

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

### AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
Input rise : 5 ns

Input timing reference levels : 1.5 V  
Output load : 1 TTL gate + 30 pF

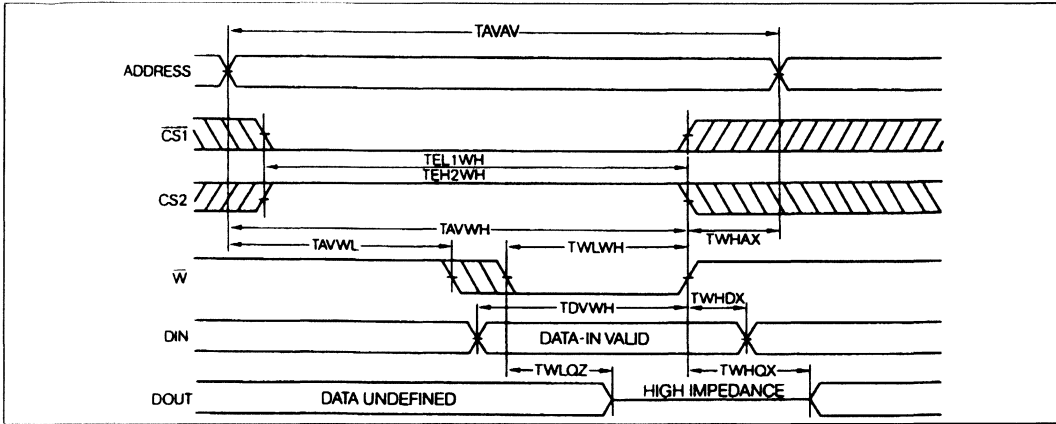
### WRITE CYCLE : Commercial specification

| SYMBOL     | PARAMETER                     | 65664<br>Q-5 | 65664<br>B-5 | 65664<br>S-5 | 65664<br>-5 | 65664<br>C-5 | UNIT | VALUE |
|------------|-------------------------------|--------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV      | Write cycle time              | 35           | 45           | 45           | 55          | 55           | ns   | min   |
| TAVWL      | Address set-up time           | 0            | 0            | 0            | 0           | 0            | ns   | min   |
| TAVWH      | Address valid to end of write | 35           | 45           | 45           | 55          | 55           | ns   | min   |
| TDVWH      | Data set-up time              | 22           | 25           | 25           | 25          | 25           | ns   | min   |
| TEL1WH     | CS1 low to write end          | 35           | 45           | 45           | 55          | 55           | ns   | min   |
| TEH2WH     | CS2 low to write end          | 35           | 45           | 45           | 55          | 55           | ns   | min   |
| TWLQZ (12) | Write low to high Z           | 15           | 15           | 15           | 20          | 20           | ns   | max   |
| TWLWH      | Write pulse width             | 30           | 40           | 40           | 50          | 50           | ns   | min   |
| TWHAX      | Address hold to end of write  | 5            | 5            | 5            | 5           | 5            | ns   | min   |
| TWHDX      | Data hold time                | 3            | 3            | 3            | 3           | 3            | ns   | min   |
| TWHQX (12) | Write high to low Z           | 0            | 0            | 0            | 0           | 0            | ns   | min   |

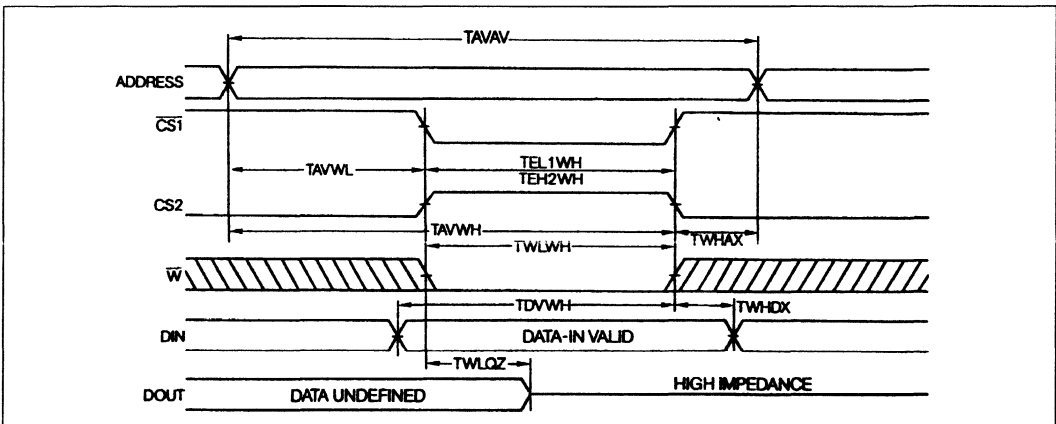
### WRITE CYCLE : Industrial and Military specification

| SYMBOL     | PARAMETER                     | 65664<br>Q-9 | 65664<br>B-9/2 | 65664<br>S-9/2 | 65664<br>-9/2 | 65664<br>C-9/2 | UNIT | VALUE |
|------------|-------------------------------|--------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV      | Write cycle time              | 35           | 45             | 45             | 55            | 55             | ns   | min   |
| TAVWL      | Address set-up time           | 0            | 0              | 0              | 0             | 0              | ns   | min   |
| TAVWH      | Address valid to end of write | 35           | 45             | 45             | 55            | 55             | ns   | min   |
| TDVWH      | Data set-up time              | 22           | 25             | 25             | 25            | 25             | ns   | min   |
| TEL1WH     | CS1 low to write end          | 35           | 45             | 45             | 55            | 55             | ns   | min   |
| TEH2WH     | CS2 low to write end          | 35           | 45             | 45             | 55            | 55             | ns   | min   |
| TWLQZ (12) | Write low to high Z           | 15           | 15             | 15             | 20            | 20             | ns   | max   |
| TWLWH      | Write pulse width             | 30           | 40             | 40             | 50            | 50             | ns   | min   |
| TWHAX      | Address hold to end of write  | 5            | 5              | 5              | 5             | 5              | ns   | min   |
| TWHDX      | Data hold time                | 3            | 3              | 3              | 3             | 3              | ns   | min   |
| TWHQX (12) | Write high to low Z           | 0            | 0              | 0              | 0             | 0              | ns   | min   |

**Note :** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 13)

3

WRITE CYCLE 2  $\overline{CS1}$  CONTROLLED (note 13)

**Note : 13.** The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
Data out is high impedance if  $\overline{OE} = \text{VIH}$ .

**READ CYCLE : Commercial specification**

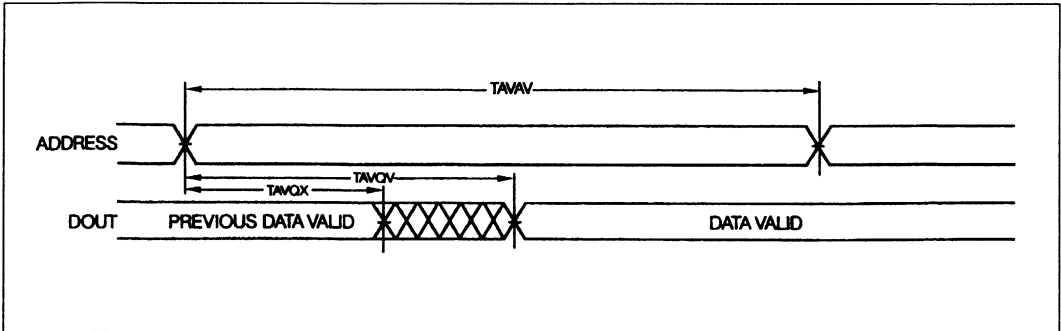
| SYMBOL | PARAMETER                       | 65664<br>Q-5 | 65664<br>B-5 | 65664<br>S-5 | 65664<br>-5 | 65664<br>C-5 | UNIT | VALUE |
|--------|---------------------------------|--------------|--------------|--------------|-------------|--------------|------|-------|
| TAVAV  | Read cycle time                 | 35           | 45           | 45           | 55          | 55           | ns   | min   |
| TAVQV  | Address access time             | 35           | 45           | 45           | 55          | 55           | ns   | max   |
| TAVQX  | Address valid to low Z          | 3            | 3            | 3            | 3           | 3            | ns   | min   |
| TEL1QV | Chip-select 1 access time       | 35           | 45           | 45           | 55          | 55           | ns   | max   |
| TEH2QV | Chip-select 2 access time       | 35           | 45           | 45           | 55          | 55           | ns   | max   |
| TEL1QX | $\overline{CS1}$ low to low Z   | 5            | 5            | 5            | 5           | 5            | ns   | min   |
| TEH2QX | CS2 to low Z                    | 5            | 5            | 5            | 5           | 5            | ns   | min   |
| TEH1QZ | $\overline{CS1}$ high to high Z | 35           | 45           | 45           | 55          | 55           | ns   | max   |
| TEL2QZ | CS2 low to high Z               | 35           | 45           | 45           | 55          | 55           | ns   | max   |
| TGLQV  | Output Enable access time       | 15           | 15           | 15           | 20          | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z    | 5            | 5            | 5            | 5           | 5            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z  | 15           | 15           | 15           | 20          | 20           | ns   | max   |

**READ CYCLE : Industrial and Military specification**

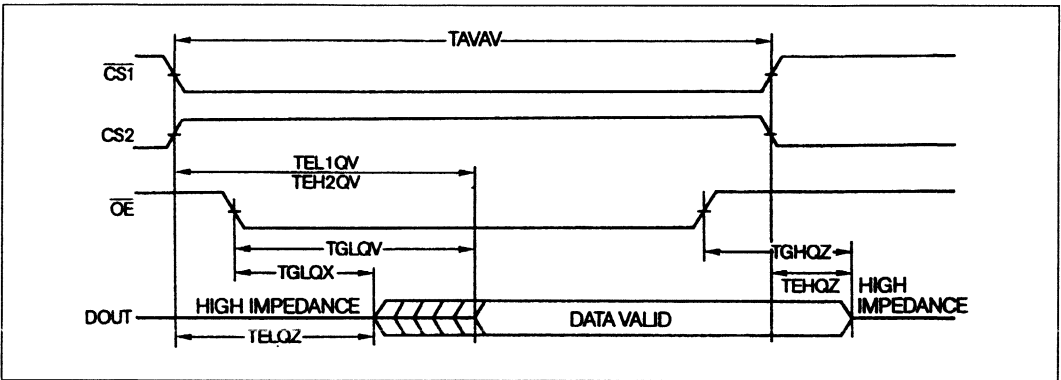
| SYMBOL | PARAMETER                       | 65664<br>Q-9 | 65664<br>B-9/2 | 65664<br>S-9/2 | 65664<br>-9/2 | 65664<br>C-9/2 | UNIT | VALUE |
|--------|---------------------------------|--------------|----------------|----------------|---------------|----------------|------|-------|
| TAVAV  | Read cycle time                 | 35           | 45             | 45             | 55            | 55             | ns   | min   |
| TAVQV  | Address saccess time            | 35           | 45             | 45             | 55            | 55             | ns   | max   |
| TAVQX  | Address valid to low Z          | 3            | 3              | 3              | 3             | 3              | ns   | min   |
| TEL1QV | Chip-select 1 access time       | 35           | 45             | 45             | 55            | 55             | ns   | max   |
| THL2QV | Chip-select 2 access time       | 35           | 45             | 45             | 55            | 55             | ns   | max   |
| TEL1QX | $\overline{CS1}$ low to low Z   | 5            | 5              | 5              | 5             | 5              | ns   | min   |
| TEH2QX | CS2 high to low Z               | 5            | 5              | 5              | 5             | 5              | ns   | min   |
| TEH1QZ | $\overline{CS1}$ high to high Z | 35           | 45             | 45             | 55            | 55             | ns   | max   |
| TEL2QZ | CS2 low to high Z               | 35           | 45             | 45             | 55            | 55             | ns   | max   |
| TGLQV  | Output Enable access time       | 15           | 15             | 15             | 20            | 20             | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z    | 5            | 5              | 5              | 5             | 5              | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z  | 15           | 15             | 15             | 20            | 20             | ns   | max   |



## READ CYCLE nb 1 (notes 16, 17)



## READ CYCLE nb 2 (notes 16, 18)



- Notes : 16.  $\overline{W}$  is high for read cycle  
 17. Device is continuously selected,  $\overline{CS1}$  &  $\overline{OE}$  = VIL and  $CS2$  = VIH  
 18. Address valid prior to or coincident with CS transition low.

## ORDERING INFORMATION

| Package                          | Device Type                      | Grade                                | Level                                        |
|----------------------------------|----------------------------------|--------------------------------------|----------------------------------------------|
| HM1                              | 65664                            | B                                    | -5                                           |
| 0 - Chip form                    | 8 k x 8 Ultimate CMOS static RAM |                                      |                                              |
| 1 - Ceramic 28 pins<br>300 mils  |                                  |                                      | - 5 : Commercial                             |
| 1E - Ceramic 28 pins<br>600 mils |                                  |                                      | - 9 : Industrial                             |
| 3 - Plastic 28 pins<br>300 mils  |                                  | B = high speed/low current           | - 2 : Military                               |
| 3E - Plastic 28 pins<br>600 mils |                                  | S = high speed/standard current      | - 8 : Military with B.I.<br>(B.I. = Burn-in) |
| 4 - LCC 32 pins                  |                                  | Blank : standard speed/low current   |                                              |
| T - SOIC 300 mils 28 pins        |                                  | C : standard                         |                                              |
| TI - SOIC 330 mils 28 pins       |                                  | Q = very high speed/standard current |                                              |
| U* - SOJ 28 pins                 |                                  |                                      |                                              |

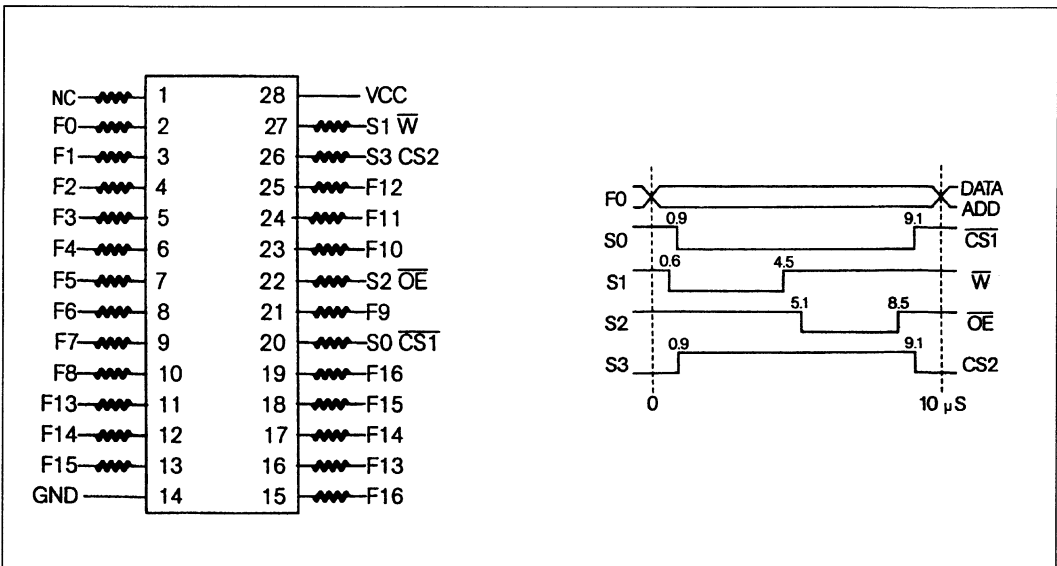
\* preliminary

## PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins  
 Plastic DIL, 600 mils, 28 pins  
 Ceramic DIL, 600 mils, 28 pins  
 SOIC DIL, 300 mils, 28 pins  
 LCC rectangular, 32 pins

## BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)  
 R = 1 KΩ per pin  
 Fo = 50 KHz ± 20 %

F<sub>n</sub> = 1/2 F<sub>n-1</sub>  
 S0 to S3 : programmable signals for write / read cycles  
 NC = Not connected



DATA SHEET

M 65697

256 k x 1  
ULTIMATE CMOS SRAM

MAIN FEATURES

3

- ACCESS TIME : 35/45/55 ns.
- VERY LOW POWER CONSUMPTION  
ACTIVE : 200 mW (TYP)  
STANDBY : 2.0  $\mu$ W (TYP)  
DATA RETENTION : 0.8  $\mu$ W (TYP)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN  
RESISTORS ARE REQUIRED

DESCRIPTION

The M 65697 is a very low power CMOS static RAM organized as 262144 x 1 bit. It is manufactured using the MHS high performance CMOS technology named SCMOS.

With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics, the portable instruments or embarked systems.

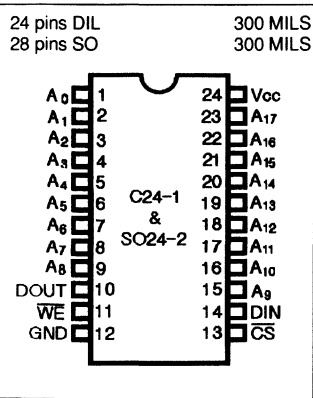
Utilizing an array of six transistors (6T) memory cells, the M 65697 combines an extremely low standby supply

current (Typical value = 0.5  $\mu$ A) with a fast access time at 45 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

The M 65697 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it deally suitable for military/space applications that demand superior levels of performance and reliability.

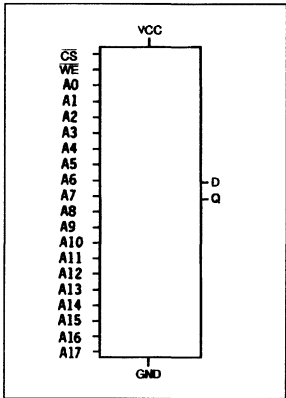
PACKAGES



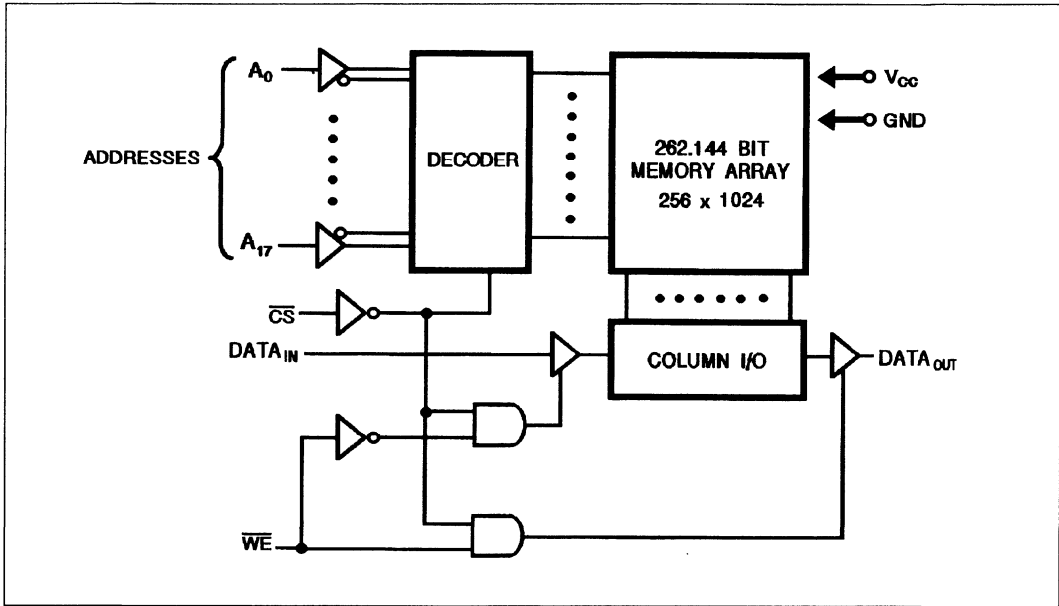
PIN NAMES

|                               |                               |
|-------------------------------|-------------------------------|
| A0-A17 : Address inputs       | $\overline{W}$ : Write enable |
| Din : Input                   | Vcc : Power                   |
| Dout : Output                 | GND : Ground                  |
| $\overline{CS}$ : Chip select |                               |

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                         |                                     |
|-------------------------|-------------------------------------|
| A0-A17 : Address inputs | $\overline{CS}$ (bar) : Chip-Select |
| D : Input               | $\overline{W}$ (bar) : Write Enable |
| Q : Output              |                                     |
| VCC : Power             |                                     |
| VSS : Ground            |                                     |

TRUTH TABLE

| $\overline{CS}$ (bar) | $\overline{W}$ (Bar) | DATA-IN | DATE-OUT | MODE                    |
|-----------------------|----------------------|---------|----------|-------------------------|
| H                     | X                    | Z       | Z        | Deselect/<br>Power-Down |
| L                     | H                    | Z       | Valid    | Read                    |
| L                     | L                    | Valid   | Z        | Write                   |

L = low, H = high, X = H or L, Z = high impedance.

### ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.3 V to + 7.0 V

Input or Output voltage applied : (Gnd - 0.3 V) to ( $V_{CC} + 0.3$  V)

Storage temperature : - 65°C to + 150°C

Electro static discharge voltage > 2000 V (MIL STD 883, METHOD 3015.2)

| OPERATING RANGE | OPERATING VOLTAGE                | OPERATING TEMPERATURE |
|-----------------|----------------------------------|-----------------------|
| Military        | $V_{CC} = 5 \text{ V} \pm 10 \%$ | 55°C to + 125°C       |
| Industrial      | $V_{CC} = 5 \text{ V} \pm 10 \%$ | 40°C to + 85°C        |
| Commercial      | $V_{CC} = 5 \text{ V} \pm 10 \%$ | 0°C to + 70°C         |

### ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STAD 883C FOR GROUP A ( Subgroups 1, 2, 3)

| PARAMETER  | DESCRIPTION                  | 65697 B |          | 65697 S |          | 65697 |          | 65697 C |          | UNIT | VALUE | NOTE 8 |
|------------|------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|--------|
|            |                              | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |        |
| ICCSB (1)  | Standby supply current       | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| ICCSB1 (2) | Standby supply current       | 1       | 50       | 100     | 500      | 1     | 50       | 100     | 500      | μA   | Max   | M      |
| ICCOP (3)  | Operating supply current     | 75      |          | 100     |          | 75    |          | 100     |          | mA   | Max   | M      |
| ICC (4)    | Operating supply current     | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| II/O (5)   | Input/Output leakage current | ± 1     |          | ± 1     |          | ± 1   |          | ± 1     |          | μA   | Max   | M      |
| VIL (6)    | Input low voltage            | 0.8     |          | 0.8     |          | 0.8   |          | 0.8     |          | V    | Max   | T      |
| VIH (6)    | Input high voltage           | 2.2     |          | 2.2     |          | 2.2   |          | 2.2     |          | V    | Min   | T      |
| VOL (7)    | Output low voltage           | 0.4     |          | 0.4     |          | 0.4   |          | 0.4     |          | V    | Max   | T      |
| VOH (7)    | Output high voltage          | 2.4     |          | 2.4     |          | 2.4   |          | 2.4     |          | V    | Min   | T      |
| CIN        | Input capacitance            | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |
| COUT       | Output capacitance           | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |

- Notes :
1.  $CS \geq V_{IH}$
  2.  $CS \geq V_{CC} - 0.3 \text{ V}$ , Output current = 0 mA
  3.  $V_{CC}$  max,  $I_{out} = 0 \text{ mA}$ , Duty cycle 100 % F = max,  $V_{in} = V_{CC} / \text{Gnd}$
  4.  $CS \leq V_{IL}$ ,  $I_{out} = 0 \text{ mA}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  5.  $V_{CC} = 5.5 \text{ V}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  6.  $V_{IH}$  max =  $V_{CC} + 0.3 \text{ V}$ ,  $V_{IL}$  min = - 0.3 V or - 1 V pulse width 50 ns.
  7.  $V_{CC}$  min,  $I_{OL} = 4 \text{ mA}$ ,  $I_{OH} = - 1 \text{ mA}$ .
  8. Including open/short test or inputs clamp voltage.
- G - Guaranteed - Not tested : Parameter measured at design validation and at any design change.  
M - Measured : Parameter measured and data-log capability.  
T - Tested : Parameter verification during testing.

DATA RETENTION MODE

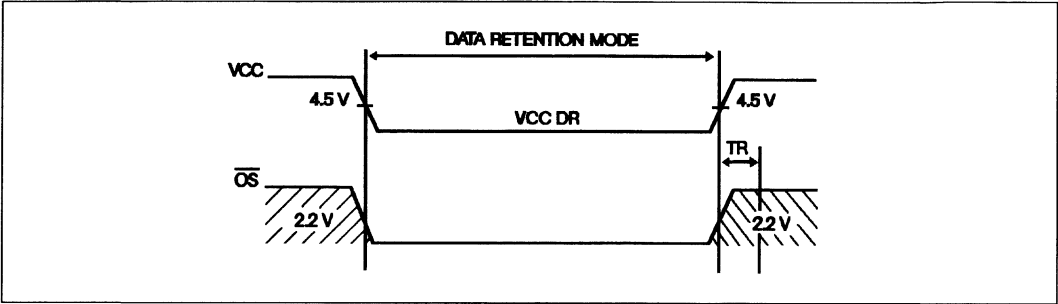
MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during date retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.

2.  $\overline{CS}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions.

3. The RAM can begin operation > 45 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

| PARAMETER   | DESCRIPTION                                                 | MINIMUM    | TYPICAL (9) | MAXIMUM |          | UNIT    | NOTE 8 |
|-------------|-------------------------------------------------------------|------------|-------------|---------|----------|---------|--------|
| VCCDR       | $V_{CC}$ for data retention                                 | 2.0        | –           | –       |          | V       | T      |
| TCDR        | Chip deselect to data retention time                        | 0.0        | –           | –       |          | ns      |        |
| TR          | Operation recovery time                                     | TAVAV (10) | –           | –       |          | ns      |        |
| ICCDR1 (11) | Data retention current @ 2.0 V : M-65697 B/-<br>M-65697 S/C | –          | 0.1         | COM     | IND, MIL | $\mu$ A | M      |
|             |                                                             |            |             | 1       | 20.0     |         |        |
| ICCDR2 (11) | Data retention current @ 3.0 V : M-65697 B/-<br>M-65697 S/C | –          | 0.3         | 20      | 200.0    | $\mu$ A | M      |
|             |                                                             |            |             | 1       | 30.0     |         |        |
|             |                                                             | –          | 0.3         | 30      | 300.0    | $\mu$ A | G      |
|             |                                                             |            |             |         |          |         |        |

Note : 9.  $T_A = 25^{\circ}\text{C}$ .  
10. TAVAV = Read cycle time.  
11.  $\overline{CS} = V_{CC}$ ,  $V_{in} = \text{Gnd}/V_{CC}$ , this parameter is only tested to  $V_{CC} = 2$  V.

# ELECTRICAL CHARACTERISTICS

## AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 4, 5, 6, 9, 10, 11)

### AC CONDITIONS :

|                               |                |                         |                                     |
|-------------------------------|----------------|-------------------------|-------------------------------------|
| Input pulse levels            | : Gnd to 3.0 V | Output load             | : 1 TTL gate + 30 pF see figure 1a/ |
| Input rise                    | : 5 ns         | Operating temperature : | 55°C to + 125°C (Military)          |
| V <sub>CC</sub>               | : 5 V ± 10 %   |                         | - 40°C to + 85°C (Industrial)       |
| Input timing reference levels | : 1.5 V        |                         | 0°C to + 70°C (Commercial)          |

### WRITE CYCLE

| SYMBOL     | PARAMETER *                      | 65697 B |          | 65697 S |          | 65697 |          | 65697 C |          | UNIT | VALUE |
|------------|----------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|            |                                  | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV      | Write cycle time                 | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVWL      | Address set-up time              | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TAVWH      | Address valid to end of write    | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TDVWH      | Data set-up time                 | 20      | 20       | 20      | 20       | 25    | 25       | 25      | 25       | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 10      | 15       | 10      | 15       | 15    | 20       | 15      | 20       | ns   | max   |
| TWLWH      | Write pulse width                | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWHAX      | Address hold to end of write     | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHDX      | Data hold time                   | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |

**Note** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.  
All parameters only tested and screened during full speed functional test.  
For subgroups 7 and 8, functional test is performed at 1 MHz with V<sub>IL</sub> = 0V and V<sub>IH</sub> = 3 V.

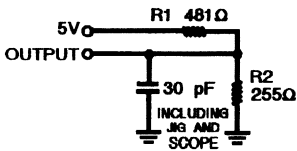


Fig. 1a : Output Load.

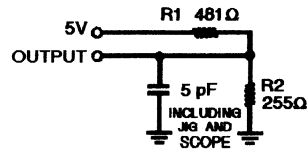


Fig. 1B : Output Load for : TELQX  
TGLQX  
TGHQZ  
TWLQZ  
TWHQX  
TEHQZ

Equivalent to : THEVENIN EQUIVALENT

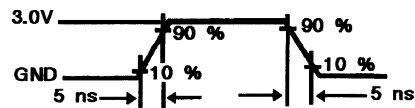
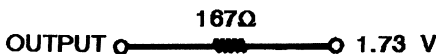


Figure 2 : All input pulses.

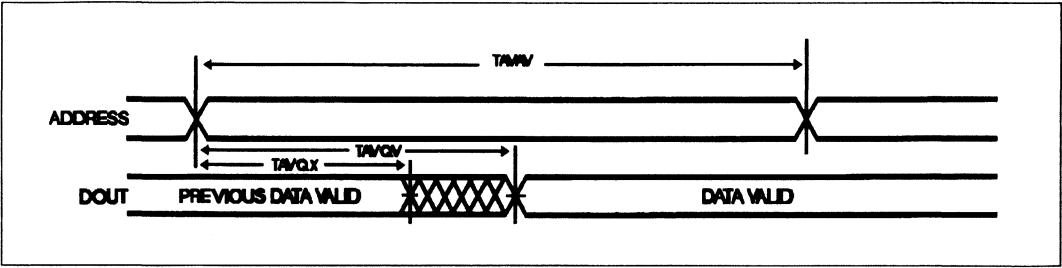




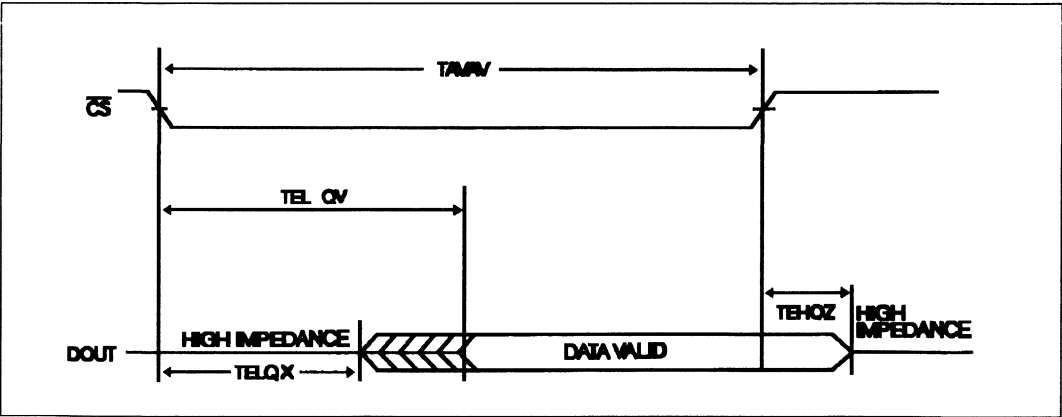
READ CYCLE

| SYMBOL | PARAMETER *                           | 65697 B |          | 65697 S |          | 65697 |          | 65697 C |          | UNIT | VALUE |
|--------|---------------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|        |                                       | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV  | Write cycle time                      | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVQV  | Address access time                   | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TAVQX  | Address valid to low Z                | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TELQV  | Chip-select access time               | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TELQX  | $\overline{\text{CS}}$ low to low Z   | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TEHQZ  | $\overline{\text{CS}}$ high to high Z | 30      | 40       | 30      | 40       | 40    | 40       | 40      | 40       | ns   | max   |

READ CYCLE nb 1 (notes 14, 15)



READ CYCLE nb 2 (notes 14, 16)



Notes : 14. W is high for read cycle.  
15. Device is continuously selected  $\overline{\text{CS}} = \text{VIL}$ .  
16. Address valid prior to or coincident with  $\overline{\text{CS}}$  transitive low.

| TEMPERATURE RANGE                                                                                                              | PACKAGE                                                                                                                     | DEVICE                 | GRADE                               | SPEED                   | FLOW                                                                                                                                                                                                                                                                                                              |
|--------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------|-------------------------------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IM                                                                                                                             | CZ                                                                                                                          | - 65697                | V                                   | - 45                    | MB                                                                                                                                                                                                                                                                                                                |
| C = COMMERCIAL 0° to + 70°C<br>I = INDUSTRIAL - 40° to + 85°C<br>M = MILITARY - 55° to + 125°C<br>S = SPATIAL - 55° to + 125°C | CZ = 24 pins DIL SIDE-BRAZED 300 mils<br>NP = 28 pins SO L CERAMIC 300 mils<br>3 = 24 pins DIP 300 mils<br>T = 28 pins SOIC | 256K x 1<br>STATIC RAM | V = Very low power<br>L = Low power | 35 ns<br>45 ns<br>55 ns | blank = No special flow<br>- 8 = MHS MILITARY PROGRAM<br>MB = MIL-STD 883C CLASS B<br>CB = COMPLIANT CECC 90000 LEVEL B<br>SHXXX = SPECIAL CUSTOMER REQUEST<br>FHXXX = FLIGHT MODELS (SPATIAL)<br>EHXXX = ENGINEERING MODELS (SPATIAL)<br>MHXXX = MECHANICAL PARTS (SPATIAL)<br>LHXXX = LIFE TEST PARTS (SPATIAL) |

## DATA SHEET

## M 65698

# 64 k x 4 HIGH SPEED CMOS SRAM

## MAIN FEATURES

- ACCESS TIME : 35/45/55 ns
- VERY LOW POWER CONSUMPTION
  - ACTIVE : 200 mW (typ)
  - STANDBY : 2.0 W (typ)
  - DATA RETENTION : 0.8 W (typ)
- WIDE TEMPERATURE RANGE : - 55° TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

## DESCRIPTION

The M 65698 is a very lower power CMOS static RAM organized as 65536 x 4 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.

With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics, the portable instruments or embarked systems.

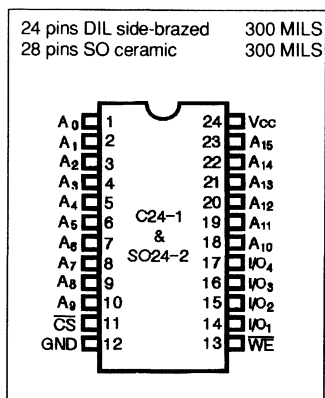
Utilizing an array of six transistors (6T) memory cells, the M 65698 combines an extremely low standby supply

current (typical value = 0.5 A) with a fast access time at 45 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

The M 65698 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

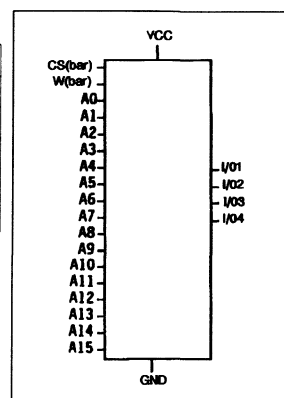
## PACKAGES



## PIN NAMES

|           |                   |
|-----------|-------------------|
| A0-A15    | Addresses         |
| I/O1-I/O4 | Data Input/Output |
| CS        | Chip select       |
| WE        | Write Enable      |
| GND       | Ground            |
| Vcc       | Power             |

## LOGIC SYMBOL



The block diagram illustrates the internal architecture of the 282144-bit memory array. It features a central **282,144-BIT MEMORY ARRAY** block, which is a **256 x 128 x 8** array. This array is connected to a **DECODER** block, which receives **ADDRESSES** (A<sub>0</sub> to A<sub>15</sub>) and outputs to the memory array. The memory array is also connected to an **INPUT DATA CONTROL** block, which receives **I/O** signals (I/O<sub>2</sub> to I/O<sub>4</sub>) and outputs to the memory array. The memory array is connected to a **COLUMN I/O** block, which outputs to the memory array. The memory array is also connected to a **CS** (Chip Select) and **WE** (Write Enable) block, which receives **CS** and **WE** signals. The memory array is connected to **Vcc** and **GND** power pins. The memory array is connected to a **DATA** bus, which is connected to the **DATA** pins of the package.

|                          |                                     |
|--------------------------|-------------------------------------|
| A0-A15 : Address inputs  | $\overline{CS}$ (bar) : Chip-Select |
| I/O1-I/O4 : Input/Output | $\overline{W}$ (bar) : Write Enable |
| V <sub>SS</sub> : Ground |                                     |
| VCC : Power              |                                     |

| $\overline{\text{CS}}$ (bar) | $\overline{\text{W}}$ (bar) | INPUTS/OUTPUTS | MODE                    |
|------------------------------|-----------------------------|----------------|-------------------------|
| H                            | X                           | Z              | Deselect/<br>POWER-DOWN |
| L                            | H                           | DATA OUT       | Read                    |
| L                            | L                           | DATA IN        | Write                   |

L = low, H = high, X = H or L, Z = high impedance.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V

Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)

Storage Temperature : - 65°C to + 150°C

Electro static discharge voltage > 2000 V (MIL STD 883, METHOD 3015.2)

| OPERATING RANGE | OPERATING VOLTAGE              | OPERATING TEMPERATURE |
|-----------------|--------------------------------|-----------------------|
| Military        | $V_{CC} = 5\text{ V} \pm 10\%$ | - 55°C to + 125°C     |
| Industrial      | $V_{CC} = 5\text{ V} \pm 10\%$ | - 40°C to +           |
| Commercial      | $V_{CC} = 5\text{ V} \pm 10\%$ | 0°C to 70°C           |

## ELECTRICAL CHARACTERISTICS

### DC PARAMETERS : COMMERCIAL, INDUSTRIAL AND MILITARY

| PARAMETER  | DESCRIPTION                  | 65698 B |          | 65698 S |          | 65698 |          | 65698 C |          | UNIT | VALUE | NOTE 8 |
|------------|------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|--------|
|            |                              | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |        |
| ICCSB (1)  | Standby supply current       | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| ICCSB1 (2) | Standby supply current       | 1       | 50       | 100     | 500      | 1     | 50       | 100     | 500      | μA   | Max   | M      |
| ICCOP (3)  | Operating supply current     | 75      |          | 100     |          | 75    |          | 100     |          | mA   | Max   | M      |
| ICC (4)    | Operating supply current     | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| II/O (5)   | Input/Output leakage current | ± 1     |          | ± 1     |          | ± 1   |          | ± 1     |          | μA   | Max   | M      |
| VIL (6)    | Input low voltage            | 0.8     |          | 0.8     |          | 0.8   |          | 0.8     |          | V    | Max   | T      |
| VIH (6)    | Input high voltage           | 2.2     |          | 2.2     |          | 2.2   |          | 2.2     |          | V    | Min   | T      |
| VOL (7)    | Output low voltage           | 0.4     |          | 0.4     |          | 0.4   |          | 0.4     |          | V    | Max   | T      |
| VOH (7)    | Output high voltage          | 2.4     |          | 2.4     |          | 2.4   |          | 2.4     |          | V    | Min   | T      |
| C IN       | Input capacitance            | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |
| C OUT      | Output capacitance           | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |

- Notes :**
1.  $\overline{CS} > V_{IH}$
  2.  $\overline{CS} > V_{CC} - 0.3\text{ V}$ , Output current = 0 mA
  3.  $V_{CC}$  max,  $I_{out} = 0\text{ mA}$ , Duty cycle 100 % F = max,  $V_{in} = V_{CC} / \text{Gnd}$
  4.  $\overline{CS} < V_{IL}$ ,  $I_{out} = 0\text{ mA}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  5.  $V_{CC} = 5.5\text{ V}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  6.  $V_{IH}$  max =  $V_{CC} + 0.3\text{ V}$ ,  $V_{IL}$  min = - 0.3 V or - 1 V pulse width 50 ns.
  7.  $V_{CC}$  min,  $I_{OL} = 4\text{ mA}$ ,  $I_{OH} = - 1\text{ mA}$ .
  8. Including open/short test or inputs clamp voltage.  
 G - Guaranteed - Not tested : Parameter measured at design validation and at any design change.  
 M - Measured : Parameter measured and data-log capability.  
 T - Tested : Parameter verification during testing.

3

.DATA RETENTION MODE

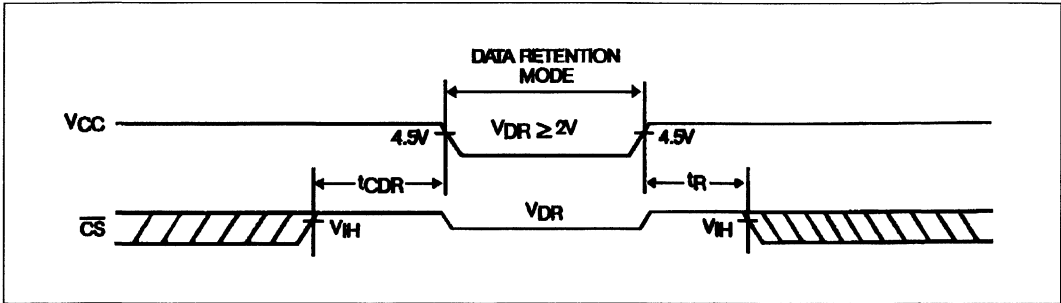
MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{cc}$  to  $V_{cc} + 0.3$  V.

2.  $\overline{CS}$  must be kept between  $V_{cc} + 0.3$  V and 70 % of  $V_{cc}$  during the power up and power down transitions.

3. The RAM can begin operation > 45 ns after  $V_{cc}$  reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

| PARAMETER   | DESCRIPTION                                                      | MINIMUM       | TYPICAL<br>(9) | MAXIMUM |               | UNIT | NOTE 8 |
|-------------|------------------------------------------------------------------|---------------|----------------|---------|---------------|------|--------|
| VCCDR       | Vcc for data retention                                           | 2.0           | —              | —       |               | V    | T      |
| TCDR        | Chip deselect to data retention time                             | 0.0           | —              | —       |               | ns   |        |
| TR          | Operation recovery time                                          | TAVAV<br>(10) | —              | —       |               | ns   |        |
| ICCDR1 (10) | Data retention current<br>@ 2.0 V : HM-65698 B/-<br>HM-65698 S/C | —             | 0.1            | COM     | IND, MIL      | μA   | M      |
|             |                                                                  | —             | 0.1            | 1<br>30 | 20.0<br>200.0 | μA   | M      |
| ICCDR2 (11) | Data retention current<br>@ 3.0 V : HM-65698 B/-<br>HM-65698 S/C | —             | 0.3            | 1       | 30.0          | μA   | G      |
|             |                                                                  | —             | 0.3            | 50      | 300.0         | μA   | G      |

Notes : 9. TA = 25°C.  
10. TAVAV = Read cycle time.  
11. CS = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS

AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 4, 5, 6, 9, 10, 11)

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
Input rise : 5 ns  
VCC : 5 V  $\pm$  10 %  
Input timing reference levels : 1.5 V

Output load : 1 TTL gate + 30 pF (see figures 1a/1b)  
OPERATING TEMPERATURE : -55°C to +125°C (Military)  
- 40°C to + 85°C (industrial)  
0°C to + 70°C (Commercial)

WRITE CYCLE

| SYMBOL     | PARAMETER                     | 65698 B |          | 65698 S |          | 65698 |          | 65698 C |          | UNIT | VALUE |
|------------|-------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|            |                               | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV      | Write cycle time              | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVWL      | Address set-up time           | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TAVWH      | Address valid to end of write | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TDVWH      | Data set-up time              | 20      | 20       | 20      | 20       | 25    | 25       | 25      | 25       | ns   | min   |
| TELWH      | CS low to write end           | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWLQZ (12) | Write low to high Z           | 10      | 15       | 10      | 15       | 15    | 20       | 15      | 20       | ns   | max   |
| TWLWH      | Write pulse width             | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWHAX      | Address hold to end of write  | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHDX      | Data hold time                | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHQX (12) | Write high to low Z           | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

\* All parameters only tested and screened during full speed functional test.

For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = 0 V and VIH = 3 V.

3

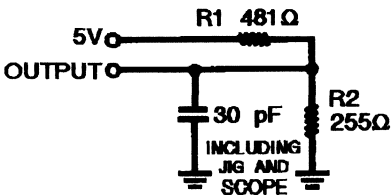


Fig. 1a : Output Load.

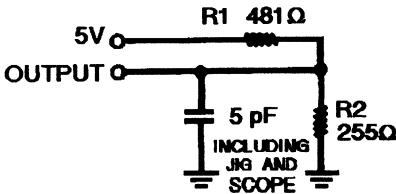


Fig. 1B : Output Load for : TELQX  
TGLQX  
TGHQZ  
TWLQZ  
TWHQX  
TEHQZ

Equivalent to : THEVENIN EQUIVALENT

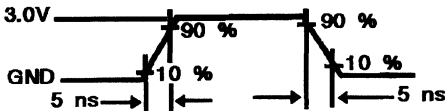
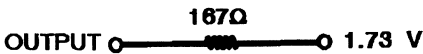
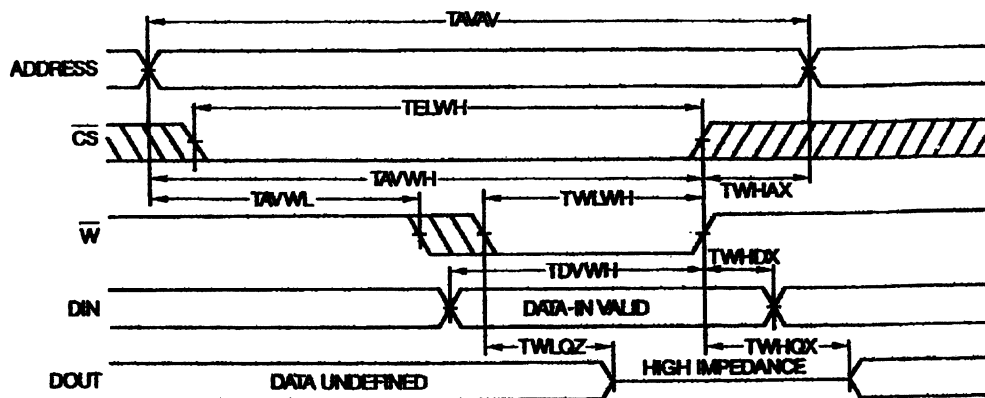
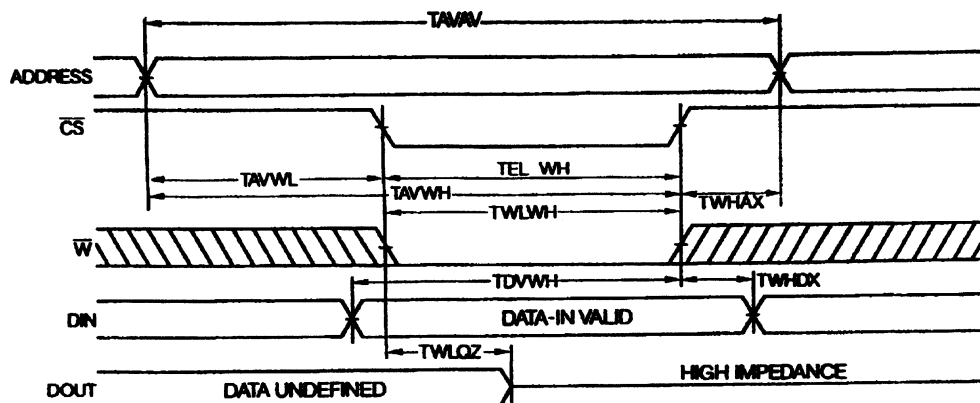


Figure 2 : All input pulses.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 13)WRITE CYCLE 2  $\overline{CS}$  CONTROLLED (note 13)

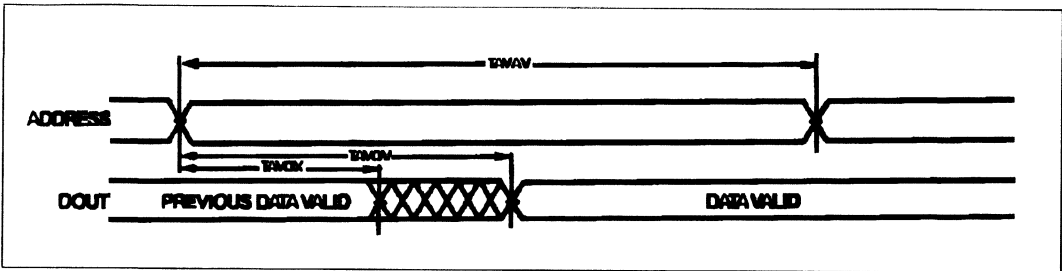
**Note :** 13. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.



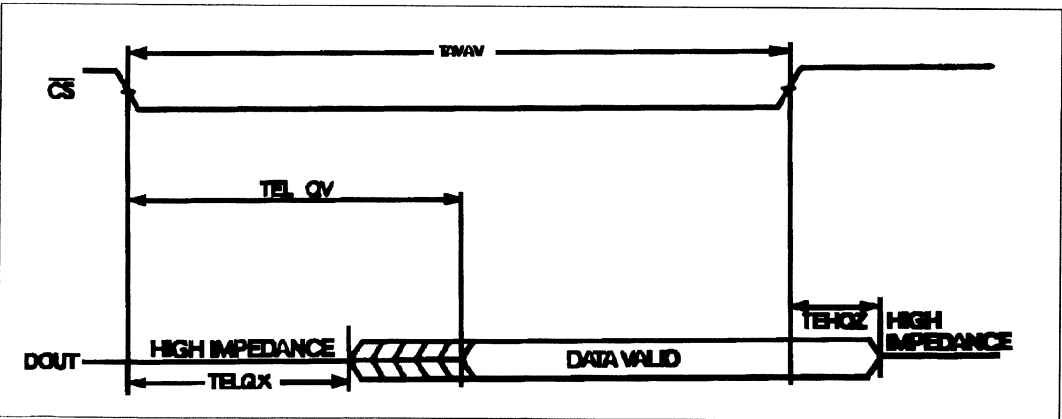
### READ CYCLE

| SYMBOL | PARAMETER *                    | 65698 B |          | 65698 S |          | 65698 |          | 65698 C |          | UNIT | VALUE |
|--------|--------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|        |                                | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV  | Read cycle time                | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVQV  | Address access time            | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TAVQX  | Address valid to low Z         | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TELQV  | Chip-select access time        | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TTEHQZ | $\overline{CS}$ high to high Z | 30      | 40       | 30      | 40       | 40    | 40       | 40      | 40       | ns   | max   |

#### READ CYCLE nb 1 (notes 14, 15)



#### READ CYCLE nb 2 (notes 14, 16)



- Notes :
- 14.  $\overline{W}$  is high for read cycle.
  - 15. Device is continuously selected  $\overline{CS} = V_{IL}$ .
  - 16. Address valid prior to or coincident with  $\overline{CS}$  transitive low.

| TEMPERATURE RANGE              | PACKAGE                               | DEVICE     | GRADE              | SPEED | FLOW                                 |
|--------------------------------|---------------------------------------|------------|--------------------|-------|--------------------------------------|
| IM                             | CZ                                    | – 65698    | V                  | – 45  | MB                                   |
| C = COMMERCIAL 0° to + 70°C    |                                       | 64K x 4    |                    | 35 ns |                                      |
| I = INDUSTRIAL – 40° to + 85°C |                                       | STATIC RAM |                    | 45 ns |                                      |
| M = MILITARY – 55° to + 125°C  |                                       |            | V = Very low power | 55 ns |                                      |
| S = SPATIAL – 55° to + 125°C   |                                       |            |                    |       |                                      |
|                                | CZ = 24 pins DIL SIDE-BRAZED 300 mils |            |                    |       |                                      |
|                                | NP = 28 pins SO L CERAMIC 300 mils    |            |                    |       |                                      |
|                                | 3 = 24 pins DIP 300 mils              |            |                    |       |                                      |
|                                | T = 28 pins SOIC 300 mils             |            |                    |       |                                      |
|                                |                                       |            |                    |       | blank = No special flow              |
|                                |                                       |            |                    |       | – 8 = MHS MILITARY PROGRAM           |
|                                |                                       |            |                    |       | MB = MIL-STD 883C CLASS B            |
|                                |                                       |            |                    |       | CB = COMPLIANT CECC 90000 LEVEL B    |
|                                |                                       |            |                    |       | SHXXX = SPECIAL CUSTOMER REQUEST     |
|                                |                                       |            |                    |       | FHXXX = FLIGHT MODELS (SPATIAL)      |
|                                |                                       |            |                    |       | EHXXX = ENGINEERING MODELS (SPATIAL) |
|                                |                                       |            |                    |       | MHXXX = MECHANICAL PARTS (SPATIAL)   |
|                                |                                       |            |                    |       | LHXXX = LIFE TEST PARTS (SPATIAL)    |

3

## DATA SHEET

## M 65656

# 32 k x 8

## ULTIMATE CMOS SRAM

## MAIN FEATURES

- ACCESS TIME : 35/45/55 ns
- VERY LOW POWER CONSUMPTION
  - ACTIVE : 200 mW (typ)
  - STANDBY : 2.0  $\mu$ W (typ)
  - DATA RETENTION : 0.8  $\mu$ W (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 AND 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

## DESCRIPTION

The M 65656 is a very lower power CMOS static RAM organized as 32768 x 8 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.

With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics, or the portable instruments or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M 65656 combines an extremely low standby supply current (Typical value = 0.5  $\mu$ A) with a fast access

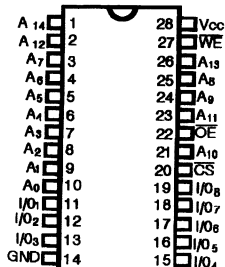
time at 45 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

The M 65656 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

## PACKAGES

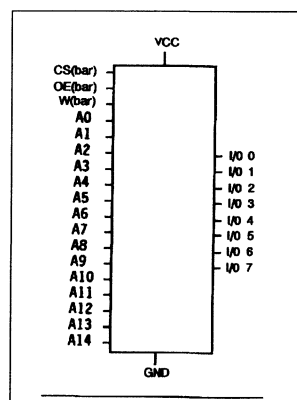
28 pins DIL ceramic 600 MILS  
28 pins DIL 600 MILS/300 MILS  
28 pins SO 300 MILS



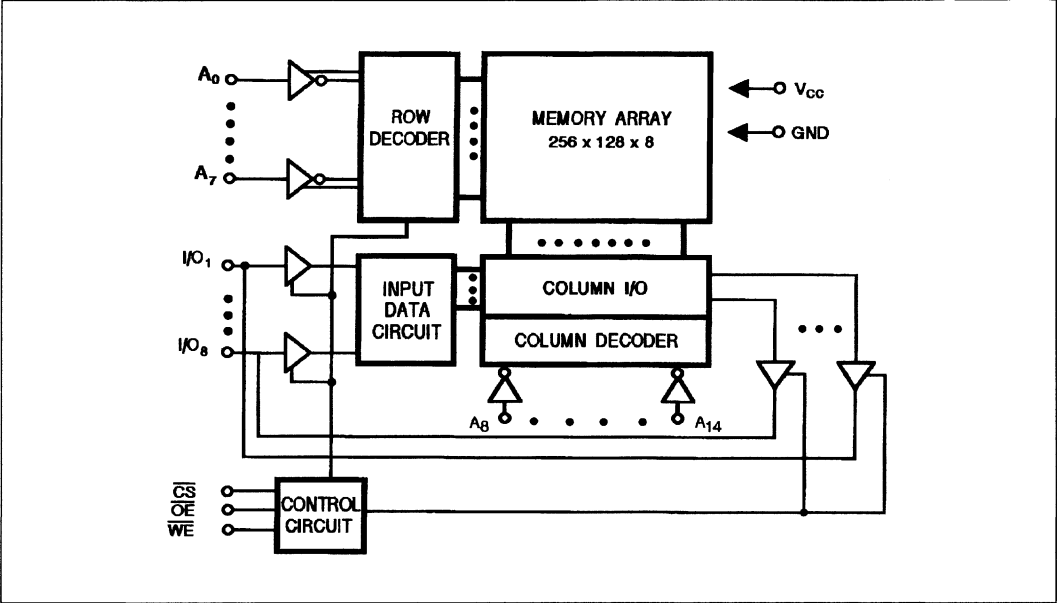
## PIN NAMES

|                                    |                   |
|------------------------------------|-------------------|
| A <sub>0</sub> -A <sub>14</sub>    | Addresses         |
| I/O <sub>0</sub> -I/O <sub>7</sub> | Data Input/Output |
| $\overline{CS}$                    | Chip select       |
| $\overline{WE}$                    | Write Enable      |
| $\overline{OE}$                    | Output Enable     |
| GND                                | Ground            |
| Vcc                                | Power             |

## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                          |                                              |
|--------------------------|----------------------------------------------|
| A0-A14 : Address inputs  | $\overline{\text{CS}}$ (bar) : Chip-Select   |
| I/O0-I/O7 : Input/Output | $\overline{\text{W}}$ (bar) : Write Enable   |
| Vcc : Power              | $\overline{\text{OE}}$ (bar) : Output Enable |
| VSS : Ground             |                                              |

TRUTH TABLE

| $\overline{\text{CS}}$ (bar) | $\overline{\text{W}}$ (bar) | $\overline{\text{OE}}$ (bar) | INPUTS/<br>OUTPUTS | MODE                        |
|------------------------------|-----------------------------|------------------------------|--------------------|-----------------------------|
| H                            | X                           | X                            | Z                  | Deselect/<br>POWER-<br>DOWN |
| L                            | H                           | H                            | DATA<br>OUT        | Read                        |
| L                            | L                           | L                            | DATA IN            | Write                       |
| L                            | H                           | H                            | Z                  | Output<br>Disable           |

L = low, H = high, X = H or L, Z = high impedance.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V

Input or Output voltage applied : (Gnd - 0.3 V) to ( $V_{CC} + 0.3$  V)

Storage Temperature : - 65°C to + 150°C

Electro static discharge voltage > 2000 V (MIL STD 883, METHOD 3015.2)

| OPERATING RANGE | OPERATING VOLTAGE                | OPERATING TEMPERATURE |
|-----------------|----------------------------------|-----------------------|
| Military        | $V_{CC} = 5 \text{ V} \pm 10 \%$ | - 55°C to + 125°C     |
| Industrial      | $V_{CC} = 5 \text{ V} \pm 10 \%$ | - 40°C to + 85°C      |
| Commercial      | $V_{CC} = 5 \text{ V} \pm 10 \%$ | 0°C to 70°C           |

## ELECTRICAL CHARACTERISTICS

### DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3)

| PARAMETER  | DESCRIPTION                  | 65656 B |          | 65656 S |          | 65656 |          | 65656 C |          | UNIT | VALUE | NOTE 8 |
|------------|------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|--------|
|            |                              | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |        |
| ICCSB (1)  | Standby supply current       | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| ICCSB1 (2) | Standby supply current       | 1       | 50       | 100     | 500      | 1     | 50       | 100     | 500      | μA   | Max   | M      |
| ICCOP (3)  | Operating supply current     | 75      | 75       | 100     | 100      | 75    | 75       | 100     | 100      | mA   | Max   | M      |
| ICC (4)    | Operating supply current     | 10      | 15       | 15      | 20       | 10    | 15       | 15      | 20       | mA   | Max   | M      |
| II/O (5)   | Input/output leakage current | ± 1     |          | ± 1     |          | ± 1   |          | ± 1     |          | μA   | Max   | M      |
| VIL (6)    | Input low voltage            | 0.8     |          | 0.8     |          | 0.8   |          | 0.8     |          | V    | Max   | T      |
| VIH (6)    | Input high voltage           | 2.2     |          | 2.2     |          | 2.2   |          | 2.2     |          | V    | Min   | T      |
| VOL (7)    | Output low voltage           | 0.4     |          | 0.4     |          | 0.4   |          | 0.4     |          | V    | Max   | T      |
| VOH (7)    | Output high voltage          | 2.4     |          | 2.4     |          | 2.4   |          | 2.4     |          | V    | min   | T      |
| C IN       | Input capacitance            | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |
| C OUT      | Output capacitance           | 8       |          | 8       |          | 8     |          | 8       |          | pF   | Max   | G      |

- Notes :
1.  $\overline{CS} > = V_{IH}$
  2.  $\overline{CS} > = V_{CC} - 0.3 \text{ V}$ , Output current = 0 mA
  3.  $V_{CC}$  max,  $I_{out} = 0 \text{ mA}$ , Duty cycle 100 %  $F = \text{max}$ ,  $V_{in} = V_{CC} / \text{Gnd}$
  4.  $\overline{CS} < = V_{IL}$ ,  $I_{out} = 0 \text{ mA}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  5.  $V_{CC} = 5.5 \text{ V}$ ,  $V_{in} = \text{Gnd to } V_{CC}$
  6.  $V_{IH} \text{ max} = V_{CC} + 0.3 \text{ V}$ ,  $V_{IL} \text{ min} = -0.3 \text{ V}$  or  $-1 \text{ V}$  pulse width 50 ns.
  7.  $V_{CC} \text{ min}$ ,  $I_{OL} = 8 \text{ mA}$ ,  $I_{OH} = -4 \text{ mA}$ .
  8. Including open/short test or inputs clamp voltage.
- G - Guaranteed - Not tested : Parameter measured at design validation and at any design change.  
M - Measured : Parameter measured and data-log capability.  
T - Tested : Parameter verification during testing.

### DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

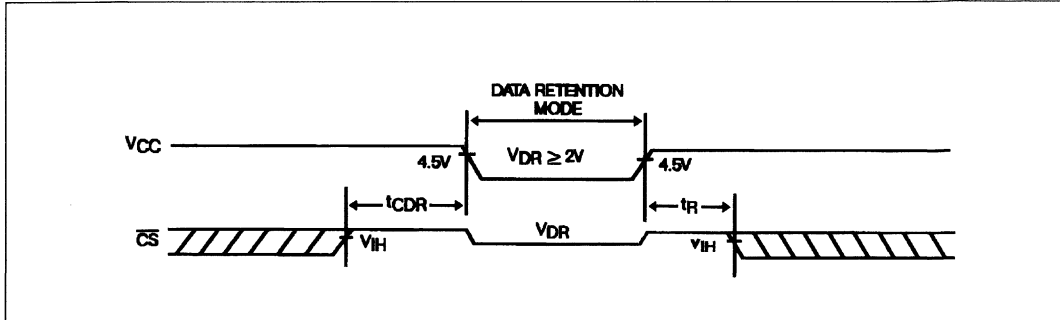
1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the

RAM outputs high impedance, minimizing power dissipation.

3.  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions.

4. The RAM can begin operation > 45 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

### TIMING



### DATA RETENTION CHARACTERISTICS

| PARAMETER   | DESCRIPTION                                                      | MINIMUM       | TYPICAL<br>(9) | MAXIMUM |          | UNIT | NOTE 8 |
|-------------|------------------------------------------------------------------|---------------|----------------|---------|----------|------|--------|
| VCCDR       | V <sub>CC</sub> for data retention                               | 2.0           | —              | —       |          | V    | T      |
| TCDR        | Chip deselect to data retention time                             | 0.0           | —              | —       |          | ns   |        |
| TR          | Operation recovery time                                          | TAVAV<br>(10) | —              | —       |          | ns   |        |
| ICCDR1 (11) | Data retention current<br>@ 2.0 V : HM-65656 B/-<br>HM-65656 S/C | —             | 0.1            | COM     | IND, MIL | μA   | M      |
|             |                                                                  |               |                | 1       | 20.0     |      |        |
|             |                                                                  |               |                | 30      | 200.0    |      |        |
| ICCDR2 (11) | Data retention current<br>@ 3.0 V : HM-65656 B/-<br>HM-65656 S/C | —             | 0.3            | 1       | 30.0     | μA   | G      |
|             |                                                                  |               |                | 50      | 300.0    |      |        |
|             |                                                                  |               |                |         |          |      |        |

Notes : 9. TA = 25°C.

10. TAVAV = Read cycle time.

11.  $\overline{CS}$  = V<sub>CC</sub>, Vin = Gnd/V<sub>CC</sub>, this parameter is only tested to V<sub>CC</sub> = 2 V.

# ELECTRICAL CHARACTERISTICS

## AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 4, 5, 6, 9, 10, 11)

### AC CONDITIONS :

|                               |                |                                                       |
|-------------------------------|----------------|-------------------------------------------------------|
| Input pulse levels            | : Gnd to 3.0 V | Output load : 1 TTL gate + 30 pF (see figures 1a/1b)  |
| Input rise                    | : 5 ns         | Operating temperature : - 55 °C to + 125°C (Military) |
| VCC                           | : 5 V ± 10 %   | - 40°C to + 85°C (industrial)                         |
| Input timing reference levels | : 1.5 V        | 0°C to + 70°C (Commercial)                            |

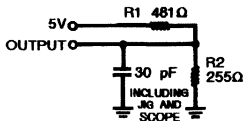
### WRITE CYCLE

| SYMBOL     | PARAMETER                        | 65656 B |          | 65656 S |          | 65656 |          | 65656 C |          | UNIT | VALUE |
|------------|----------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|            |                                  | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV      | Write cycle time                 | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVWL      | Address set-up time              | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TAVWH      | Address valid to end of write    | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TDVWH      | Data set-up time                 | 20      | 20       | 20      | 20       | 25    | 25       | 25      | 25       | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 10      | 15       | 10      | 15       | 15    | 20       | 15      | 20       | ns   | max   |
| TWLWH      | Write pulse width                | 30      | 40       | 30      | 40       | 40    | 50       | 40      | 50       | ns   | min   |
| TWHAX      | Address hold to end of write     | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHDX      | Data hold time                   | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0       | 0        | 0       | 0        | 0     | 0        | 0       | 0        | ns   | min   |

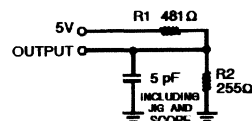
**Note :** 12 The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

\* : All parameters only tested and screened during full speed functional test.

For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = 0 V and VIH = 3 V.



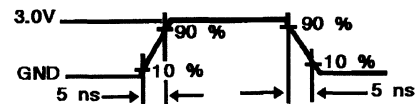
**Fig. 1a :** Output Load.



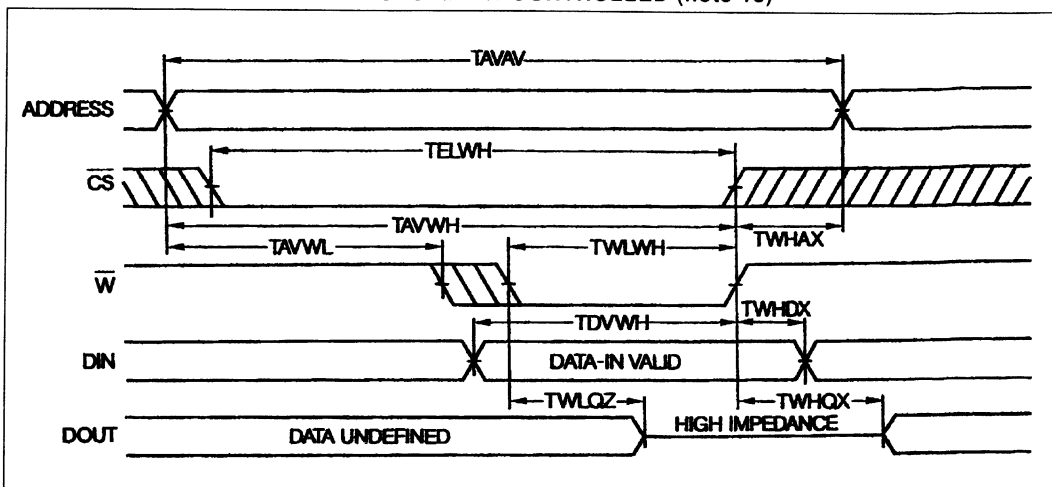
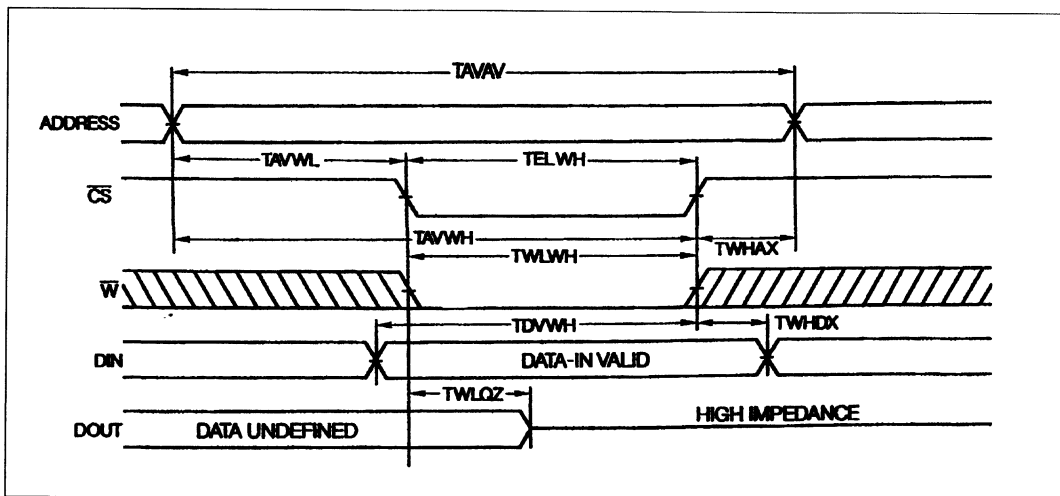
**Fig. 1B :** Output Load for :

TELQX  
TGLQX  
TGHQZ  
TWLQZ  
TWHQX  
TEHQZ

Equivalent to : THEVENIN EQUIVALENT



**Figure 2 :** All input pulses.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 13)WRITE CYCLE 2  $\overline{CS}$  CONTROLLED (note 13)

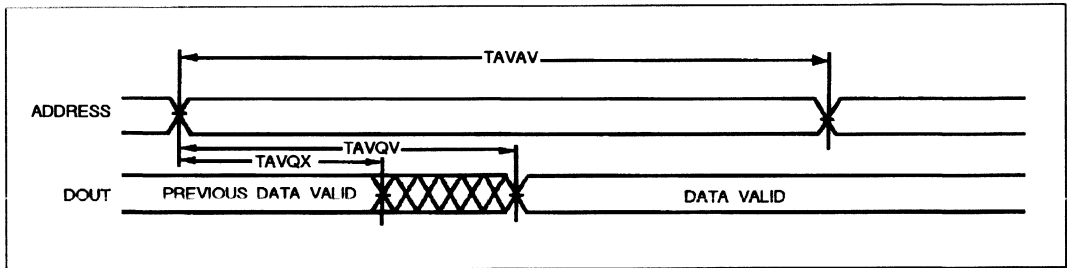
**Note : 13.** The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
Data out is high impedance if  $\overline{OE} = V_{IH}$ .



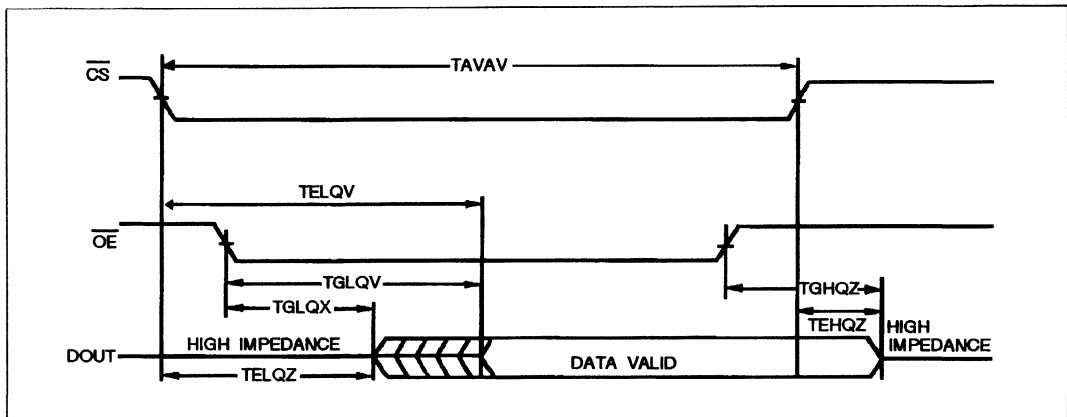
READ CYCLE

| SYMBOL | PARAMETER *                           | 65656 B |          | 65656 S |          | 65656 |          | 65656 C |          | UNIT | VALUE |
|--------|---------------------------------------|---------|----------|---------|----------|-------|----------|---------|----------|------|-------|
|        |                                       | COM     | IND, MIL | COM     | IND, MIL | COM   | IND, MIL | COM     | IND, MIL |      |       |
| TAVAV  | Read cycle time                       | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | min   |
| TAVQV  | Address access time                   | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TAVQX  | Address valid to low Z                | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TELQV  | Chip-select access time               | 35      | 45       | 35      | 45       | 45    | 55       | 45      | 55       | ns   | max   |
| TELQX  | $\overline{\text{CS}}$ low to low Z   | 3       | 3        | 3       | 3        | 3     | 3        | 3       | 3        | ns   | min   |
| TEHQZ  | $\overline{\text{CS}}$ high to high Z | 30      | 40       | 30      | 40       | 35    | 40       | 35      | 40       | ns   | max   |
| TGLQV  | Output Enable access time             | 15      | 20       | 15      | 20       | 20    | 25       | 20      | 25       | ns   | max   |
| TGLQX  | $\overline{\text{OE}}$ low to low Z   | 2       | 2        | 2       | 2        | 2     | 2        | 2       | 2        | ns   | min   |
| TGHQZ  | $\overline{\text{OE}}$ high to high Z | 10      | 15       | 10      | 15       | 20    | 20       | 20      | 20       | ns   | max   |

READ CYCLE nb 1 (notes 16, 17)



READ CYCLE nb 2 (notes 16, 18)



- Notes : 16.  $\overline{\text{W}}$  is high for read cycle.  
17. Device is continuously selected  $\overline{\text{CS}}$  &  $\overline{\text{OE}}$  = VIL.  
18. Address valid prior to or coincident with CS transition low.

| TEMPERATURE RANGE<br>IM                                                                                                   | PACKAGE<br>1I                                                                                                                                                                                                      | DEVICE<br>- 65656     | GRADE<br>V                          | SPEED<br>- 45           | FLOW<br>MB                                                                                                                                                                                                                                                                                                         |
|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------------------------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C = COMMERCIAL 0° 70°C<br>I = INDUSTRIAL - 40° to + 85°C<br>M = MILITARY - 55° to + 125°C<br>S = SPATIAL - 55° to + 125°C | 1I = 28 pins DIL CERAMIC 600 mils<br>CI = 28 pins DIL SIDE-BRAZED 600 mils<br>CP = 28 pins DIL SIDE-BRAZED 300 mils<br>NP = 28 pins SO L CERAMIC 300 mils<br>3 = 28 pins DIP 300 mils<br>T = 28 pins SOIC 300 mils | 32K x 8<br>STATIC RAM | V = Very low power<br>L = Low power | 35 ns<br>45 ns<br>55 ns | blank = no special flow<br>- 8 = MHS MILITARY PROGRAM<br>MB = MIL-STD 883C CLASS B<br>CB = COMPLIANT CECC 90000 LEVEL B<br>SHXXX = SPECIAL CUSTOMER REQUEST<br>FHXXX = FLIGHT MODELS (SPATIAL)<br>EHXXX = ENGINEERING MODELS (SPATIAL)<br>MHXXX = MECHANICAL PARTS (SPATIAL)<br>LHXXX = LIFE TESTS PARTS (SPATIAL) |

# HIGH SPEED CMOS SRAM





## DATA SHEET

## HM 65767

# 16 K x 1 HIGH SPEED CMOS SRAM

## FEATURES

- FAST ACCESS TIME  
MILITARY : 25/35/45/55 ns (max)  
COMMERCIAL : 20/25/35/45/55 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 275 mW (typ)  
STANDBY : 55 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

## DESCRIPTION

The HM 65767 is a high speed CMOS static RAM organized as 16384x1 bit. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 20 ns are available with maximum power consumption of only 385 mW. The HM 65767 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 70 % when the circuit is deselected.

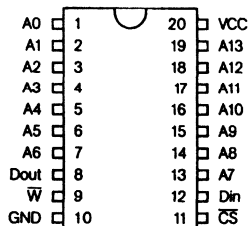
Easy memory expansion is provided by an active low chip select (CS) and three state drivers. All inputs and outputs of the HM 65767 are TTL compatible and operate from single 5 V supply thus simplifying system design. The HM 65767 is processed following the test methods of MIL STD 883C.

## PACKAGES

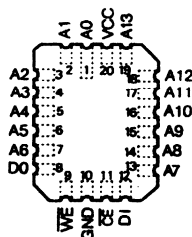
Plastic 300 mils, 20 pins, DIL.  
Ceramic 300 mils, 20 pins, DIL.  
Tape and Reel Service.

SOIC 300 mils, 20 pins  
LCC 20 pins.

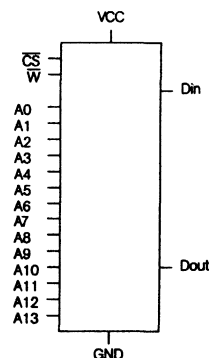
### Pinout DIL 20 pins (top view)



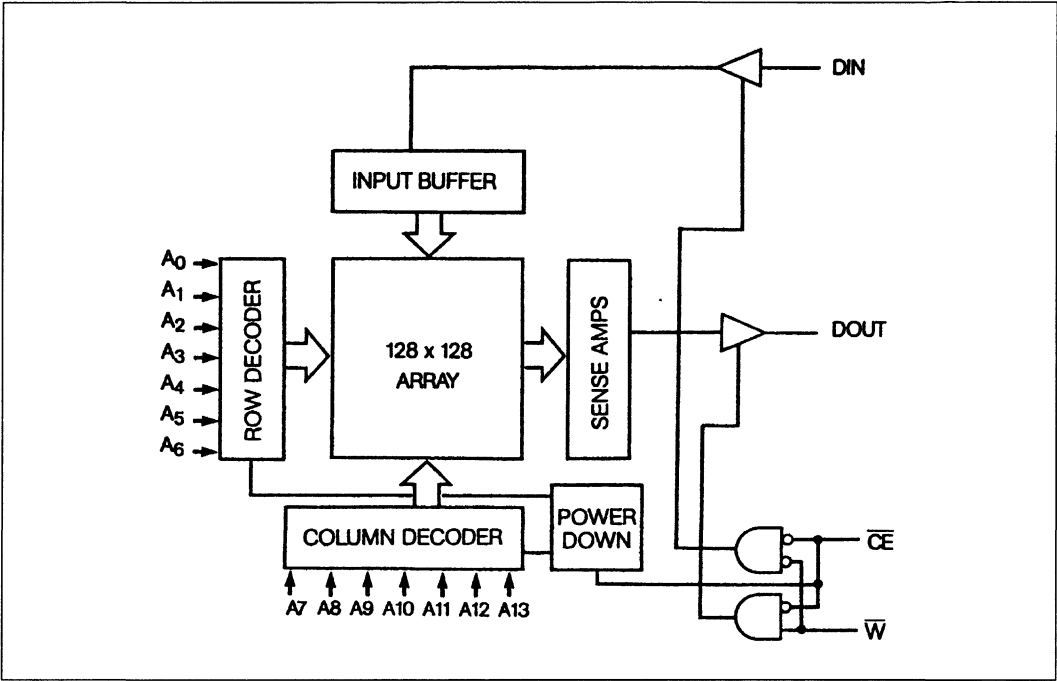
### Pinout LCC 20 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                 |                  |                |                |
|-----------------|------------------|----------------|----------------|
| A0-A13          | : Address inputs | $\overline{W}$ | : Write enable |
| Din             | : Input          | Vcc            | : Power        |
| Dout            | : Output         | GND            | : Ground       |
| $\overline{CS}$ | : Chip Select    |                |                |

TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

L = low - H = high - X = H or L, Z = high impedance

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$

Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$   
 Output current into outputs (low) :  $20\text{ mA}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

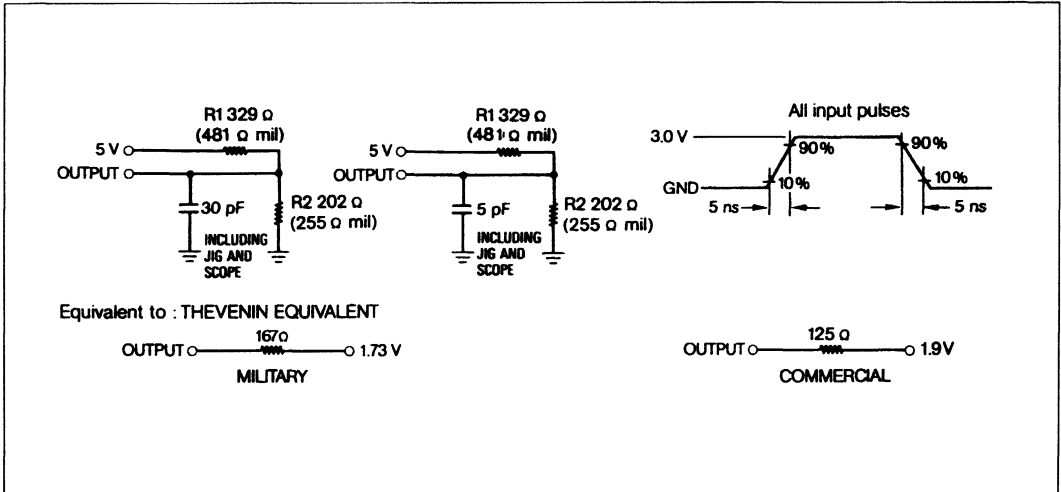
**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.0     | —       | 5.5     | V    |

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 4       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |
| C CS (1)  | CS capacitance     | —       | —       | 5       | pF   |

Note : 1.  $T_A = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{cc} = 5.0\text{ V}$ .

**AC TEST LOADS AND WAVEFORMS**

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|------------------------------|---------|---------|---------|---------|
| IIX (2)   | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ (3)   | Output leakage current       | - 50.0  | -       | 50.0    | $\mu$ A |
| IOS (3)   | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL (4)   | Output low voltage           | -       | -       | 0.4     | V       |
| VOH (5)   | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :** 2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.  
 3.  $V_{cc} = \text{max}$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
 4.  $V_{cc} \text{ min}$ ,  $I_{OL} = 12.0 \text{ mA}$  (commercial)  $8.0 \text{ mA}$  (military).  
 5.  $V_{cc} \text{ min}$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**Consumption for Commercial specification :**

| SYMBOL    | PARAMETER                 | 65767<br>F-5 | 65767<br>H-5 | 65767<br>K-5 | 65767<br>M-5 | 65767<br>N-5 | UNIT | VALUE |
|-----------|---------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current    | 30           | 20           | 20           | 20           | 30           | mA   | max   |
| ICCOP (7) | Dynamic operating current | 70           | 70           | 70           | 70           | 90           | mA   | max   |

**Consumption for Military specification :**

| SYMBOL    | PARAMETER                 | 65767<br>H-2 | 65767<br>K-2 | 65767<br>M-2 | 65767<br>N-2 | UNIT | VALUE |
|-----------|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current    | 30           | 20           | 20           | 20           | mA   | max   |
| ICCOP (7) | Dynamic operating current | 80           | 70           | 70           | 70           | mA   | max   |

- Notes :** 6.  $\overline{CS} \leq V_{IH}$ , a pull-up resistor to  $V_{cc}$  on the  $\overline{CS}$  input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values above.  
 7.  $V_{cc} \text{ max}$ , Output current = 0 mA,  $f = \text{max}$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .  
 \* Preliminary specification.



## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH : + 30 pF

## WRITE CYCLE : Commercial specification

| SYMBOL    | PARAMETER                               | 65767<br>F-5 | 65767<br>H-5 | 65767<br>K-5 | 65767<br>M/N-5 | UNIT | VALUE |
|-----------|-----------------------------------------|--------------|--------------|--------------|----------------|------|-------|
| TAVAV     | Write cycle time                        | 20           | 25           | 30           | 40             | ns   | min   |
| TAVWL     | Address set-up time                     | 0            | 0            | 0            | 0              | ns   | min   |
| TAVWH     | Address valid to end of write           | 20           | 25           | 30           | 40             | ns   | min   |
| TDVWH     | Data set-up time                        | 15           | 15           | 15           | 15             | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end | 20           | 25           | 30           | 40             | ns   | min   |
| TWLQZ (8) | Write low to high Z                     | 10           | 25           | 30           | 20             | ns   | max   |
| TWLWH     | Write pulse width                       | 15           | 15           | 20           | 20             | ns   | min   |
| TWHAX     | Address hold to end of write            | 2            | 2            | 2            | 2              | ns   | min   |
| TWDHX     | Data hold time                          | 0            | 0            | 0            | 0              | ns   | min   |
| TWHQX (8) | Write high to low Z                     | 3            | 0            | 0            | 0              | ns   | min   |
| TEHAX     | Address hold end $\overline{\text{CS}}$ | 3            | 3            | 3            | 3              | ns   | min   |

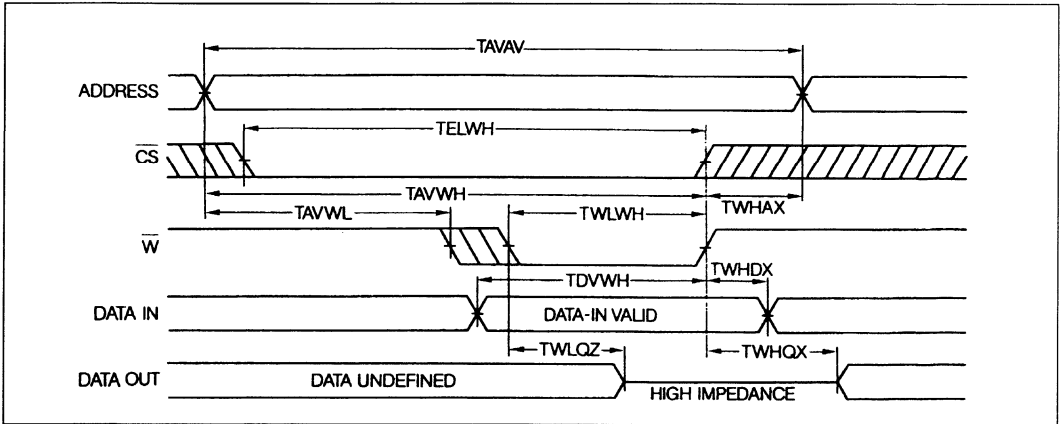
4

## WRITE CYCLE : Military specification

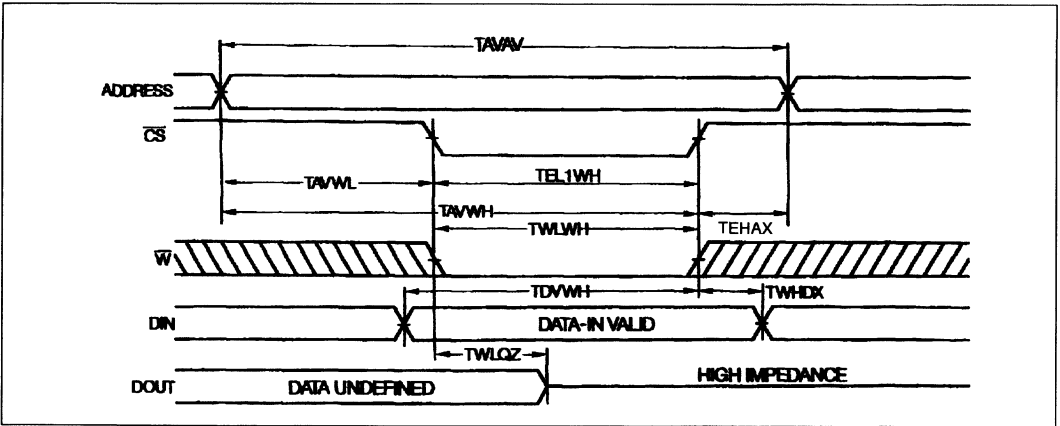
| SYMBOL    | PARAMETER                               | 65767<br>H-2 | 65767<br>K-2 | 65767<br>M-2 | 65767<br>N-2 | UNIT | VALUE |
|-----------|-----------------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                        | 25           | 30           | 40           | 40           | ns   | min   |
| TAVWL     | Address set-up time                     | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Space <sup>1</sup>                      | 25           | 30           | 40           | 40           | ns   | min   |
| TDVWH     | Data set-up time                        | 15           | 15           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end | 25           | 30           | 40           | 40           | ns   | min   |
| TWLQZ (8) | Write low to high Z                     | 15           | 20           | 20           | 20           | ns   | max   |
| TWLWH     | Write pulse width                       | 15           | 20           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold to end of write            | 0            | 0            | 0            | 0            | ns   | min   |
| TWDHX     | Data hold time                          | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z                     | 3            | 0            | 0            | 0            | ns   | min   |
| TEHAX     | Address hold end $\overline{\text{CS}}$ | 3            | 3            | 3            | 3            | ns   | min   |

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)



WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)



**READ CYCLE : Commercial specification**

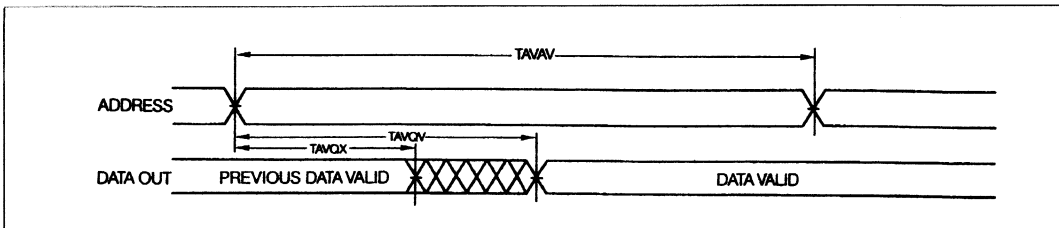
| SYMBOL | PARAMETER                          | 65767<br>F-5 | 65767<br>H-5 | 65767<br>K-5 | 65767<br>M-5 | 65767<br>N-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 20           | 25           | 30           | 40           | 50           | ns   | min   |
| TAVQV  | Address access time                | 20           | 25           | 30           | 40           | 50           | ns   | max   |
| TAVQX  | Address valid to low Z             | 2            | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 5            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 15           | 20           | 25           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 20           | 25           | 30           | 30           | ns   | max   |

**READ CYCLE : Military specification**

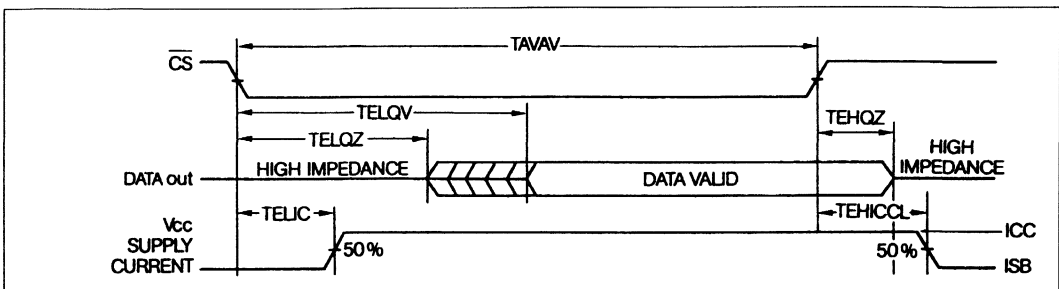
| SYMBOL | PARAMETER                          | 65767<br>H-2 | 65767<br>K-2 | 65767<br>M-2 | 65767<br>N-2 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 25           | 35           | 40           | 50           | ns   | min   |
| TAVQV  | Address access time                | 25           | 35           | 40           | 50           | ns   | max   |
| TAVQX  | Address valid to low Z             | 2            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 25           | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 10           | 20           | 25           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 25           | 30           | 30           | ns   | max   |

\* Preliminary specification.

**READ CYCLE nb 1**



**READ CYCLE nb 2**



# ORDERING INFORMATION

| Package             | Device type                          | Grade     | Level                    |                       |
|---------------------|--------------------------------------|-----------|--------------------------|-----------------------|
| HM1                 | 65767 (A)                            | H         | - 5 : R                  | Tape and Reel Service |
|                     | 16 k x 1 high speed power static RAM |           | - 5 : Commercial         |                       |
|                     |                                      |           | - 2 : Military           |                       |
|                     |                                      |           | - 8 : Military with B.I. |                       |
|                     |                                      |           | (B.I. = Burn-In)         |                       |
| 0 - Chip form       |                                      | F = 20 ns |                          |                       |
| 1 - Ceramic 20 pins |                                      | H = 25 ns |                          |                       |
| 3 - Plastic 20 pins |                                      | K = 35 ns |                          |                       |
| 300 mils            |                                      | M = 45 ns |                          |                       |
| 4 - LCC 20 pins     |                                      | N = 55 ns |                          |                       |
| T - SOIC 20 pins    |                                      |           |                          |                       |

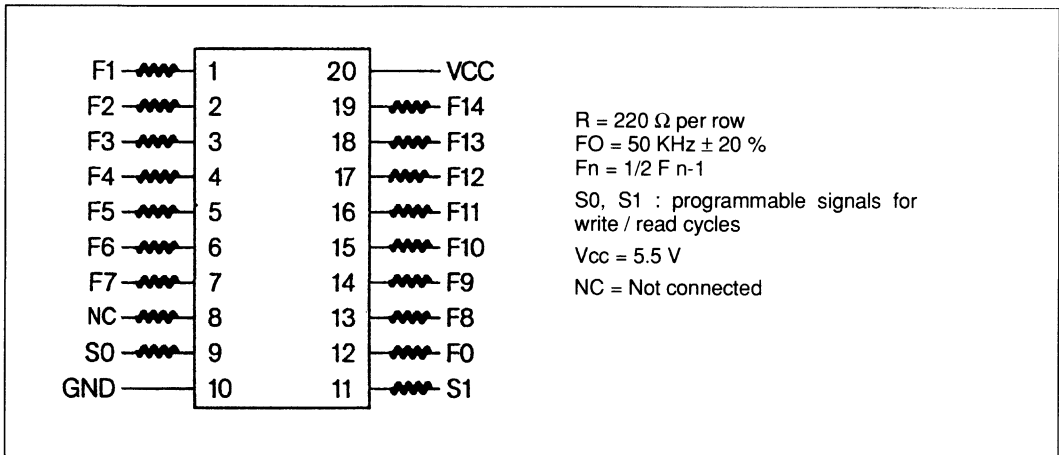
## 4

### PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 20 pins  
 SOIC DIL, 300 mils, 20 pins  
 Ceramic, 300 mils, 20 pins  
 LCC rectangular, 20 pins.

### BURN-IN SCHEMATICS



## DATA SHEET

## HM 65768

# 4 K x 4 HIGH SPEED CMOS SRAM

## FEATURES

- FAST ACCESS TIME  
MILITARY : 25\*/35/45/55 ns (max)  
COMMERCIAL : 20/25/35/45/55 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 200 mW (typ)  
STANDBY : 35 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

## DESCRIPTION

The HM 65768 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 20 ns are available with maximum power consumption of only 385 mW. The HM 65768 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 77 % when the circuit is deselected.

Each memory expansion is provided by an active low chip select (CS) and three state drivers.

All inputs and outputs of the HM 65768 are TTL compatible and operate from single 5 V supply thus simplifying system design.

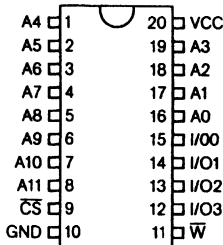
The HM 65768 is processed following the test methods of MIL STD 883C.

## PACKAGES

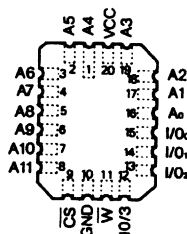
Plastic 300 mils, 20 pins, DIL.  
Ceramic 300 mils, 20 pins, DIL.  
Tape and Reel Service

SOIC 300 mils, 20 pins, DIL.  
SOJ 300 mils, 20 pins  
LCC 20 pins.

## Pinout DIL 20 pins (top view)

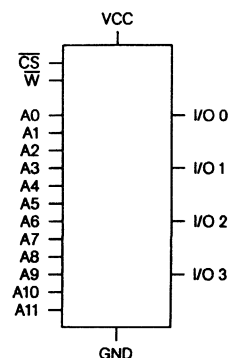


## Pinout LCC 20 pins (top view)

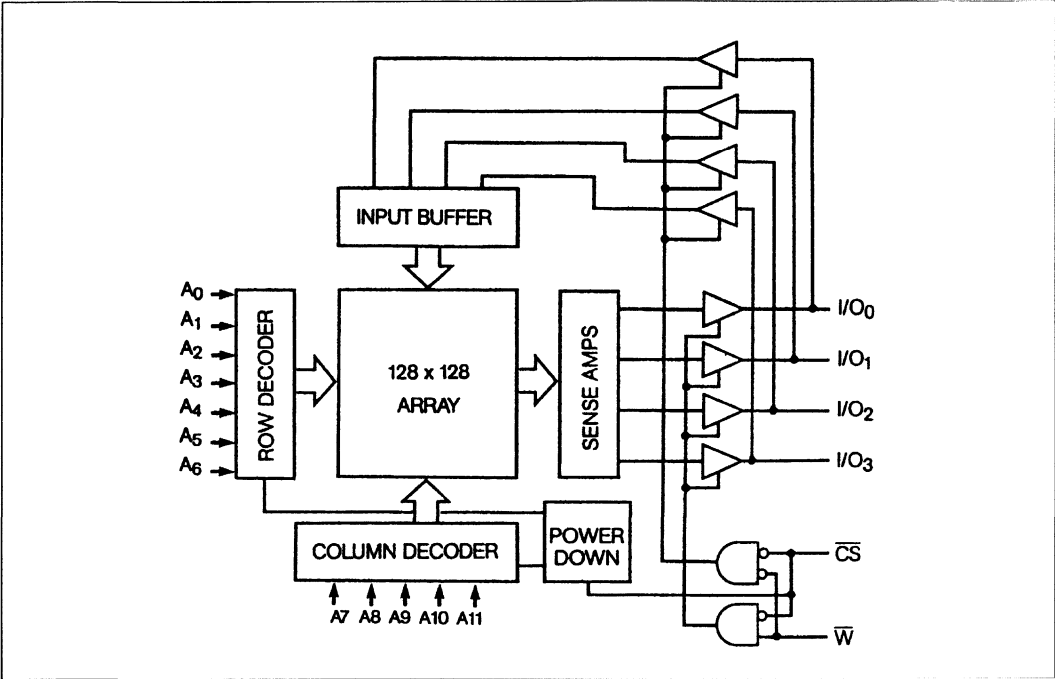


\* preliminary specification

## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|           |                  |                 |                |
|-----------|------------------|-----------------|----------------|
| A0-A11    | : Address inputs | $\overline{CS}$ | : Chip Select  |
| I/O0-I/O3 | : Input/Output   | $\overline{W}$  | : Write enable |
| Vcc       | : Power          |                 |                |
| Gnd       | : Ground         |                 |                |

TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$

Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$   
 Output current into outputs (low) :  $20\text{ mA}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.0     | —       | 5.5     | V    |

4

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 4       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

L = low, H = high, X = H or L, Z = high impedance

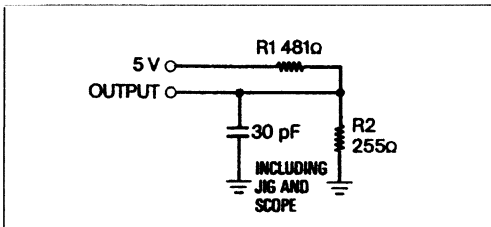
**AC TEST LOADS WAVEFORMS**

Fig. 1a.

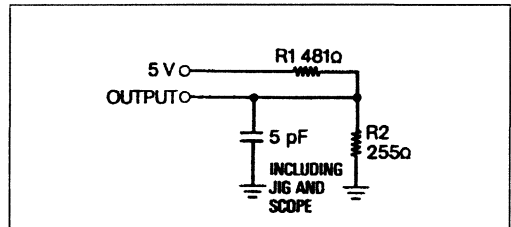


Fig. 1b.

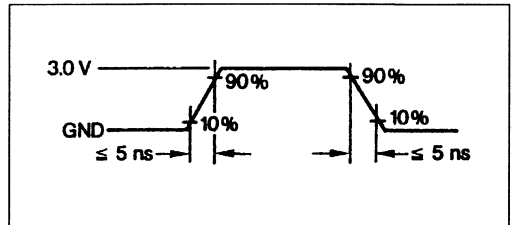
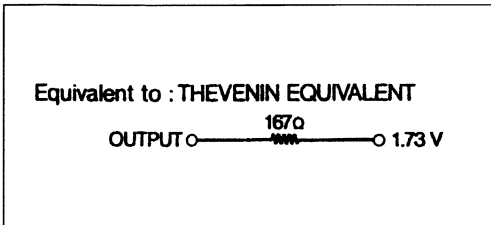


Fig. 2.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|-----|------------------------------|---------|---------|---------|------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | μA   |
| IOZ       | (3) | Output leakage current       | - 50.0  | -       | 50.0    | μA   |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA   |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V    |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V    |

**Note :** 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V.

**Notes :** 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.

3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.

Not more than 1 output should be shorted at one time.

4. Vcc min, IOL = 8.0 mA .

**Consumption for Commercial specification :**

| SYMBOL     | PARAMETER                 | 65768<br>F-5* | 65768<br>H-5 | 65768<br>K-5 | 65768<br>M-5 | 65768<br>N-5 | UNIT | VALUE |
|------------|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 30            | 15           | 15           | 15           | 30           | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 30            | 11           | 11           | 11           | 30           | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 70            | 70           | 70           | 70           | 90           | mA   | max   |

**Consumption for Commercial specification :**

| SYMBOL     | PARAMETER                 | 65768<br>F-5* | 65768<br>H-5 | 65768<br>K-5 | 65768<br>M-5 | 65768<br>N-5 | UNIT | VALUE |
|------------|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 30            | 15           | 15           | 15           | 30           | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 30            | 11           | 11           | 11           | 30           | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 70            | 70           | 70           | 70           | 90           | mA   | max   |

**Notes :** 5. Vcc min, IOH = - 4.0 mA.

6. CS ≥ VIH, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.

7. CS ≥ Vcc - 300 mV.

8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.



## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : +30 pF

## WRITE CYCLE : Commercial specification

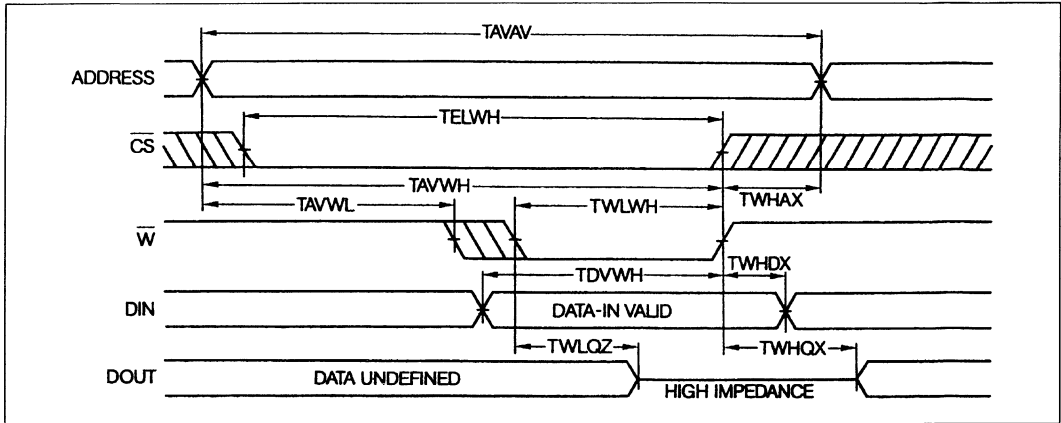
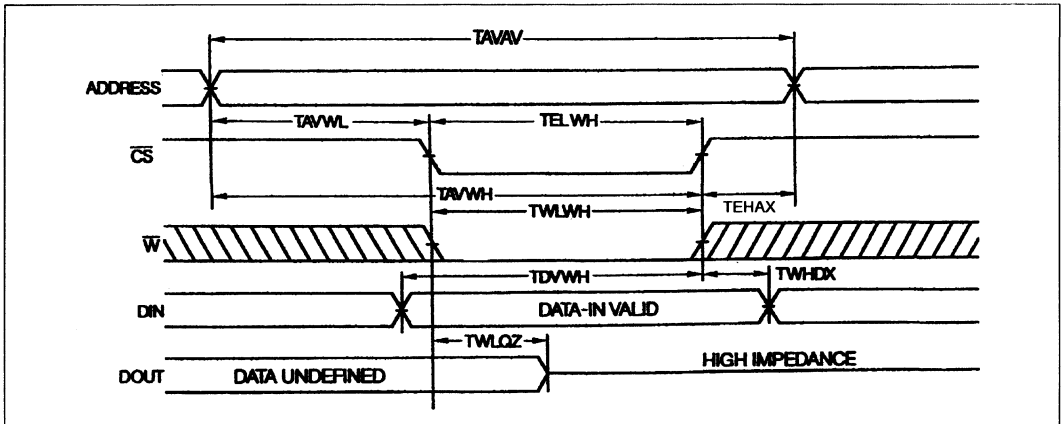
| SYMBOL    | PARAMETER                      | 65768<br>F-5* | 65768<br>H-5 | 65768<br>K-5 | 65768<br>M/N-5 | UNIT | VALUE |
|-----------|--------------------------------|---------------|--------------|--------------|----------------|------|-------|
| TAVAV     | Write Cycle time               | 20            | 25           | 35           | 40             | ns   | min   |
| TAVWL     | Address set-up time            | 0             | 0            | 0            | 0              | ns   | min   |
| TAVWH     | Address valid to end of write  | 15            | 20           | 30           | 35             | ns   | min   |
| TDVWH     | Data set-up time               | 10            | 15           | 15           | 15             | ns   | min   |
| TELWH     | CS low to write end            | 15            | 25           | 35           | 35             | ns   | min   |
| TWLQZ (9) | Write low to high Z            | 10            | 10           | 15           | 20             | ns   | max   |
| TWLWH     | Write pulse width              | 15            | 20           | 30           | 35             | ns   | min   |
| TWHAX     | Address hold from end of write | 0             | 0            | 0            | 0              | ns   | min   |
| TWHDX     | Data hold time                 | 0             | 0            | 3            | 3              | ns   | min   |
| TWHQX (9) | Write high to low Z            | 3             | 6            | 6            | 6              | ns   | min   |
| TEHAX     | Address hold from end CS       | 3             | 3            | 3            | 3              | ns   | min   |

4

## WRITE CYCLE : Military specification

| SYMBOL    | PARAMETER                      | 65768<br>H-2* | 65768<br>K-2 | 65768<br>M-2 | 65768<br>N-2 | UNIT | VALUE |
|-----------|--------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write Cycle time               | 25            | 35           | 40           | 40           | ns   | min   |
| TAVWL     | Address set-up time            | 0             | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write  | 20            | 30           | 35           | 35           | ns   | min   |
| TDVWH     | Data set-up time               | 15            | 15           | 15           | 15           | ns   | min   |
| TELWH     | CS low to write end            | 25            | 35           | 35           | 35           | ns   | min   |
| TWLQZ (9) | Write low to high Z            | 10            | 15           | 20           | 20           | ns   | max   |
| TWLWH     | Write pulse width              | 20            | 30           | 35           | 35           | ns   | min   |
| TWHAX     | Address hold from end of write | 2             | 2            | 2            | 2            | ns   | min   |
| TWHDX     | Data hold time                 | 0             | 0            | 3            | 3            | ns   | min   |
| TWHQX (9) | Write high to low Z            | 3             | 6            | 6            | 6            | ns   | min   |
| TEHAX     | Address hold from end CS       | 3             | 3            | 3            | 3            | ns   | min   |

Note : 9. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)

**READ CYCLE : Commercial specification**

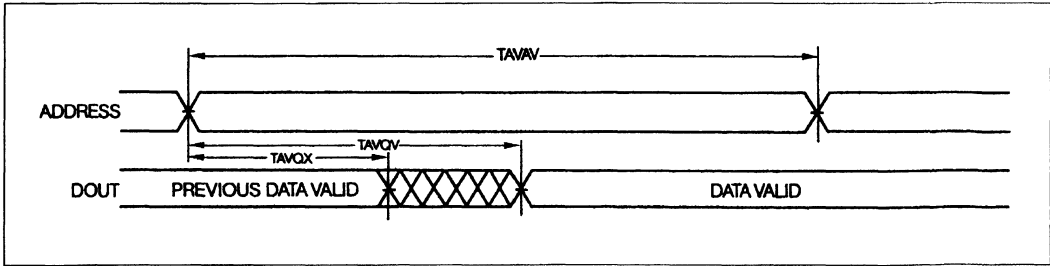
| SYMBOL | PARAMETER                          | 65768<br>F-5 | 65768<br>H-5 | 65768<br>K-5 | 65768<br>M-5 | 65768<br>N-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 20           | 25           | 35           | 45           | 55           | ns   | min   |
| TAVQV  | Address access time                | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TAVQX  | Address valid to low Z             | 2            | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 5            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 15           | 20           | 25           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 25           | 25           | 25           | 30           | 30           | ns   | max   |

**READ CYCLE : Military specification**

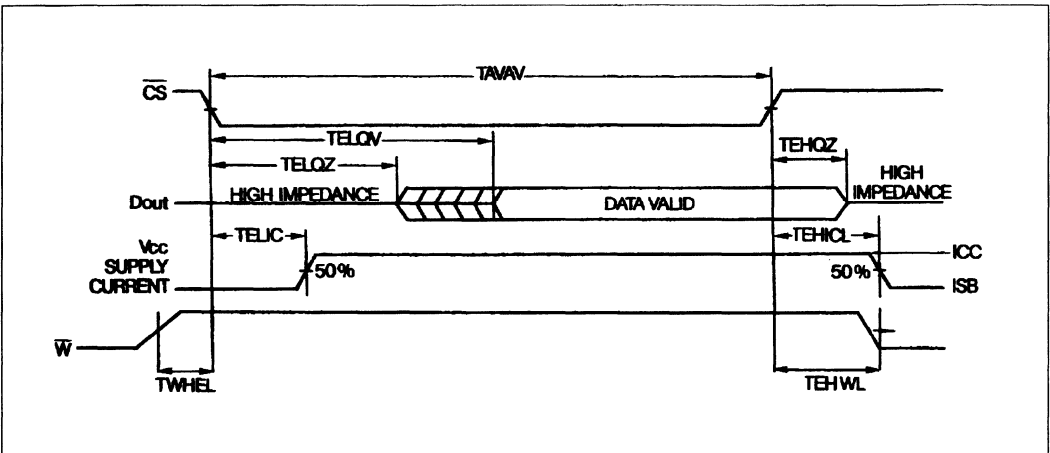
| SYMBOL | PARAMETER                          | 65768<br>H-2* | 65768<br>K-2 | 65768<br>M-2 | 65768<br>N-2 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 25            | 35           | 45           | 55           | ns   | min   |
| TAVQV  | Address access time                | 25            | 35           | 45           | 55           | ns   | max   |
| TAVQX  | Address valid to low Z             | 2             | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 25            | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5             | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15            | 20           | 25           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 5             | 25           | 30           | 30           | ns   | max   |

\* Preliminary specification.

## READ CYCLE nb 1



## READ CYCLE nb 2



### ORDERING INFORMATION

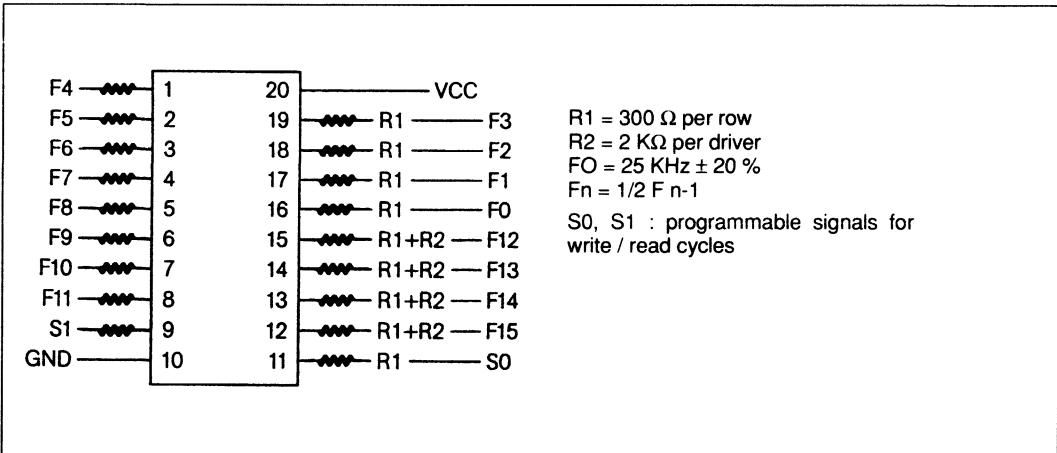
| Package             | Device type                   | Grade     | Level                    |                       |
|---------------------|-------------------------------|-----------|--------------------------|-----------------------|
| HM1                 | 65768A                        | H         | - 5 : R                  |                       |
|                     | 4 k x 4 high speed static RAM |           |                          | Tape and Reel Service |
| 0 - Chip form       |                               | F = 20 ns | - 5 : Commercial         |                       |
| 1 - Ceramic 20 pins |                               | H = 25 ns | - 2 : Military           |                       |
| 3 - Plastic 20 pins |                               | K = 35 ns | - 8 : Military with B.I. |                       |
| 4 - LCC 20 pins     |                               | M = 45 ns | (B.I. = Burn-In)         |                       |
| T - SOIC 20 pins    |                               | N = 55 ns |                          |                       |
| U - SOJ 20 pins     |                               |           |                          |                       |

### PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 20 pins  
 SOIC DIL, 300 mils, 20 pins  
 Ceramic, 300 mils, 20 pins  
 LCC rectangular, 20 pins

### BURN-IN SCHEMATICS





## DATA SHEET

## HM 65770

# 4 K x 4

## HIGH SPEED CMOS SRAM

### WITH OUTPUT ENABLE

## FEATURES

- FAST ACCESS TIME
  - MILITARY : 25/35/45 ns (max)
  - COMMERCIAL : 20/25/35/45 ns (max)
- LOW POWER CONSUMPTION
  - ACTIVE : 385 mW (max)
  - STANDBY : 27.5 mW (max)
- WIDE TEMPERATURE RANGE :
  - 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY
- OUTPUT ENABLE

4

## DESCRIPTION

The HM 65770 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 20 ns are available with maximum power consumption of only 385 mW.

The HM 65770 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 90 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS), an active low output enable (OE) and three state drivers.

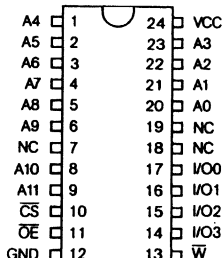
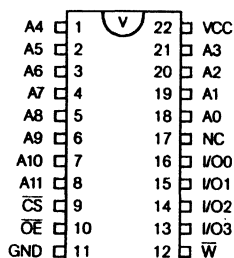
All inputs and outputs of the HM 65770 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65770 is processed following the test methods of MIL STD 883C.

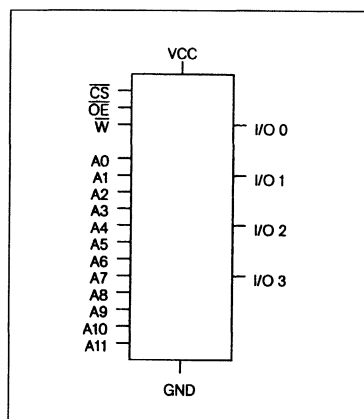
## PACKAGES

Plastic 300 mils, 22 pins, DIL.      SO 300 mils, 24 pins  
Ceramic 300 mils, 22 pins, DIL.

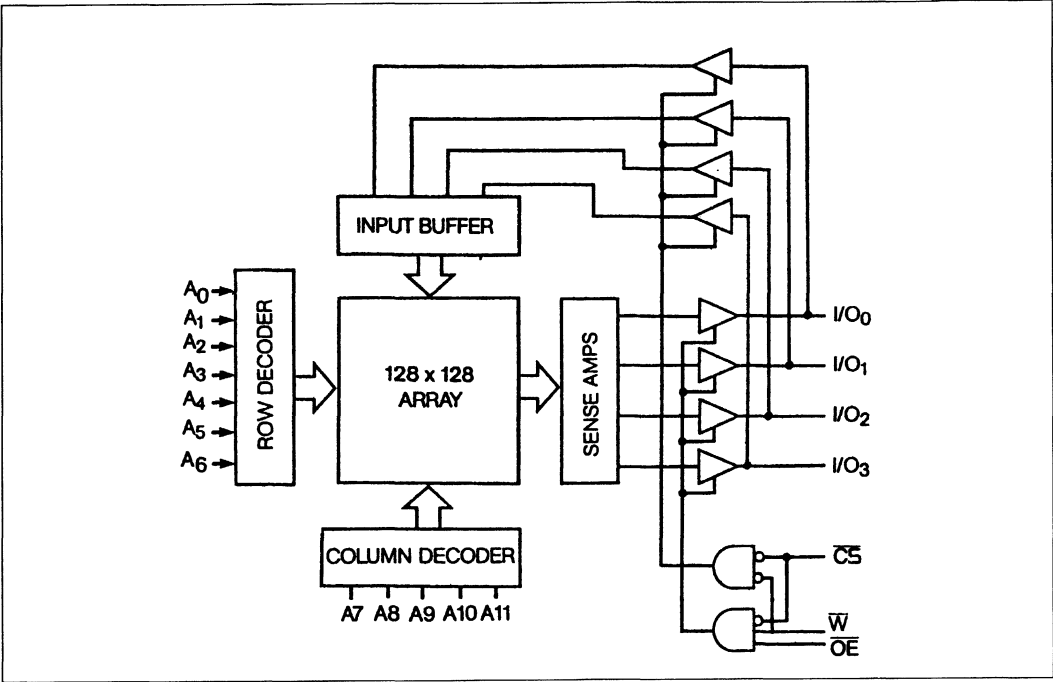
## Pinout DIL 22/24 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|           |                  |                 |                 |
|-----------|------------------|-----------------|-----------------|
| A0-A11    | : Address inputs | $\overline{CS}$ | : Chip Select   |
| I/O0-I/O3 | : Input/Output   | $\overline{W}$  | : Write enable  |
| Vcc       | : Power          | $\overline{OE}$ | : Output enable |
| Gnd       | : Ground         |                 |                 |

TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|-----------------|----------------|---------|----------|----------|
| H               | X               | X              | Z       | Z        | Deselect |
| L               | L               | H              | Z       | Valid    | Read     |
| L               | H               | L              | Valid   | Z        | Write    |
| L               | L               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance.



ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V  
DC input voltage : - 3.0 V to 7.0 V  
DC output voltage in high Z state : - 0.5 V to + 7.0 V

Storage temperature : - 65°C to + 150°C  
Output current into outputs (low) : 20 mA

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V $\pm$ 10 %    | - 55°C to + 125°C     |
| Commercial | (- 5) | 5 V $\pm$ 10 %    | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.0     | -       | VCC     | V    |

CAPACITANCE

| PARAMETER | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|------------------------|---------|---------|---------|------|
| Cin       | (1) Input capacitance  | -       | -       | 4       | pF   |
| Cout      | (1) Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C · f = 1 MHz · Vcc = 5.0 V. These parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

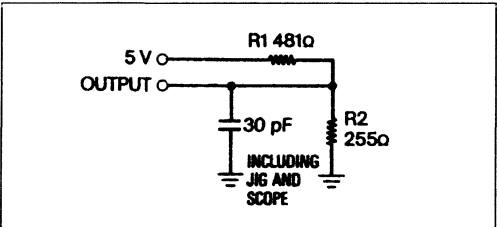


Fig. 1a.

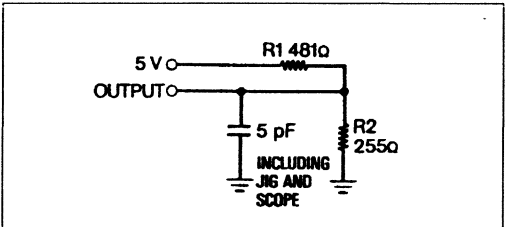


Fig. 1b.

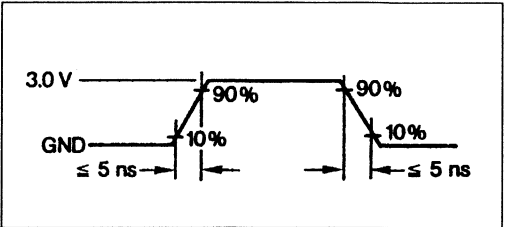
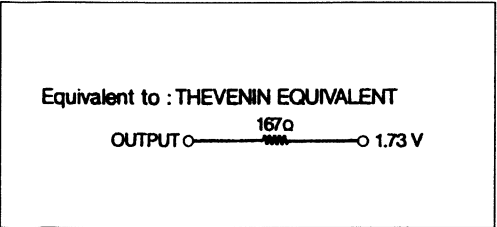


Fig. 2.

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|------------------------------|---------|---------|---------|---------|
| IIX (2)   | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ (3)   | Output leakage current       | - 50.0  | -       | 50.0    | $\mu$ A |
| IOS (3)   | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL (4)   | Output low voltage           | -       | -       | 0.4     | V       |
| VOH (5)   | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

## Consumption for Commercial specification :

| SYMBOL    | PARAMETER                 | 65770<br>F-5 | 65770<br>H-5 | 65770<br>K-5 | 65770<br>M-5 | UNIT | VALUE |
|-----------|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current    | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (7) | Dynamic operating current | 90           | 90           | 90           | 90           | mA   | max   |

## Consumption for Military specification :

| SYMBOL    | PARAMETER                 | 65770<br>H-2 | 65772<br>K-2 | 65770<br>M-2 | UNIT | VALUE |
|-----------|---------------------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current    | 20           | 20           | 20           | mA   | max   |
| ICCOP (7) | Dynamic operating current | 120          | 120          | 120          | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$ , a pull-up resistor to  $V_{cc}$  on the  $\overline{CS}$  input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values above.
  7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

## WRITE CYCLE : Commercial specification

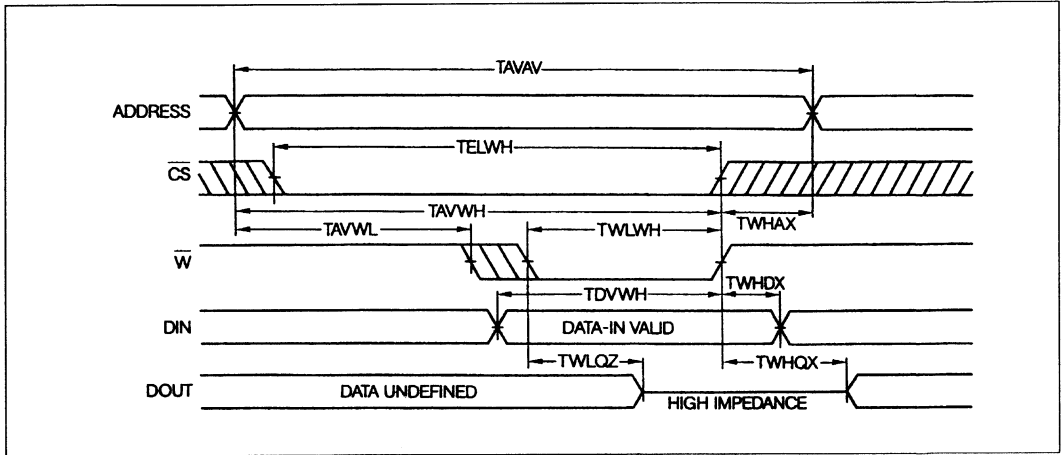
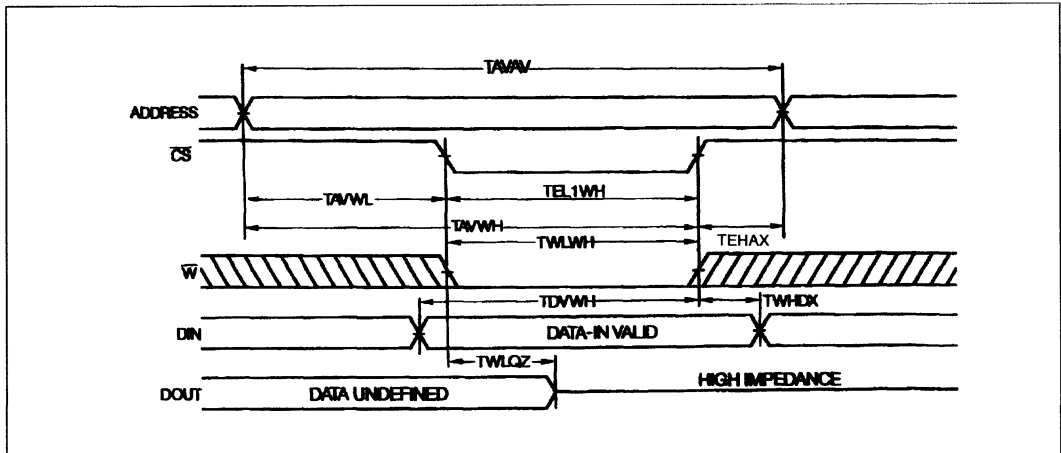
| SYMBOL    | PARAMETER                                    | 65770<br>F-5 | 65770<br>H-5 | 65770<br>K-5 | 65770<br>M-5 | UNIT | VALUE |
|-----------|----------------------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                             | 20           | 25           | 35           | 45           | ns   | min   |
| TAVWL     | Address set-up time                          | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write                | 15           | 20           | 30           | 35           | ns   | min   |
| TDVWH     | Data set-up time                             | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end      | 15           | 20           | 35           | 35           | ns   | min   |
| TWLQZ (8) | Write low to high Z                          | 10           | 10           | 15           | 20           | ns   | max   |
| TWLWH     | Write pulse width                            | 15           | 20           | 30           | 35           | ns   | min   |
| TWHAX     | Address hold from end of write               | 2            | 2            | 2            | 2            | ns   | min   |
| TWHDX     | Data hold time                               | 0            | 0            | 0            | 3            | ns   | min   |
| TWHQX (8) | Write high to low Z                          | 3            | 6            | 6            | 6            | ns   | min   |
| TEHAX     | Address hold from end $\overline{\text{CS}}$ | 3            | 3            | 3            | 3            | ns   | min   |

4

## WRITE CYCLE : Military specification

| SYMBOL    | PARAMETER                               | 65770<br>H-2 | 65770<br>K-2 | 65770<br>M-2 | UNIT | VALUE |
|-----------|-----------------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                        | 25           | 35           | 40           | ns   | min   |
| TAVWL     | Address set-up time                     | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write           | 20           | 30           | 35           | ns   | min   |
| TDVWH     | Data set-up time                        | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end | 25           | 30           | 35           | ns   | min   |
| TWLQZ (8) | Write low to high Z                     | 10           | 15           | 20           | ns   | max   |
| TWLWH     | Write pulse width                       | 20           | 30           | 35           | ns   | min   |
| TWHAX     | Address hold to end of write            | 2            | 2            | 2            | ns   | min   |
| TWHDX     | Data hold time                          | 0            | 0            | 3            | ns   | min   |
| TWHQX (8) | Write high to low Z                     | 6            | 6            | 6            | ns   | min   |
| TEHAX     | Address hold end $\overline{\text{CS}}$ | 3            | 3            | 3            | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 :  $\overline{W}$  Controlled (note 9)WRITE CYCLE 2  $\overline{CS}$  Controlled (note 9)

**Note :** 9. The internal write time of the memory is defined by the overlap of CS LOW and W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**READ CYCLE : Commercial specification**

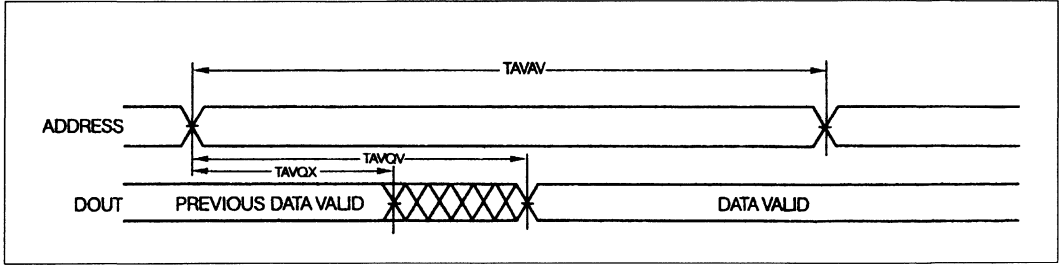
| SYMBOL | PARAMETER                          | 65770<br>F-5 | 65770<br>H-5 | 65770<br>K-5 | 65770<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Write cycle time                   | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 2            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 3            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 15           | 20           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 25           | 25           | 30           | ns   | max   |
| TGLQV  | Output Enable access time          | 12           | 15           | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 2            | 0            | 0            | 0            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 12           | 15           | 15           | 15           | ns   | max   |

4

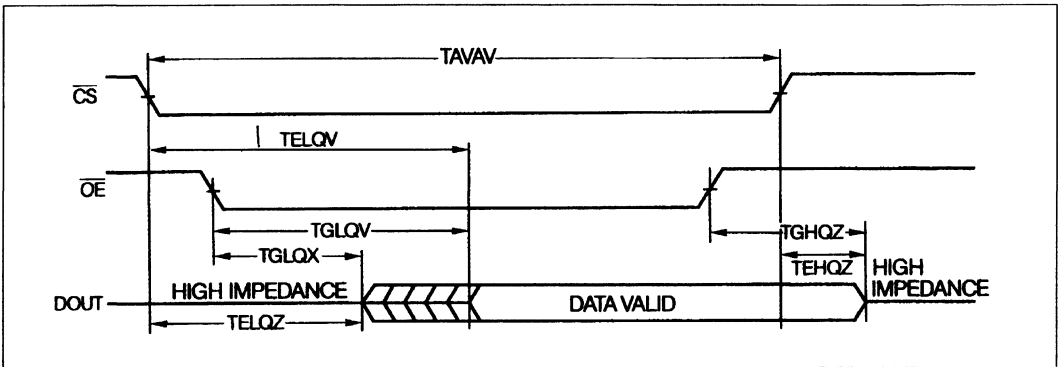
**READ CYCLE : Military specification**

| SYMBOL | PARAMETER                          | 65770<br>H-2 | 65770<br>K-2 | 65770<br>M-2 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 5            | 5            | 5            | ns   | min   |
| TELQV  | Chip-select access time            | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 20           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 25           | 30           | ns   | max   |
| TGLQV  | Output Enable access time          | 15           | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 0            | 0            | 0            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 15           | 15           | 20           | ns   | max   |

READ CYCLE nb 1 : (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



- Notes : 10.  $\overline{W}$  is HIGH for read cycle.  
 11. Device is continuously selected,  $\overline{CS}$  = VIL and  $\overline{OE}$  = VIL.  
 12. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

ORDERING INFORMATION

| Package                                                                       | Device                                           | Grade                                            | Level                                                                                                             |
|-------------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| HM1                                                                           | 65770                                            | K                                                | - 5                                                                                                               |
| 0 - Chip form<br>1 - Ceramic 22 pins<br>3 - Plastic 22 pins<br>T - SO 24 pins | 4 k x 4 high speed static RAM with Output Enable | F = 20 ns<br>H = 25 ns<br>K = 35 ns<br>M = 45 ns | - 5 : Commercial<br>- 5+ : Commercial with B.I.<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins  
 Ceramic, 300 mils, 20 pins  
 SOIC DIL 300 mils, 24 pins

DATA SHEET

HM 65772

4 k x 4  
HIGH SPEED CMOS SRAM  
SEPARATE I/O

FEATURES

- FAST ACCESS TIME  
MILITARY : 25/35/45 ns (max)  
COMMERCIAL : 20/25/35/45 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 385 mW (max)  
STANDBY : 27.5 mW (max)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY
- SEPARATE INPUT/OUTPUT

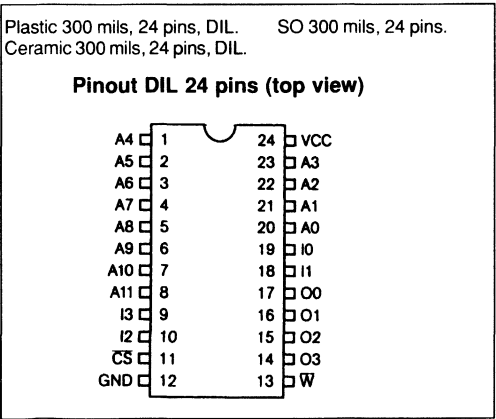
4

DESCRIPTION

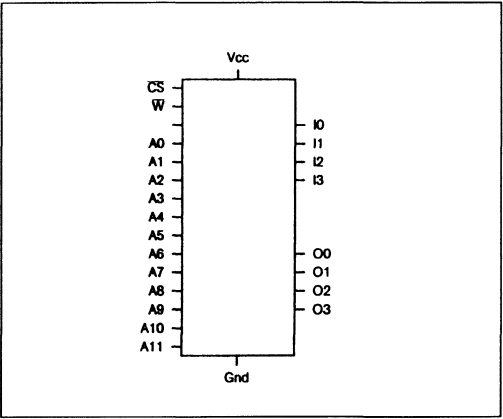
The HM 65772 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 20 ns are available with maximum power consumption of only 385 mW. The HM 65772 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 10 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS), four separate input/output buffers and three state drivers. All inputs and outputs of the HM 65772 are TTL compatible and operate from single 5 V supply thus simplifying system design. The HM 65772 is processed following the test methods of MIL STD 883C.

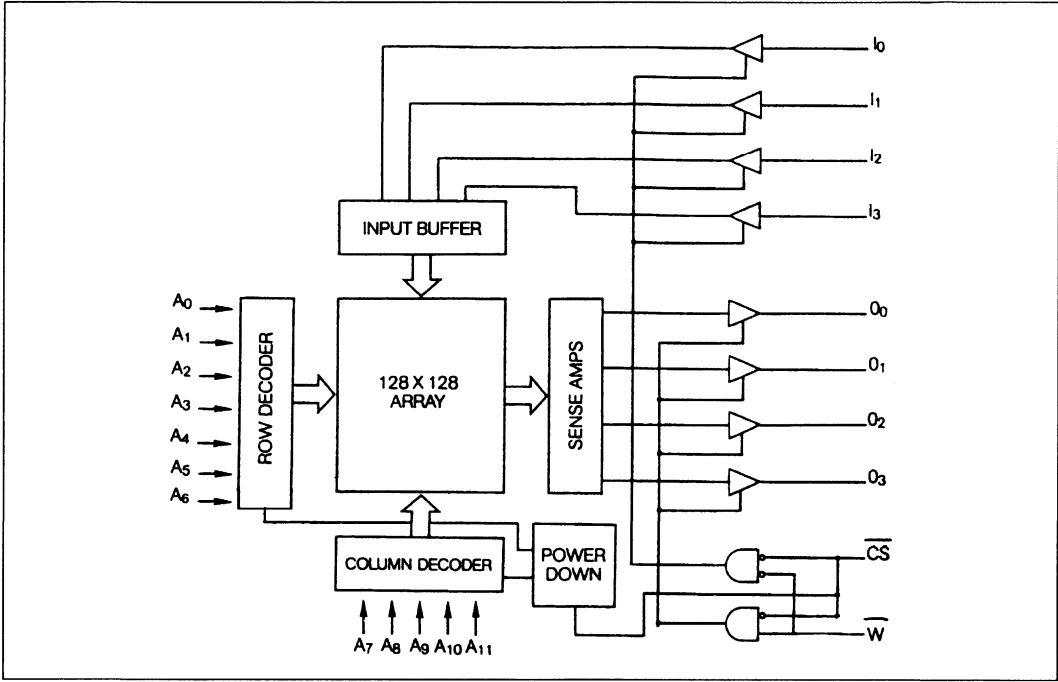
PACKAGES



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                |                  |                 |               |
|----------------|------------------|-----------------|---------------|
| A0-A11         | : Address inputs | $\overline{CS}$ | : Chip Select |
| I0-I3          | : Inputs         | VCC             | : Power       |
| O0-O3          | : Outputs        | GND             | : Ground      |
| $\overline{W}$ | : Write enable   |                 |               |

TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

Note : or L, Z = high impedance



**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$

Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$   
 Output current into outputs (low) :  $20\text{ mA}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 4       | pF   |
| Cout (1)  | Output Capacitance | -       | -       | 7       | pF   |

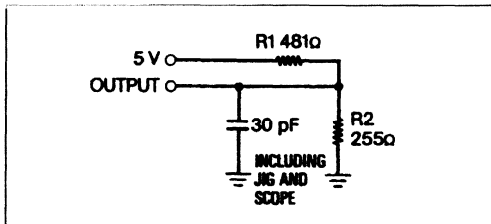
**AC TEST LOADS WAVEFORMS**

Fig. 1a.

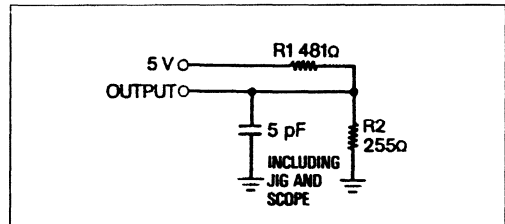


Fig. 1b.

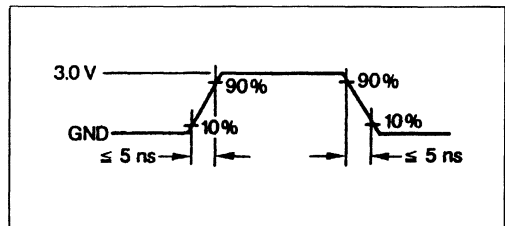
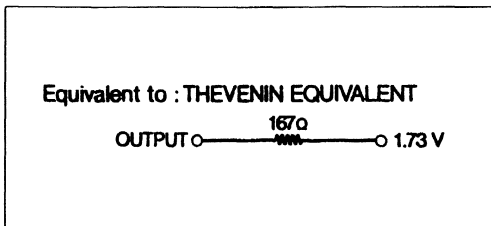


Fig. 2.

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 15.0  | -       | 10.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (4) | Output High voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

## Consumption for Commercial specification :

| SYMBOL    | PARAMETER                | 65772<br>F-5 | 65772<br>H-5 | 65772<br>K-5 | 65772<br>M-5 | UNIT | VALUE |
|-----------|--------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current   | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (7) | Operating supply current | 80           | 70           | 70           | 70           | mA   | max   |

## Consumption for Military specification :

| SYMBOL    | PARAMETER                | 65772<br>H-2 | 65772<br>K-2 | 65772<br>M-2 | UNIT | VALUE |
|-----------|--------------------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current   | 20           | 20           | 20           | mA   | max   |
| ICCOP (7) | Operating supply current | 90           | 90           | 90           | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$ , a pull up resistor to  $V_{cc}$  on the  $\overline{CS}$  input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values above.
  7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

## WRITE CYCLE : Commercial specification

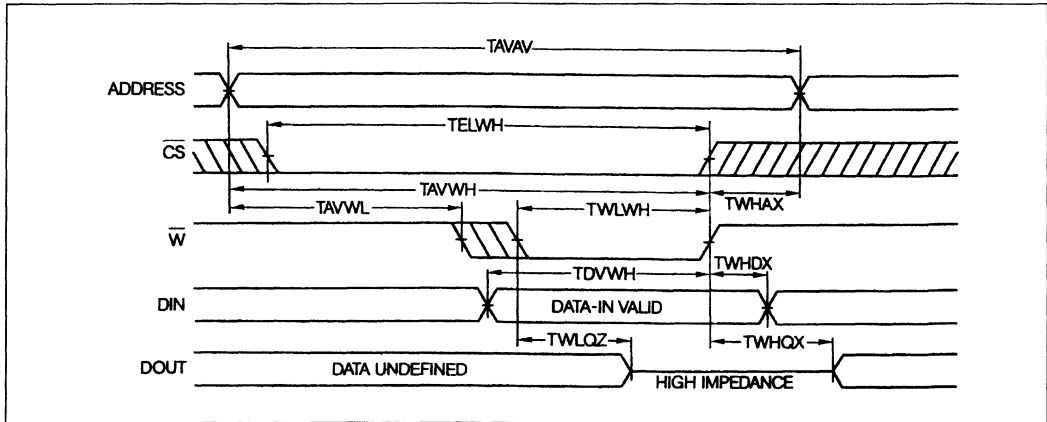
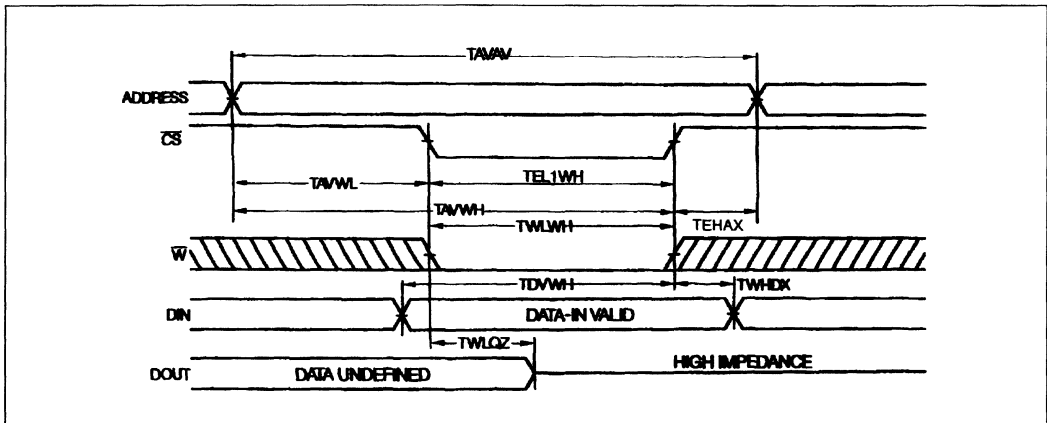
| SYMBOL    | PARAMETER                        | 65772<br>F-5 | 65772<br>H-5 | 65772<br>K-5 | 65772<br>M-5 | UNIT | VALUE |
|-----------|----------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write Cycle time                 | 20           | 25           | 35           | 45           | ns   | min   |
| TAVWL     | Address set-up time              | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write    | 15           | 20           | 30           | 40           | ns   | min   |
| TDVWH     | Data set-up time                 | 10           | 15           | 15           | 20           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 15           | 20           | 30           | 40           | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 10           | 10           | 15           | 20           | ns   | max   |
| TWLWH     | Write pulse width                | 15           | 20           | 30           | 40           | ns   | min   |
| TWHAX     | Address hold to end of write     | 2            | 2            | 2            | 2            | ns   | min   |
| TWDHX     | Data hold time                   | 0            | 0            | 0            | 3            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 3            | 6            | 6            | 6            | ns   | min   |
| TEHAX     | Address hold end $\overline{CS}$ | 3            | 3            | 3            | 3            | ns   | min   |

4

## WRITE CYCLE : Military specification

| SYMBOL    | PARAMETER                        | 65772<br>H-2 | 65772<br>K-2 | 65772<br>M-2 | UNIT | VALUE |
|-----------|----------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write Cycle time                 | 25           | 35           | 45           | ns   | min   |
| TAVWL     | Address set-up time              | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write    | 25           | 30           | 40           | ns   | min   |
| TDVWH     | Data set-up time                 | 20           | 20           | 20           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 25           | 30           | 40           | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 10           | 15           | 20           | ns   | max   |
| TWLWH     | Write pulse width                | 20           | 30           | 40           | ns   | min   |
| TWHAX     | Address hold to end of write     | 2            | 2            | 2            | ns   | min   |
| TWDHX     | Data hold time                   | 0            | 0            | 3            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 6            | 6            | 6            | ns   | min   |
| TEHAX     | Address hold end $\overline{CS}$ | 3            | 3            | 3            | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 10)WRITE CYCLE 2  $\overline{CS}$  CONTROLLED (note 10)

**Note :** 10. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**READ CYCLE : Commercial specification**

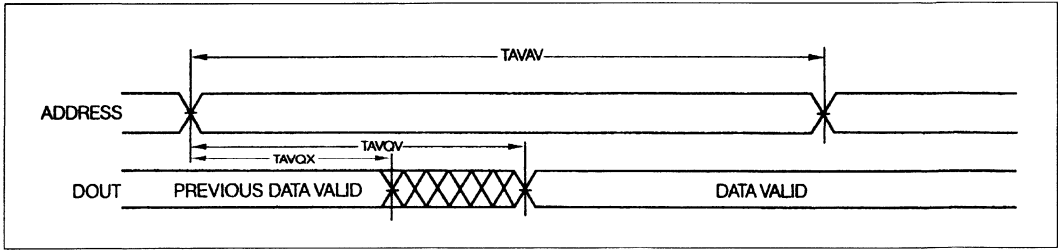
| SYMBOL | PARAMETER                          | 65772<br>F-5 | 65772<br>H-5 | 65772<br>K-5 | 65772<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ Cycle time                    | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQX  | Address valid to low Z             | 2            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 20           | 25           | 35           | 45           | ns   | min   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 15           | 20           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 25           | 25           | 30           | ns   | max   |

**READ CYCLE : Military specification**

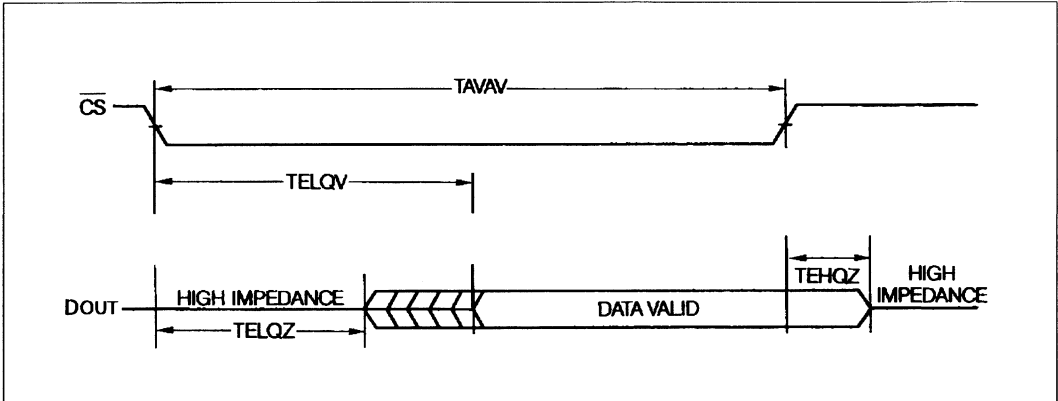
| SYMBOL | PARAMETER                          | 65772<br>H-2 | 65772<br>K-2 | 65772<br>M-2 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Write Cycle time                   | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 25           | 35           | 45           | ns   | min   |
| TAVQX  | Address valid to low Z             | 5            | 5            | 5            | ns   | min   |
| TELQV  | Chip-select access time            | 25           | 35           | 45           | ns   | min   |
| TELQX  | $\overline{CS}$ low to low Z       | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 15           | 20           | 25           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 25           | 25           | 30           | ns   | max   |

4

READ CYCLE nb1 : (notes 11, 12)



READ CYCLE nb2 : (notes 11, 13)



**Note** : 11. W is HIGH for Read cycle.

**Notes** : 12. Device is continuously selected, CS = VIL.

13. Address valid prior to or coincident with CS transition LOW.

ORDERING INFORMATION

| Package                                                                         | Device                                          | Grade                                            | Level                                                                              |
|---------------------------------------------------------------------------------|-------------------------------------------------|--------------------------------------------------|------------------------------------------------------------------------------------|
| HM1                                                                             | 65772                                           | K                                                | -5                                                                                 |
| 0 - Chip form<br>1 - Ceramic 24 pins<br>3 - Plastic 24 pins<br>T - SOIC 24 pins | 4 k x 4 high speed static RAM with separate I/O | F = 20 ns<br>H = 25 ns<br>K = 35 ns<br>M = 45 ns | - 5 : Commercial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins  
Ceramic DIL, 300 mils, 24 pins  
SOIC DIL, 300 mils, 24 pins

## DATA SHEET

## HM 65728

# 2 k x 8 HIGH SPEED CMOS SRAM

## FEATURES

- FAST ACCESS TIME
  - MILITARY : 35/45/55 ns (max)
  - COMMERCIAL : 20/25/35/45/55 ns (max)
- LOW POWER CONSUMPTION
  - ACTIVE : 310 mW (typ)
  - STANDBY : 55 mW (typ)
- WIDE TEMPERATURE RANGE :
  - 55°C TO + 125°C
- 300 AND 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

## DESCRIPTION

The HM 65728 is a high speed CMOS static RAM organized as 2048 x 8 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 20 ns are available with maximum power consumption of only 600 mW.

The HM 65728 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65728 are TTL compatible and operate from single 5V supply thus simplifying system design.

The HM 65728 is processed following the test methods of MIL STD 883C.

## PACKAGES

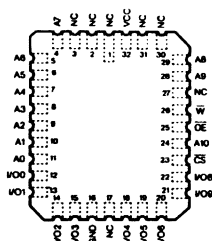
Plastic 300 & 600 mils, 24 pins, DIL  
SO 300 mils, 24 pins  
Tape and Reel Service

Ceramic 300 mils, 24 pins, DIL  
LCC, 32 pins

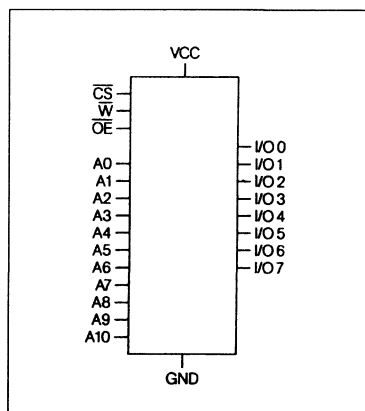
### Pinout DIL 24 pins (top view)

|      |    |    |      |
|------|----|----|------|
| A7   | 1  | 24 | VCC  |
| A6   | 2  | 23 | A8   |
| A5   | 3  | 22 | A9   |
| A4   | 4  | 21 | W    |
| A3   | 5  | 20 | OE   |
| A2   | 6  | 19 | A10  |
| A1   | 7  | 18 | CS   |
| A0   | 8  | 17 | I/O7 |
| I/O0 | 9  | 16 | I/O6 |
| I/O1 | 10 | 15 | I/O5 |
| I/O2 | 11 | 14 | I/O4 |
| GND  | 12 | 13 | I/O3 |

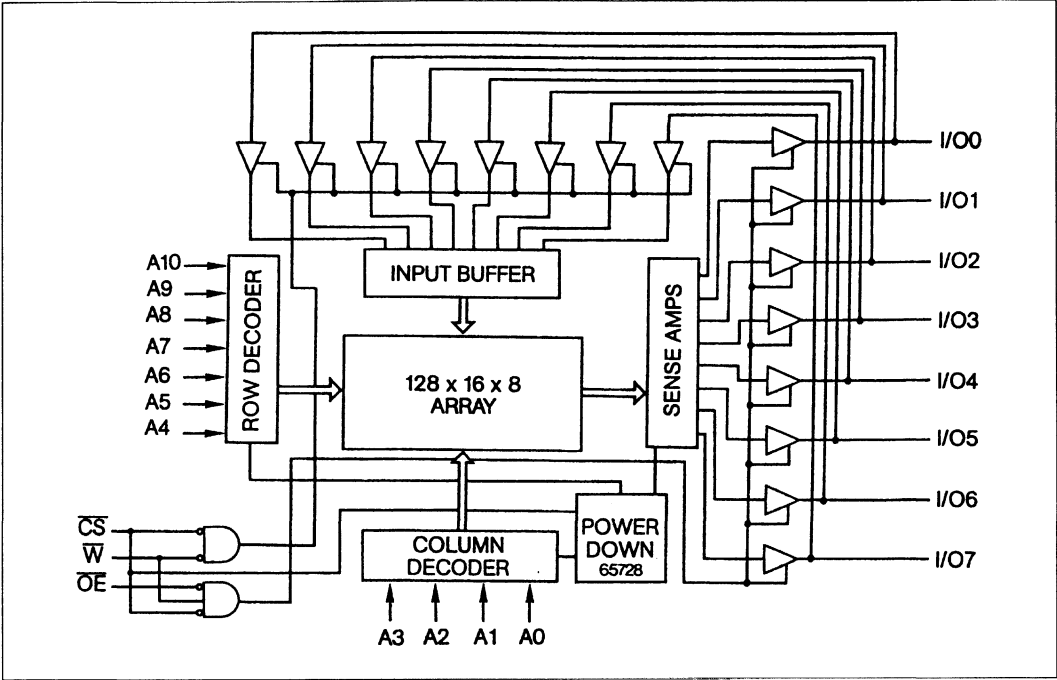
### Pinout LCC 32 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|           |                  |                 |                 |
|-----------|------------------|-----------------|-----------------|
| A0-A10    | : Address inputs | $\overline{CS}$ | : Chip Select   |
| I/O0-I/O7 | : Input/Output   | $\overline{OE}$ | : Output Enable |
| Vcc       | : Power          | $\overline{W}$  | : Write enable  |
| Gnd       | : Ground         |                 |                 |

TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|-----------------|----------------|---------|----------|----------|
| H               | X               | X              | Z       | Z        | Deselect |
| L               | L               | H              | Z       | Valid    | Read     |
| L               | H               | L              | Valid   | Z        | Write    |
| L               | L               | L              | Valid   | Z        | Write    |



**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$

Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$   
 Output current into outputs (low) :  $20\text{ mA}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.0     | —       | 5.5     | V    |

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

Note : 1.  $T_A = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{cc} = 5.0\text{ V}$ , these parameters are not tested.

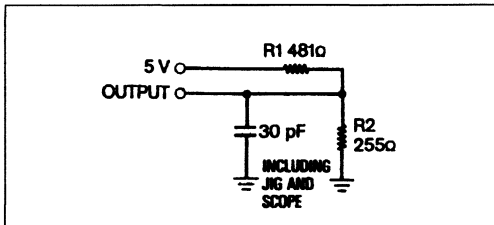
**AC TEST LOADS WAVEFORMS**

Fig. 1a.

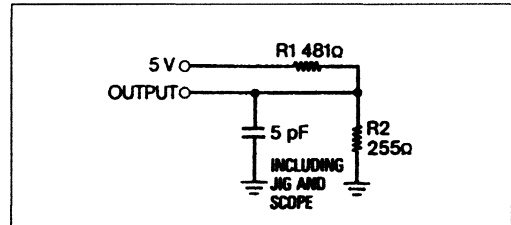


Fig. 1b.

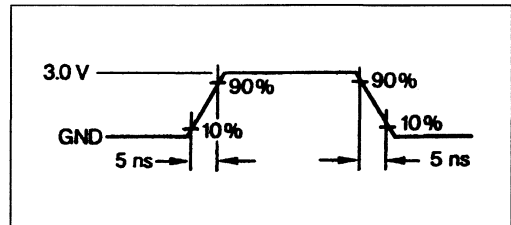
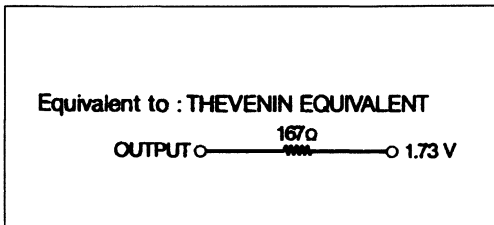


Figure 2 : All Input Pulses.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 40.0  | -       | 40.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 300.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (4) | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**Consumption for Commercial specification :**

| SYMBOL |     | PARAMETER                 | 65728<br>F-5 | 65728<br>H-5 | 65728<br>K-5 | 65728<br>M-5 | 65728<br>N-5 | UNIT | VALUE |
|--------|-----|---------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40           | 20           | 20           | 20           | 30           | mA   | max   |
| ICCOP  | (7) | Dynamic Operating current | 100          | 100          | 100          | 100          | 100          | mA   | max   |

**Consumption for Military specification :**

| SYMBOL |     | PARAMETER                 | 65728<br>H-2* | 65728<br>K-2 | 65728<br>M-2 | 65728<br>N-2 | UNIT | VALUE |
|--------|-----|---------------------------|---------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40            | 30           | 30           | 30           | mA   | max   |
| ICCOP  | (7) | Dynamic Operating current | 120           | 120          | 120          | 120          | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$ , a pull up resistor to  $V_{cc}$  on the  $\overline{CS}$  input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values above.
  7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .  
\* Preliminary specification.

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

**WRITE CYCLE : Commercial Specification**

| SYMBOL       | PARAMETER                               | 65728<br>F-5 | 65728<br>H-5 | 65728<br>K-5 | 65728<br>M-5 | 65728<br>N-5 | UNIT | VALUE |
|--------------|-----------------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV        | Write cycle time                        | 20           | 25           | 35           | 45           | 55           | ns   | min   |
| TAVWL        | Address set-up time                     | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH        | Address valid to end of write           | 20           | 20           | 30           | 40           | 50           | ns   | min   |
| TDVWH        | Data set-up time                        | 15           | 15           | 15           | 20           | 25           | ns   | min   |
| TELWH        | $\overline{\text{CS}}$ low to write end | 20           | 20           | 30           | 40           | 50           | ns   | min   |
| TWLQZ (8)    | Write low to high Z                     | 10           | 10           | 15           | 15           | 20           | ns   | max   |
| TWLWH        | Write pulse width                       | 15           | 20           | 20           | 20           | 30           | ns   | min   |
| TWHAX        | Address hold to end of write            | 0            | 2            | 2            | 2            | 2            | ns   | min   |
| TWHDX        | Data hold time                          | 0            | 0            | 0            | 0            | 5            | ns   | min   |
| TWHQX (8, 9) | Write high to low Z                     | 3            | 3            | 0            | 0            | 0            | ns   | min   |
| TEHAX        | Address hold end $\overline{\text{CS}}$ | 3            | 3            | 3            | 3            | 3            | ns   | min   |

Notes : 8. The data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.

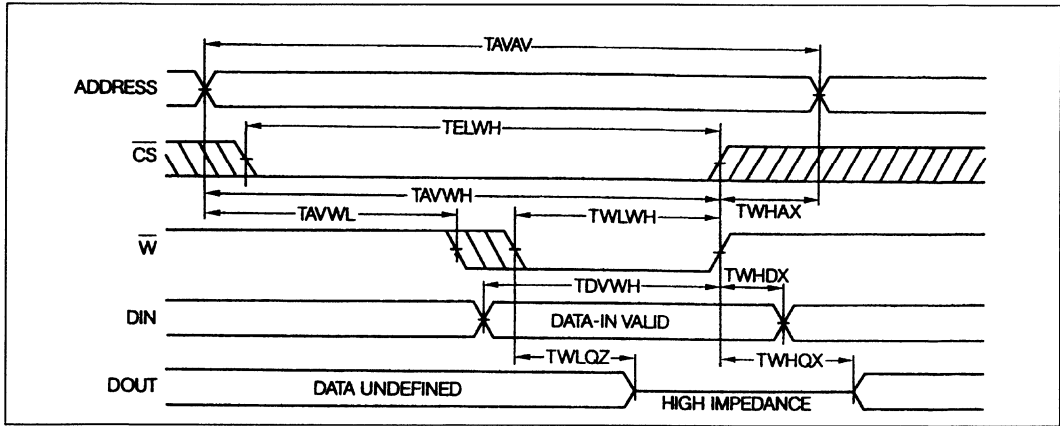
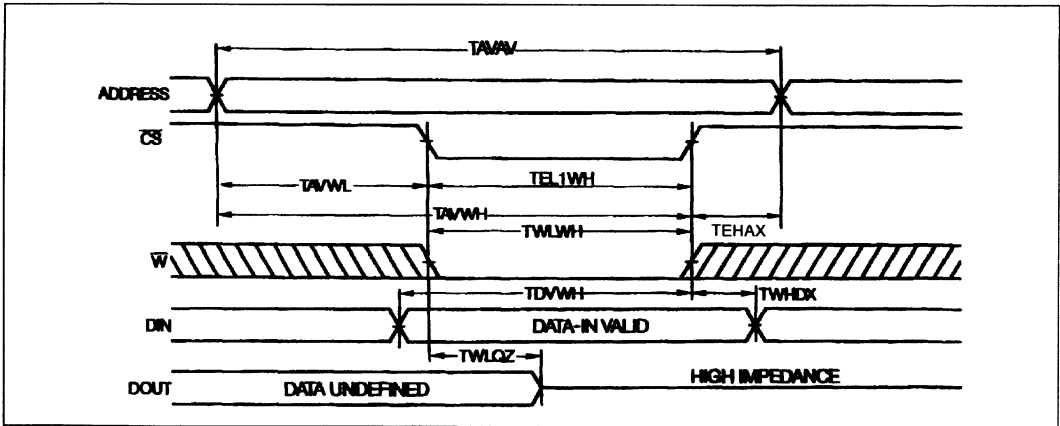
9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.

\* Preliminary specification.

**WRITE CYCLE : Military specification**

| SYMBOL    | PARAMETER                               | 65728<br>H-2* | 65728<br>K-2 | 65728<br>M-2 | 65728<br>N-2 | UNIT | VALUE |
|-----------|-----------------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write Cycle time                        | 25            | 35           | 45           | 55           | ns   | min   |
| TAVWL     | Address set-up time                     | 0             | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write           | 20            | 30           | 40           | 50           | ns   | min   |
| TDVWH     | Data set-up time                        | 10            | 15           | 20           | 25           | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end | 20            | 30           | 40           | 50           | ns   | min   |
| TWLQZ (8) | Write low to high Z                     | 10            | 15           | 15           | 20           | ns   | max   |
| TWLWH     | Write pulse width                       | 20            | 20           | 25           | 30           | ns   | min   |
| TWHAX     | Address hold to end of write            | 2             | 2            | 2            | 2            | ns   | min   |
| TWHDX     | Data hold time                          | 5             | 5            | 5            | 5            | ns   | min   |
| TEHAX     | Address hold end $\overline{\text{CS}}$ | 3             | 3            | 3            | 3            | ns   | min   |

\* Preliminary specification

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)

**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER                          | 65728<br>F-5 | 65728<br>H-5 | 65728<br>K-5 | 65728<br>M-5 | 65728<br>N-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 20           | 25           | 35           | 45           | 55           | ns   | min   |
| TAVQV  | Address access time                | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3            | 3            | 5            | 5            | 5            | ns   | min   |
| TELQV  | Chip-select access time            | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 3            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 12           | 12           | 15           | 20           | 20           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15           | 15           | 20           | 25           | 25           | ns   | max   |
| TGLQV  | Output enable access time          | 10           | 15           | 15           | 20           | 25           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 2            | 2            | 0            | 0            | 0            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 10           | 10           | 15           | 15           | 20           | ns   | max   |

**READ CYCLE : Military specification**

| SYMBOL | PARAMETER                          | 65728<br>H-2* | 65728<br>K-2 | 65728<br>M-2 | 65728<br>N-2 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 25            | 35           | 45           | 55           | ns   | min   |
| TAVQV  | Address access time                | 25            | 35           | 45           | 55           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 5            | 5            | 5            | ns   | min   |
| TELQV  | Chip-select access time            | 25            | 35           | 45           | 55           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3             | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 12            | 15           | 20           | 20           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20            | 20           | 25           | 25           | ns   | max   |
| TGLQV  | Output enable access time          | 12            | 15           | 20           | 25           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 0             | 0            | 0            | 0            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 12            | 15           | 15           | 20           | ns   | max   |

\* Preliminary specification



## ORDERING INFORMATION

| Package                          | Device type                   | Grade     | Level                    |
|----------------------------------|-------------------------------|-----------|--------------------------|
| HM1                              | 65728 (A)                     | H         | - 5 : R                  |
|                                  | 2 k x 8 high speed static RAM |           | Tape and Reel Service    |
| 0 - Chip form                    |                               | F = 20 ns | - 5 : Commercial         |
| 1 - Ceramic 24 pins              |                               | H = 25 ns | - 2 : Military           |
| 3 - Plastic 24 pins<br>300 mils  |                               | K = 35 ns | - 8 : Military with B.I. |
| 3E - Plastic 24 pins<br>600 mils |                               | M = 45 ns | (B.I. = Burn-In)         |
| 4 - LCC 32 pins                  |                               | N = 55 ns |                          |
| T - SOIC 24 pins                 |                               |           |                          |

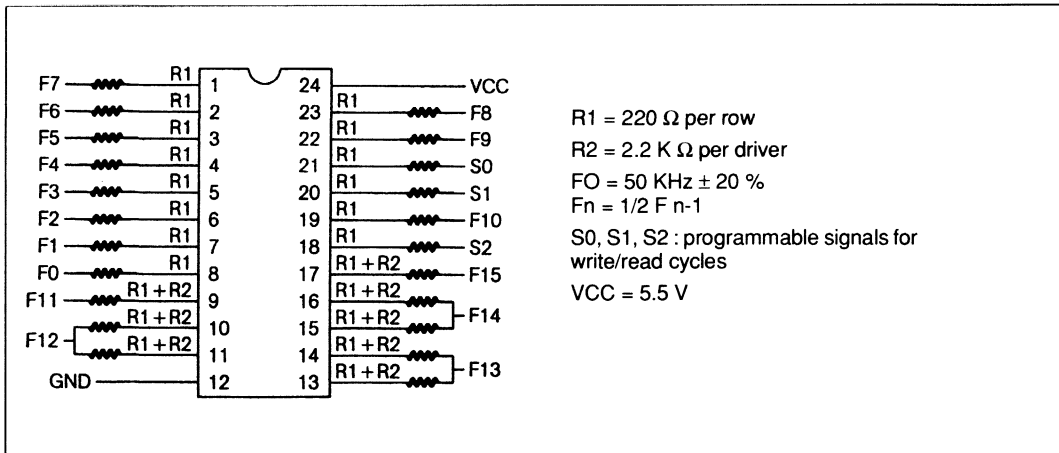
4

## PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

The reference are : Plastic DIL, 300 mils, 24 pins  
 Plastic DIL, 600 mils, 24 pins  
 SOIC DIL, 300 mils, 24 pins  
 Ceramic, 300 mils, 24 pins  
 LCC rectangular, 32 pins

## BURN-IN SCHEMATICS







# DATA SHEET

# HM 65787

## 64 K x 1 HIGH SPEED CMOS SRAM

### FEATURES

- FAST ACCESS TIME  
INDUSTRIAL/MILITARY : 25/35/45/55 ns  
COMMERCIAL : 15\*/20/25/35/45 ns
- LOW POWER CONSUMPTION  
ACTIVE : 320 mW (typ)  
STANDBY : 75 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

### DESCRIPTION

The HM 65787 is a high speed CMOS static RAM organized as 65536 x 1 bit. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.

The HM 65787 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by

60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

All inputs and outputs of the HM 65787 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65787 is processed following the test methods of MIL STD 883C.

### PACKAGES

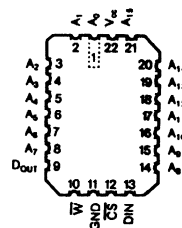
Plastic 300 mils, 22 pins, DIL.  
Ceramic 300 mils, 22 pins, DIL.  
Tape and Reel Service

SOIC & SOJ 300 mils, 24 pins.  
LCC\* 22 pins.

Pinout DIL 22/24 pins (top view)

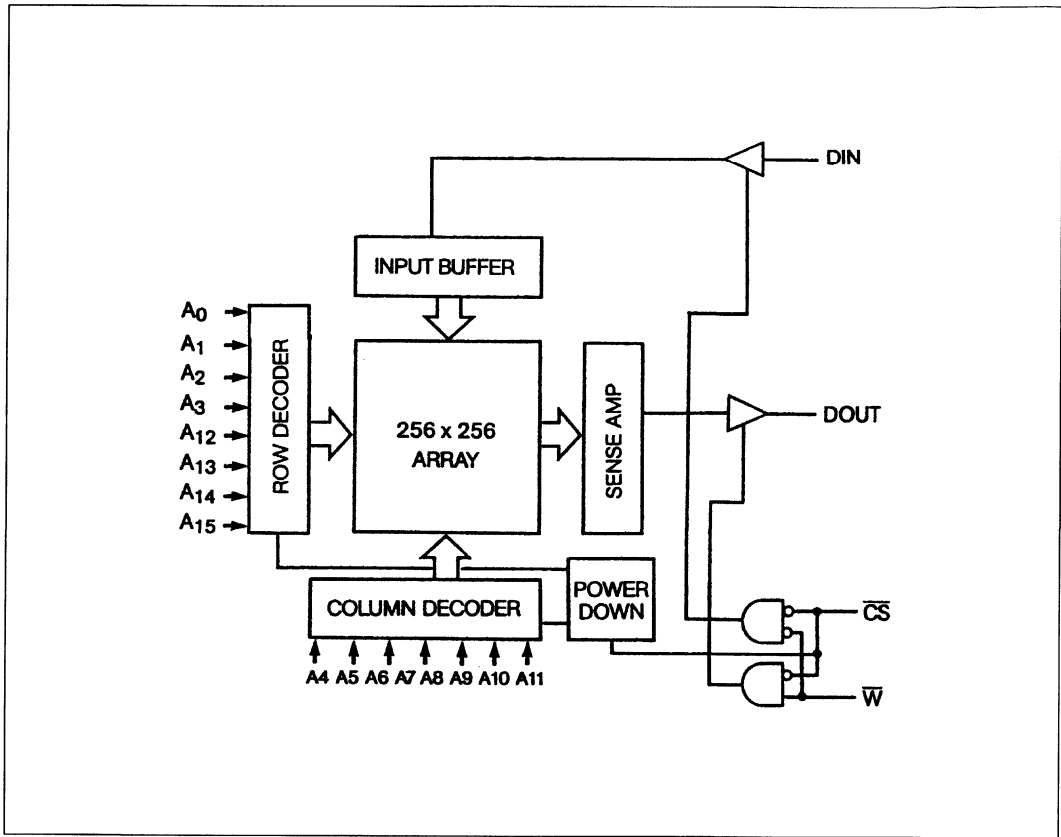
|      |    |    |     |      |    |    |     |
|------|----|----|-----|------|----|----|-----|
| A0   | 1  | 22 | VCC | A0   | 1  | 24 | VCC |
| A1   | 2  | 21 | A15 | A1   | 2  | 23 | A15 |
| A2   | 3  | 20 | A14 | A2   | 3  | 22 | A14 |
| A3   | 4  | 19 | A13 | A3   | 4  | 21 | A13 |
| A4   | 5  | 18 | A12 | A4   | 5  | 20 | A12 |
| A5   | 6  | 17 | A11 | A5   | 6  | 19 | NC  |
| A6   | 7  | 16 | A10 | NC   | 7  | 18 | A11 |
| A7   | 8  | 15 | A9  | A6   | 8  | 17 | A10 |
| Dout | 9  | 14 | A8  | A7   | 9  | 16 | A9  |
| W    | 10 | 13 | Din | Dout | 10 | 15 | A8  |
| GND  | 11 | 12 | CS  | W    | 11 | 14 | Din |
|      |    |    |     | GND  | 12 | 13 | CS  |

Pinout LCC 22 pins (top view)

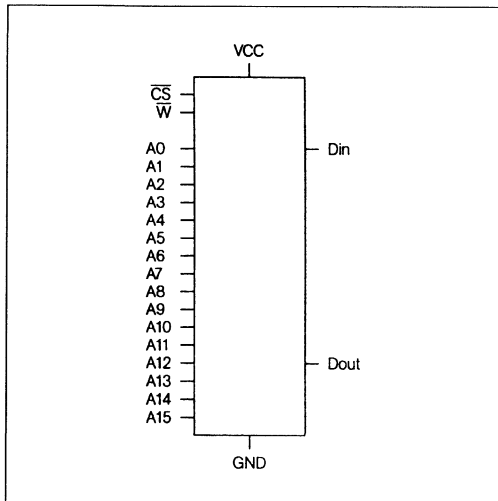


\* Preliminary

## BLOCK DIAGRAM



## LOGIC SYMBOL



## PIN NAMES

|                 |                  |                |                |
|-----------------|------------------|----------------|----------------|
| A0-A15          | : Address inputs | $\overline{W}$ | : Write enable |
| Din             | : Input          | Vcc            | : Power        |
| Dout            | : Output         | GND            | : Ground       |
| $\overline{CS}$ | : Chip select    |                |                |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V  
DC input voltage : - 0.3 V to + 7.0 V  
DC output voltage in high Z state : - 0.5 V to + 7.0 V  
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA  
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

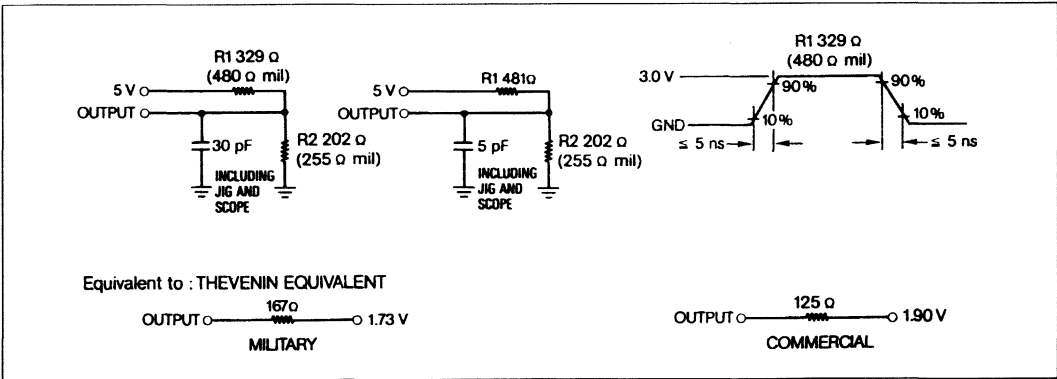
| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| VCC       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | 5.5     | V    |

CAPACITANCE

| PARAMETER | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|------------------------|---------|---------|---------|------|
| Cin       | (1) Input capacitance  | -       | -       | 5       | pF   |
| Cout      | (1) Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C, f = 1 MHz, VCC = 5.0 V.

AC TEST LOADS AND WAVEFORMS



**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       |         |

**Note :** 2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.  
 3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
 4.  $V_{cc} \min$ ,  $I_{OL} = 12.0 \text{ mA}$  (commercial)  $8.0 \text{ mA}$  (military).  
 5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**Consumption for Commercial specification :**

| SYMBOL |     | PARAMETER                 | 65787<br>E*-5 | 65787<br>F-5 | 65787<br>H-5 | 65787<br>K-5 | 65787<br>M-5 | UNIT | VALUE |
|--------|-----|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40            | 40           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 90            | 80           | 80           | 80           | 80           | mA   | max   |

**Consumption for Military specification :**

| SYMBOL |     | PARAMETER                 | 65787<br>F*-9/-2 | 65787<br>H-9/-2 | 65787<br>K-9/-2 | 65787<br>N-9/2 | 65787<br>N-9/-2 | UNIT | VALUE |
|--------|-----|---------------------------|------------------|-----------------|-----------------|----------------|-----------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40               | 40              | 30              | 30             | 30              | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20               | 20              | 20              | 20             | 20              | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 90               | 80              | 80              | 80             | 80              | mA   | max   |

**Notes :** 6.  $\overline{CS} \geq V_{IH}$  min duty cycle = 100 %, a pull-up resistor to  $V_{cc}$  on the CS input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values given above.  
 7.  $CS = V_{cc} - 0.3 \text{ V}$   $I_{out} = 0 \text{ mA}$ .  
 8.  $V_{cc} \max$ , Output current =  $0 \text{ mA}$ ,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .  
 \* Preliminary

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

**WRITE CYCLE : Commercial specification**

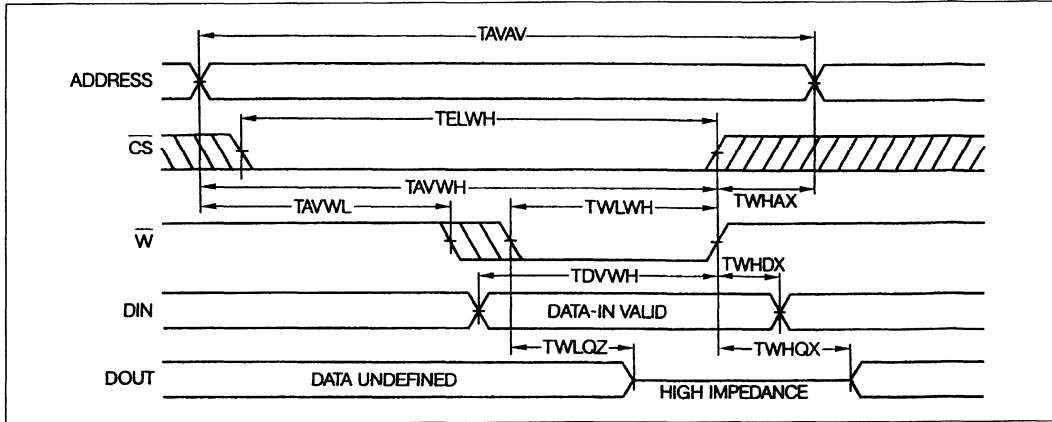
| SYMBOL    | PARAMETER                        | 65787<br>E*-5 | 65787<br>F-5 | 65787<br>H-5 | 65787<br>K-5 | 65787<br>M-5 | UNIT | VALUE |
|-----------|----------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                 | 15            | 20           | 20           | 25           | 40           | ns   | min   |
| TAVWL     | Address set-up time              | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write    | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TDVWH     | Data set-up time                 | 10            | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 7             | 7            | 7            | 10           | 15           | ns   | max   |
| TWLWH     | Write pulse width                | 12            | 15           | 15           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold from end of write   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX     | Data hold time                   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5             | 5            | 5            | 5            | 5            | ns   | min   |

4

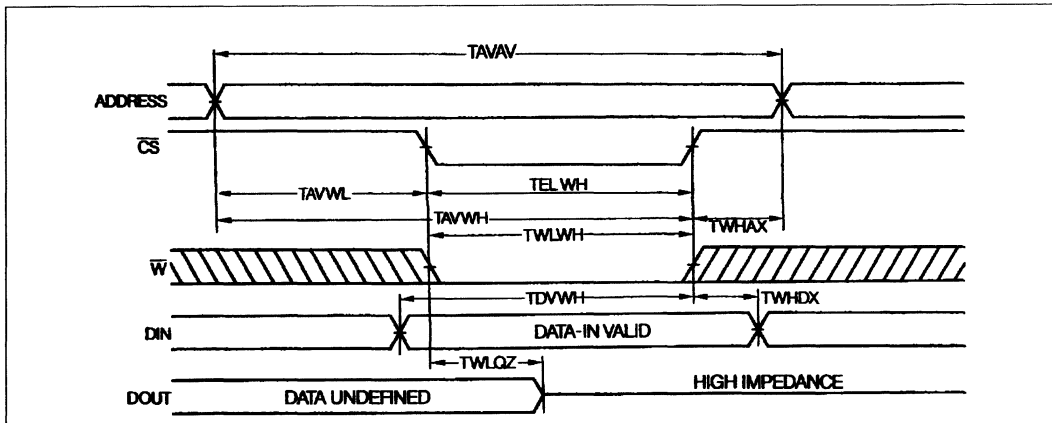
**WRITE CYCLE : Industrial and Military specification**

| SYMBOL    | PARAMETER                        | 65787<br>F*-9/-2 | 65787<br>H-9/-2 | 65787<br>K-9/-2 | 65787<br>M-9/-2 | 65787<br>N-9/-2 | UNIT | VALUE |
|-----------|----------------------------------|------------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV     | Write cycle time                 | 20               | 20              | 25              | 40              | 50              | ns   | min   |
| TAVWL     | Address set-up time              | 0                | 0               | 0               | 0               | 0               | ns   | min   |
| TAVWH     | Address valid to end of write    | 15               | 20              | 25              | 30              | 40              | ns   | min   |
| TDVWH     | Data set-up time                 | 10               | 10              | 15              | 15              | 20              | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 15               | 20              | 25              | 30              | 40              | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 7                | 7               | 10              | 15              | 15              | ns   | max   |
| TWLWH     | Write pulse width                | 15               | 15              | 20              | 20              | 25              | ns   | min   |
| TWHAX     | Address hold from end of write   | 0                | 0               | 0               | 0               | 0               | ns   | min   |
| TWHDX     | Data hold time                   | 0                | 0               | 0               | 0               | 0               | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5                | 5               | 5               | 5               | 5               | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.  
 \* Preliminary.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)

4

WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)

**READ CYCLE : Commercial specification**

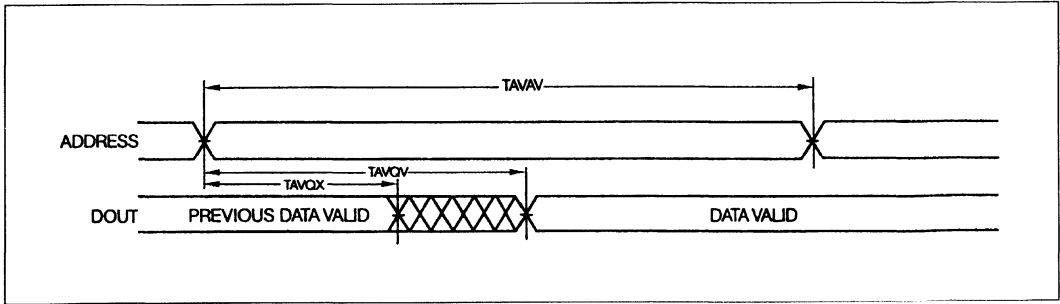
| SYMBOL | PARAMETER                          | 65787<br>E*-5 | 65787<br>F-5 | 65787<br>H-5 | 65787<br>K-5 | 65787<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 15            | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5             | 5            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8             | 8            | 10           | 15           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15            | 20           | 20           | 20           | 25           | ns   | max   |

**READ CYCLE : Commercial specification**

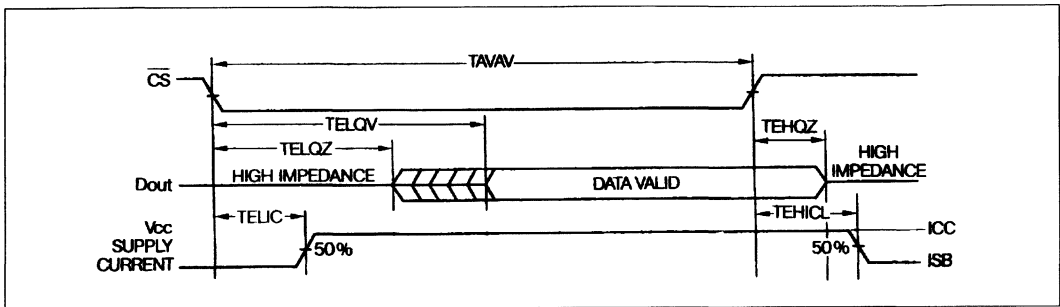
| SYMBOL | PARAMETER                          | 65787<br>F*-9/-2 | 65787<br>H-9/-2 | 65787<br>K-9/-2 | 65787<br>M-9/-2 | 65787<br>N-9/-2 | UNIT | VALUE |
|--------|------------------------------------|------------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV  | Read cycle time                    | 20               | 25              | 35              | 45              | 55              | ns   | min   |
| TAVQV  | Address access time                | 20               | 25              | 35              | 45              | 55              | ns   | min   |
| TAVQX  | Address valid to low Z             | 3                | 3               | 3               | 3               | 3               | ns   | min   |
| TELQV  | Chip-select access time            | 20               | 25              | 35              | 45              | 55              | ns   | min   |
| TELQX  | $\overline{CS}$ low to low Z       | 5                | 5               | 5               | 5               | 5               | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8                | 10              | 15              | 15              | 20              | ns   | min   |
| TELIC  | $\overline{CS}$ low to power up    | 0                | 0               | 0               | 0               | 0               | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20               | 20              | 20              | 25              | 30              | ns   | min   |

\* Preliminary.

## READ CYCLE nb 1



## READ CYCLE nb 2





### ORDERING INFORMATION

| Package             | Device                         | Grade      | Type Level               |
|---------------------|--------------------------------|------------|--------------------------|
| HM1                 | 65787                          | F          | - 5 : R                  |
|                     | 64 k x 1 high speed static RAM |            | Tape and Reel Service    |
| 0 - Chip form       |                                | E* = 15 ns | - 5 : Commercial.        |
| 1 - Ceramic 22 pins |                                | F = 20 ns  | - 9 : Industrial         |
| 3 - Plastic 22 pins |                                | H = 25 ns  | - 2 : Military           |
| 4 - LCC 22 pins     |                                | K = 35 ns  | - 8 : Military with B.I. |
| T - SOIC 24 pins    |                                | M = 45 ns  | (B.I. = Burn-In)         |
| U - SOJ 24 pins     |                                | N = 55 ns  |                          |

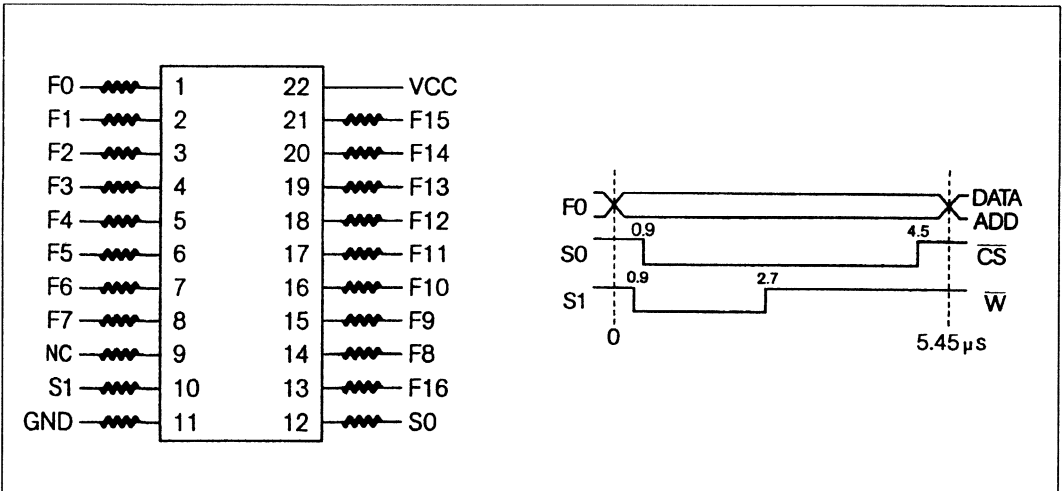
\* Preliminary

### PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins.  
SOIC DIL, 300 mils, 24 pins.  
Ceramic, 300 mils, 22 pins.  
LCC rectangular, 22 pins.

### BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)

R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %

F<sub>n</sub> = 1/2 F<sub>n-1</sub>

S0 & S1 : programmable signals for write/read cycles

NC = Non connected.





September 1990

## DATA SHEET

## HM 65788

# 16 K x 4 HIGH SPEED CMOS SRAM

## FEATURES

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 25/35/45/55 ns  
COMMERCIAL : 15\*/20/25/35/45 ns
- **LOW POWER CONSUMPTION**  
ACTIVE : 267 mW (typ)  
STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**  
- 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

4

## DESCRIPTION

The HM 65788 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.

The HM 65788 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by

60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

All inputs and outputs of the HM 65788 are TTL compatible and operate from single 5 V supply thus simplifying system design.

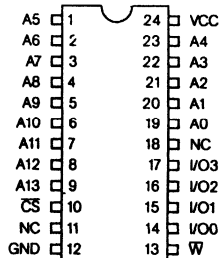
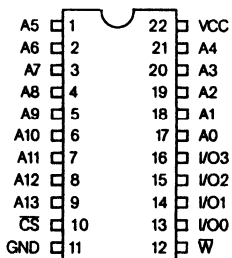
The HM 65788 is processed following the test methods of MIL STD 883C.

## PACKAGES

Plastic 300 mils, 22 pins, DIL.  
Ceramic 300 mils, 22 pins, DIL.  
Tape and Reel Service.

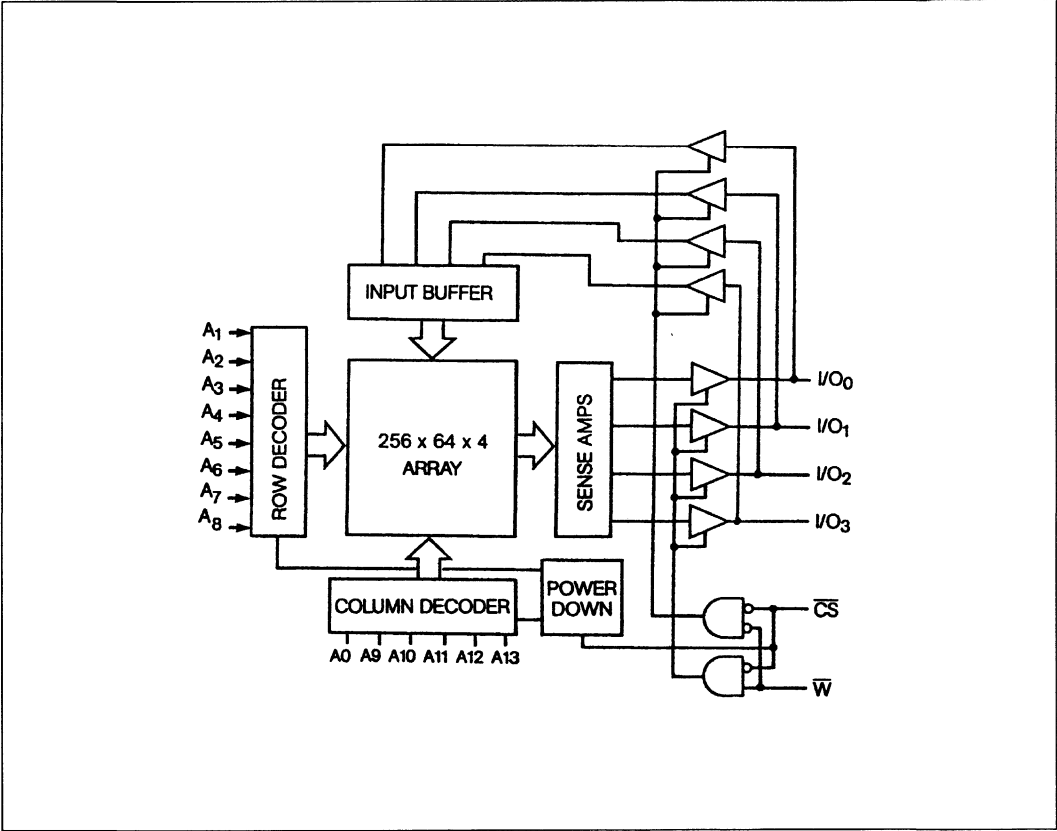
SOIC & SOJ 300 mils, 24 pins

Pinout DIL 22/24 pins (top view)

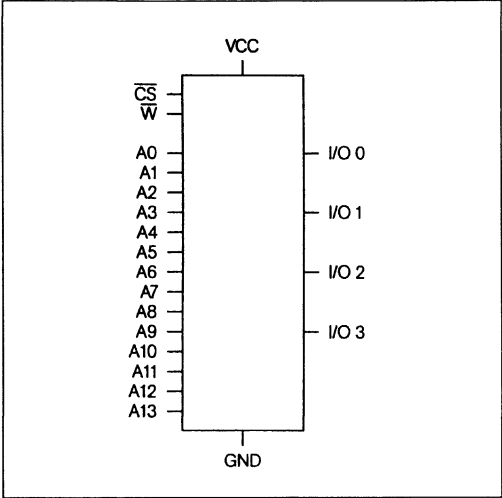


\* preliminary

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

|                            |                               |
|----------------------------|-------------------------------|
| A0-A13 : Address inputs    | GND : Ground                  |
| I/O0-I/O3 : Inputs/Outputs | $\overline{CS}$ : Chip select |
| VCC : Power                | $\overline{W}$ : Write enable |

TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|----------------|---------|----------|----------|
| H               | X              | Z       | Z        | Deselect |
| L               | H              | Z       | Valid    | Read     |
| L               | L              | Valid   | Z        | Write    |

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-0.3\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$   
 Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$

Output current into outputs (low) :  $20\text{ mA}$   
 Electro static discharge voltage :  $> 2001\text{ V (MIL STD 883C method 3015.2)}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $5\text{ V} \pm 10\%$ | $-40^{\circ}\text{C to }+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

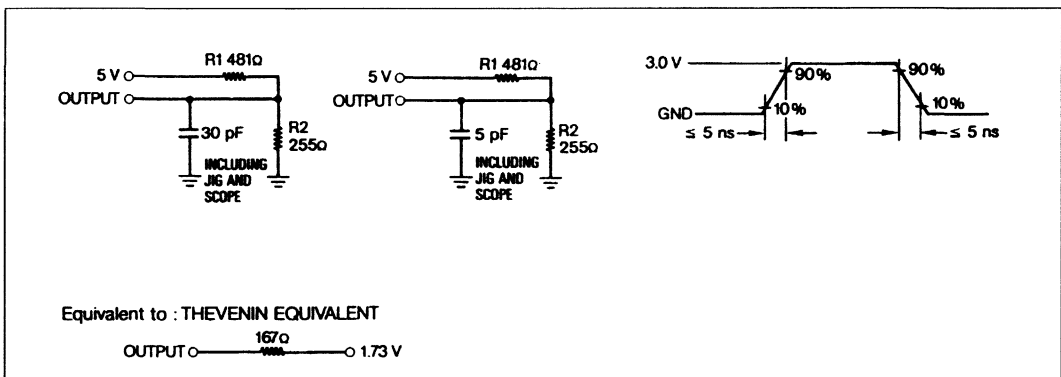
**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | —       | VCC     | V    |

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

Note : 1. TA =  $25^{\circ}\text{C}$ , f =  $1\text{ MHz}$ , VCC =  $5.0\text{ V}$ , these parameters are not 100 % tested.

**AC TEST LOADS AND WAVEFORMS**

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|-----|------------------------------|---------|---------|---------|------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | μA   |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | μA   |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA   |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V    |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       |      |

**Notes :**

2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

**Consumption for Commercial specification (- 5) :**

| SYMBOL     | PARAMETER                 | 65787<br>E*-5 | 65788<br>F-5 | 65788<br>H-5 | 65788<br>K-5 | 65788<br>M-5 | UNIT | VALUE |
|------------|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 40            | 40           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 115           | 100          | 100          | 100          | 100          | mA   | max   |

**Consumption for Industrial (- 9) and Military specification (- 2) :**

| SYMBOL     | PARAMETER                 | 65788<br>H-9/2 | 65788<br>K-9/2 | 65788<br>M-9/2 | 65788<br>N-9/-2 | UNIT | VALUE |
|------------|---------------------------|----------------|----------------|----------------|-----------------|------|-------|
| ICCSB (6)  | Standby supply current    | 40             | 30             | 30             | 30              | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 20             | 20             | 20             | 20              | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 100            | 100            | 100            | 100             | mA   | max   |

**Notes :**

6.  $\overline{CS} \geq V_{IH}$  min duty cycle = 100 %, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7.  $\overline{CS} = V_{cc} - 0.3\text{ V}$  Iout = 0 mA.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.  
\* Preliminary.

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30

## WRITE CYCLE : Commercial specification

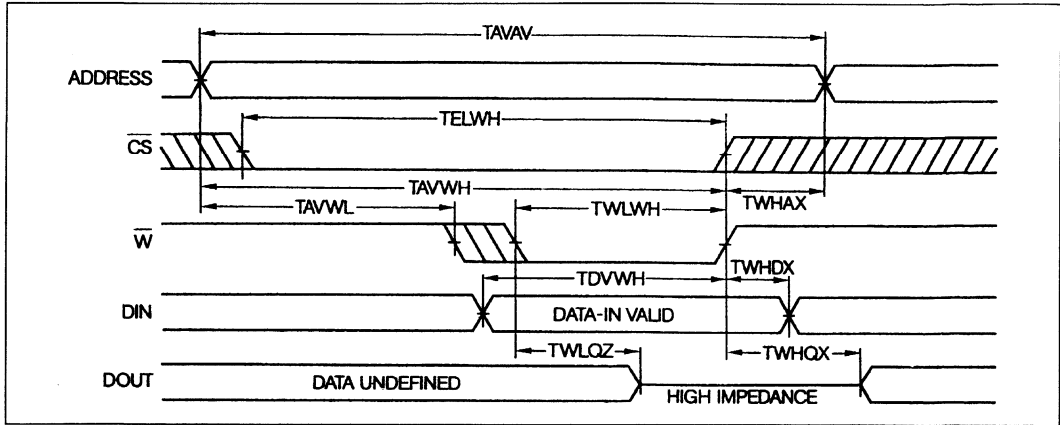
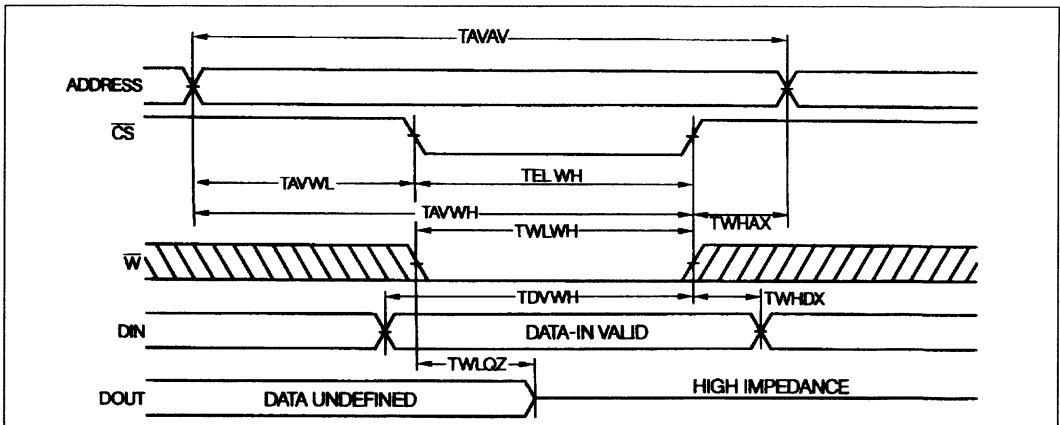
| SYMBOL    | PARAMETER                        | 65788<br>E-5* | 65788<br>F-5 | 65788<br>H-5 | 65788<br>K-5 | 65788<br>M-5 | UNIT | VALUE |
|-----------|----------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                 | 15            | 20           | 20           | 25           | 40           | ns   | min   |
| TAVWL     | Address set-up time              | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write    | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TDVWH     | Data set-up time                 | 10            | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TWLQZ (9) | Write low to high Z              | 7             | 7            | 7            | 10           | 15           | ns   | max   |
| TWLWH     | Write pulse width                | 12            | 15           | 15           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold from end of write   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX     | Data hold time                   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5             | 5            | 5            | 5            | 5            | ns   | min   |

## WRITE CYCLE : Industrial and Military specification

| SYMBOL    | PARAMETER                        | 65788<br>H-9/2 | 65788<br>K-9/2 | 65788<br>M-9/2 | 65788<br>N-9/2 | UNIT | VALUE |
|-----------|----------------------------------|----------------|----------------|----------------|----------------|------|-------|
| TAVAV     | Write cycle time                 | 20             | 25             | 40             | 50             | ns   | min   |
| TAVWL     | Address set-up time              | 0              | 0              | 0              | 0              | ns   | min   |
| TAVWH     | Address valid to end of write    | 20             | 25             | 30             | 40             | ns   | min   |
| TDVWH     | Data set-up time                 | 10             | 15             | 15             | 20             | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 20             | 25             | 30             | 40             | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 7              | 10             | 15             | 25             | ns   | max   |
| TWLWH     | Write pulse width                | 15             | 20             | 20             | 30             | ns   | min   |
| TWHAX     | Address hold from end of write   | 0              | 0              | 0              | 0              | ns   | min   |
| TWHDX     | Data hold time                   | 0              | 0              | 0              | 0              | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5              | 5              | 5              | 5              | ns   | min   |

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

\* Preliminary.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 9)WRITE CYCLE 2  $\overline{CS}$  CONTROLLED (note 9)

**Note :** 9. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.



**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER                          | 65788<br>E-5* | 65788<br>F-5 | 65788<br>H-5 | 65788<br>K-5 | 65788<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 15            | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8             | 8            | 10           | 15           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15            | 20           | 20           | 20           | 25           | ns   | max   |

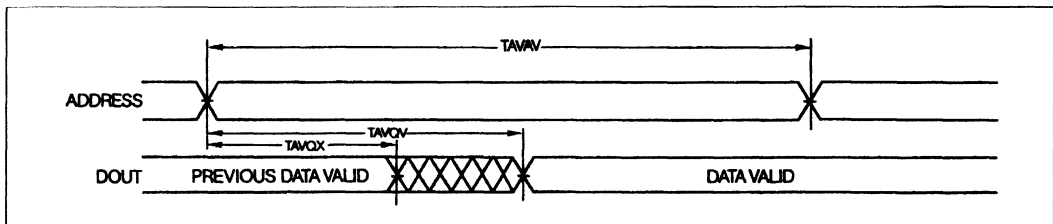
\* Preliminary.

**READ CYCLE : Industrial and Military specification**

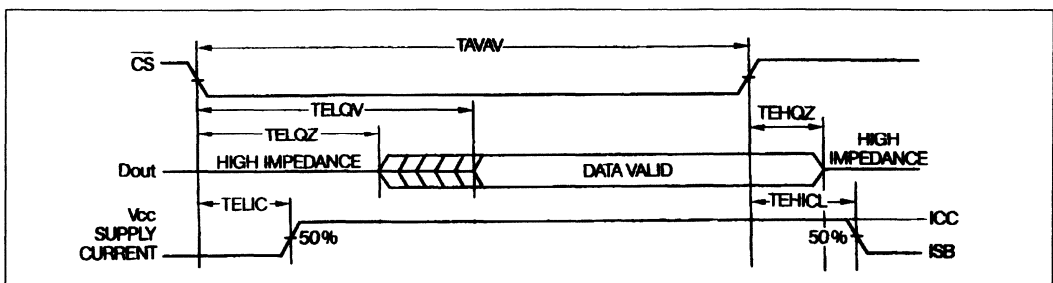
| SYMBOL | PARAMETER                          | 65788<br>H-9/2 | 65788<br>K-9/2 | 65788<br>M-9/2 | 65788<br>N-9/2 | UNIT | VALUE |
|--------|------------------------------------|----------------|----------------|----------------|----------------|------|-------|
| TAVAV  | Read cycle time                    | 25             | 35             | 45             | 55             | ns   | min   |
| TAVQV  | Address access time                | 25             | 35             | 45             | 55             | ns   | max   |
| TAVQX  | Address valid to low Z             | 3              | 3              | 3              | 3              | ns   | min   |
| TELQV  | Chip-select access time            | 25             | 35             | 45             | 55             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5              | 5              | 5              | 5              | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 10             | 15             | 15             | 20             | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0              | 0              | 0              | 0              | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20             | 20             | 25             | 25             | ns   | max   |

4

**READ CYCLE nb 1**



**READ CYCLE nb 2**



# ORDERING INFORMATION

| Package                   | Device type                    | Grade      | Level                    |                       |
|---------------------------|--------------------------------|------------|--------------------------|-----------------------|
| HM1                       | 65788                          | F          | - 5 : R                  | Tape and Reel Service |
|                           | 16 k x 4 High speed static RAM |            | - 5 : Commercial         |                       |
|                           |                                |            | - 9 : Industrial         |                       |
|                           |                                |            | - 2 : Military           |                       |
|                           |                                |            | - 8 : Military with B.I. | (B.I. = Burn-In)      |
| 0 - Chip form             |                                | E* = 15 ns |                          |                       |
| 1 - Ceramic 22 pins       |                                | F = 20 ns  |                          |                       |
| 3 - Plastic 22 pins       |                                | H = 25 ns  |                          |                       |
| T - SOIC 24 pins 300 mils |                                | K = 35 ns  |                          |                       |
| U - SOJ 24 pins 300 mils  |                                | M = 45 ns  |                          |                       |
|                           |                                | N = 55 ns  |                          |                       |

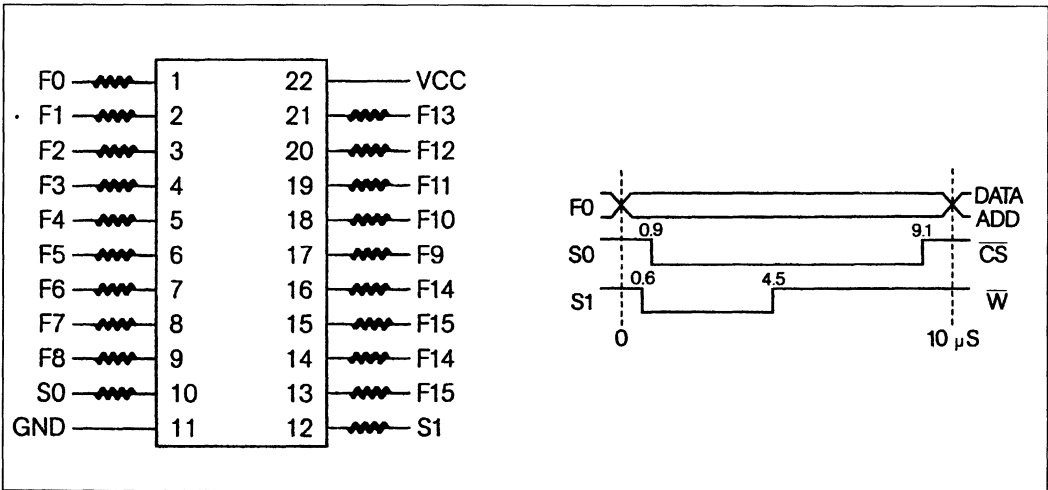
## 4

### PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins  
SOIC DIL, 300 mils, 24 pins  
Ceramic, 300 mils, 22 pins  
LCC rectangular, 22 pins

### BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)

R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %

F<sub>n</sub> = 1/2 F<sub>n-1</sub>

S0 & S1 : programmable signals for write/read cycles

NC = Non connected.

## DATA SHEET

## HM 65789

# 16 K x 4 HIGH SPEED CMOS SRAM WITH OUTPUT ENABLE

## FEATURES

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 25\*/35/45/55 ns  
COMMERCIAL : 15\*/20/25/35/45 ns
- **LOW POWER CONSUMPTION**  
ACTIVE : 267 mW (typ)  
STANDBY : 75 mW (typ)
- **WIDE TEMPERATURE RANGE :**  
- 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **OUTPUT ENABLE**

4

## DESCRIPTION

The HM 65789 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.

The HM 65789 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65789 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65789 is processed following the test methods of MIL STD 883C.

## PACKAGES

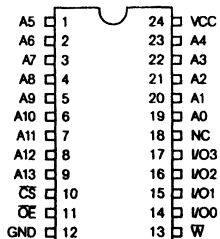
Plastic 300 mils, 24 pins, DIL.

SOIC &amp; SOJ 300 mils, 24 pins.

Ceramic 300 mils, 24 pins, DIL.

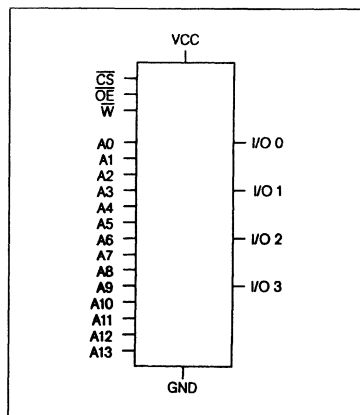
Tape and Reel Service.

### Pinout DIL 24 pins (top view)

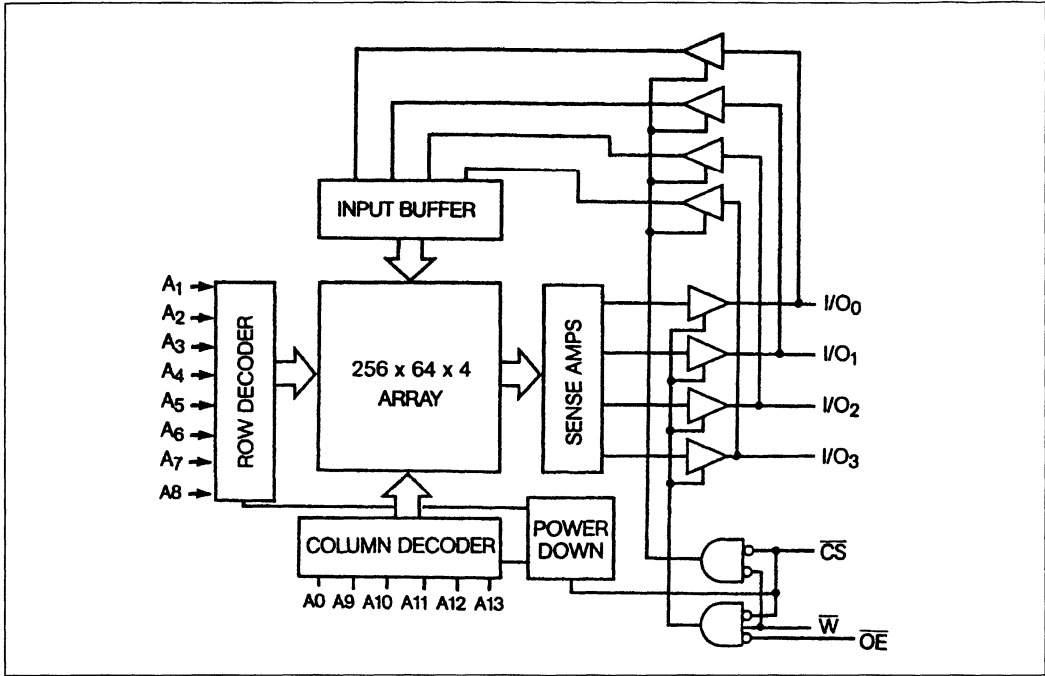


\* preliminary

## LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN NAMES

|                            |                                 |
|----------------------------|---------------------------------|
| A0-A13 : Address inputs    | $\overline{CS}$ : Chip-select   |
| I/O0-I/O3 : Inputs/Outputs | $\overline{OE}$ : Output enable |
| VCC : Power                | $\overline{W}$ : Write enable   |
| GND : Ground               |                                 |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|-----------------|----------------|---------|----------|----------|
| H               | X               | X              | Z       | Z        | Deselect |
| L               | L               | H              | Z       | Valid    | Read     |
| L               | X               | L              | Valid   | Z        | Write    |

L = low - H = high - X = H or L-Z = high impedance.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$   
 Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$

Output current into outputs (low) :  $20\text{ mA}$   
 Electro static discharge voltage :  $> 2001\text{ V}$  (MIL STD 883C method 3015.2)

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |
| Industrial | (- 9) | $5\text{ V} \pm 10\%$ | $-40^{\circ}\text{C to }+85^{\circ}\text{C}$  |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | —       | VCC     | V    |

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

Note : 1.  $T_A = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{cc} = 5.0\text{ V}$ , these parameters are not 100 % tested.

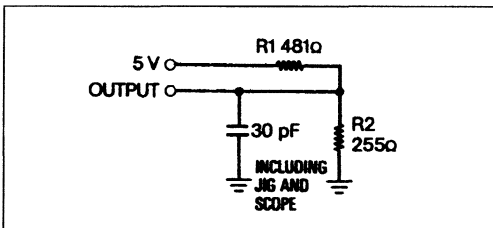
**AC TEST LOADS WAVEFORMS**

Fig. 1a.

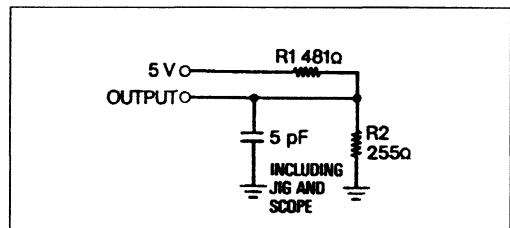


Fig. 1b.

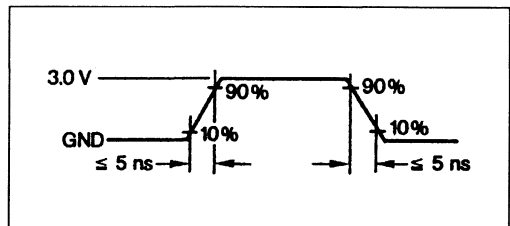
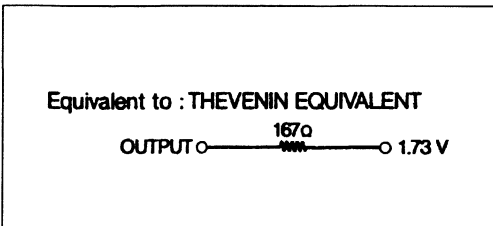


Fig. 2.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|-----|------------------------------|---------|---------|---------|------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | μA   |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | μA   |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA   |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V    |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       |      |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**Consumption for Commercial specification :**

| SYMBOL     | PARAMETER                 | 65789<br>E*-5 | 65789<br>F-5 | 65789<br>H-5 | 65789<br>K-5 | 65789<br>M-5 | UNIT | VALUE |
|------------|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 40            | 40           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 115           | 100          | 100          | 100          | 100          | mA   | max   |

**Consumption for Military specification :**

| SYMBOL     | PARAMETER                 | 65789<br>H-9/-2 | 65789<br>K-9/-2 | 65789<br>M-9/2 | 65789<br>N-9/-2 | UNIT | VALUE |
|------------|---------------------------|-----------------|-----------------|----------------|-----------------|------|-------|
| ICCSB (6)  | Standby supply current    | 40              | 30              | 30             | 30              | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 20              | 20              | 20             | 20              | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 100             | 100             | 100            | 100             | mA   | max   |

- Notes :**
6.  $CS \geq V_{IH}$ , min duty cycle = 100 %. A pull-up resistor to  $V_{cc}$  on the CS input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed values above.
  7.  $CS = V_{cc} - 0.3 \text{ V}$   $I_{out} = 0 \text{ mA}$ .
  8.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or Gnd.  
\* Preliminary.

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

**WRITE CYCLE : Commercial specification**

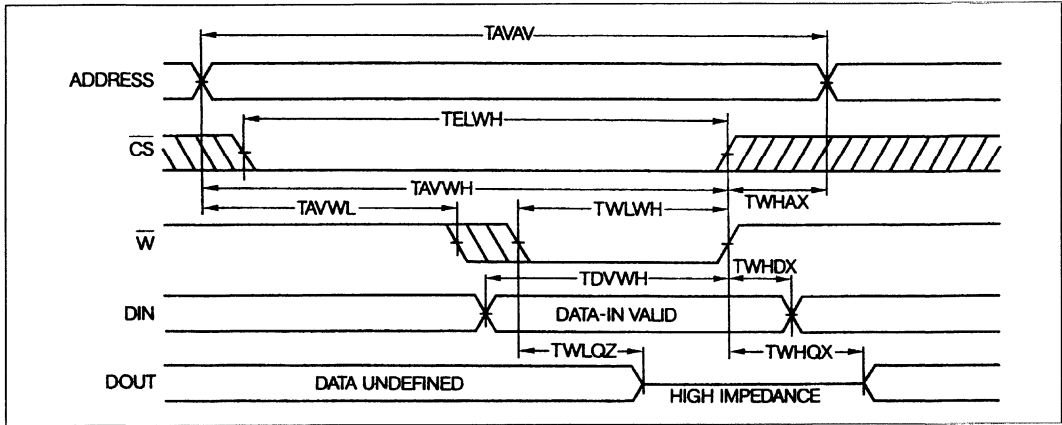
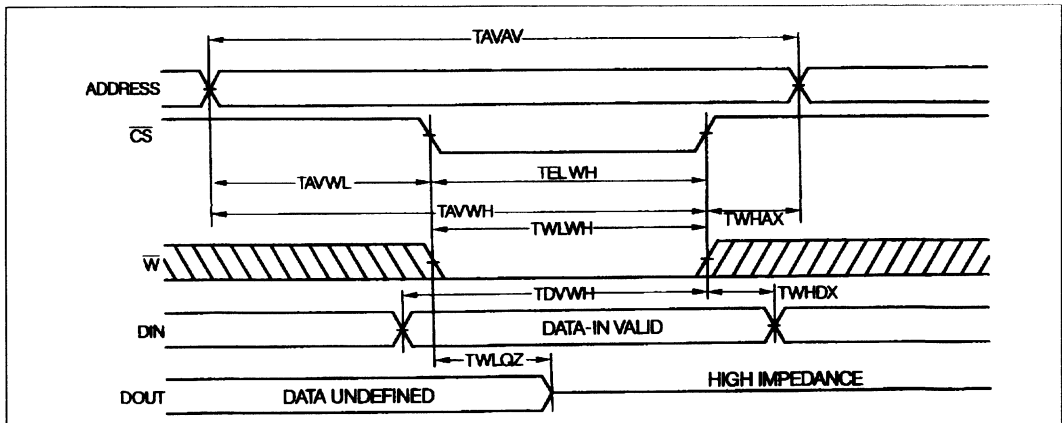
| SYMBOL    | PARAMETER                      | 65789<br>E-5* | 65789<br>F-5 | 65789<br>H-5 | 65789<br>K-5 | 65789<br>M-5 | UNIT | VALUE |
|-----------|--------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time               | 15            | 20           | 20           | 25           | 40           | ns   | min   |
| TAVWL     | Address set-up time            | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write  | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TDVWH     | Data set-up time               | 10            | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH     | CS low to write end            | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TWLQZ     | Write low to high Z            | 7             | 7            | 7            | 10           | 15           | ns   | max   |
| TWLWH     | Write pulse width              | 12            | 15           | 15           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold from end of write | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX     | Data hold time                 | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z            | 5             | 5            | 5            | 5            | 5            | ns   | min   |

4

**WRITE CYCLE : Military specification**

| SYMBOL    | PARAMETER                      | 65789<br>H-9/-2 | 65789<br>K-9/-2 | 65789<br>M-9/-2 | UNIT | VALUE |
|-----------|--------------------------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV     | Write cycle time               | 20              | 25              | 40              | ns   | min   |
| TAVWL     | Address set-up time            | 0               | 0               | 0               | ns   | min   |
| TAVWH     | Address valid to end of write  | 20              | 25              | 30              | ns   | min   |
| TDVWH     | Data set-up time               | 10              | 15              | 15              | ns   | min   |
| TELWH     | CS low to write end            | 20              | 25              | 30              | ns   | min   |
| TWLQZ (8) | Write low to high Z            | 7               | 10              | 15              | ns   | max   |
| TWLWH     | Write pulse width              | 15              | 20              | 25              | ns   | min   |
| TWHAX     | Address hold from end of write | 0               | 0               | 0               | ns   | min   |
| TWHDX     | Data hold time                 | 0               | 0               | 0               | ns   | min   |
| TWHQX (8) | Write high to low Z            | 5               | 5               | 5               | ns   | min   |

**Note :** 9. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.  
 \* Preliminary.

WRITE CYCLE 1 :  $\overline{W}$  CONTROLLED (note 9)WRITE CYCLE 2 :  $\overline{CS}$  CONTROLLED (note 9)

**Note :** 10. The internal write of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
Data-out will be high impedance if  $\overline{OE} = \text{VIH}$ .



**READ CYCLE : Commercial specification**

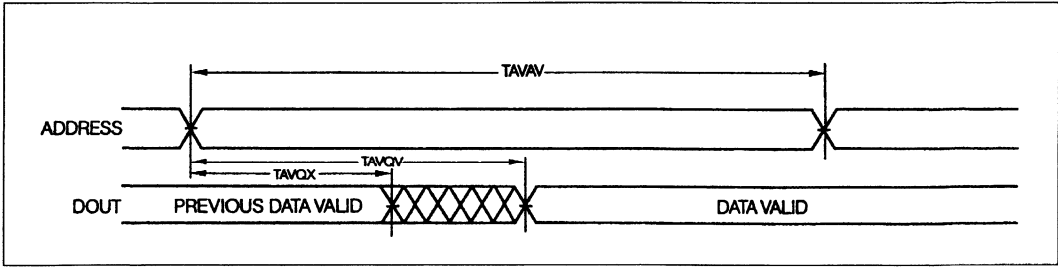
| SYMBOL | PARAMETER                          | 65789<br>E-5* | 65789<br>F-5 | 65789<br>H-5 | 65789<br>K-5 | 65789<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Read cycle time                    | 15            | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8             | 8            | 10           | 15           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TGLQV  | Output enable access time          | 10            | 10           | 12           | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 8             | 8            | 10           | 12           | 15           | ns   | max   |

**READ CYCLE : Military specification**

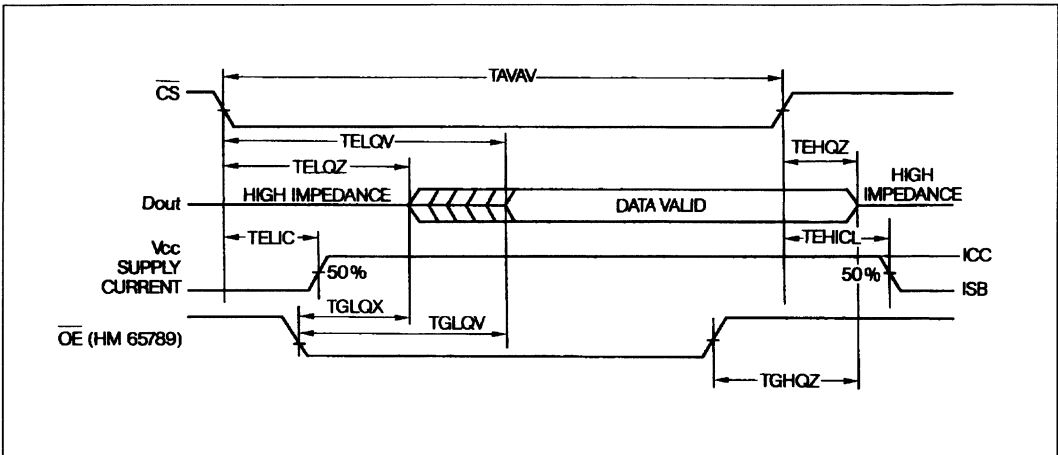
| SYMBOL | PARAMETER                          | 65789<br>H-9/2 | 65789<br>K9/2 | 65789<br>M9/2 | 65789<br>N-9/2 | UNIT | VALUE |
|--------|------------------------------------|----------------|---------------|---------------|----------------|------|-------|
| TAVAV  | Read cycle time                    | 25             | 35            | 45            | 55             | ns   | min   |
| TAVQV  | Address access time                | 25             | 35            | 45            | 55             | ns   | max   |
| TAVQX  | Address valid to low Z             | 3              | 3             | 3             | 3              | ns   | min   |
| TELQV  | Chip-select access time            | 25             | 35            | 45            | 55             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3              | 3             | 3             | 3              | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 10             | 15            | 15            | 15             | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0              | 0             | 0             | 0              | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 25             | 35            | 45            | 55             | ns   | max   |
| TGLQV  | Output enable access time          | 12             | 15            | 20            | 25             | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3              | 3             | 3             | 3              | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 10             | 12            | 15            | 15             | ns   | max   |

\* Preliminary.

## READ CYCLE nb 1 : (notes 10, 11)



## READ CYCLE nb 2 : (notes 10, 12)



Notes : 11.  $\overline{W}$  is high for read cycle.

12. Device is continuously selected,  $\overline{CS} = \text{VIL}$ ,  $\overline{OE} = \text{VIL}$ .

13. Address valid prior or coincident with  $\overline{CS}$  transition low.

# ORDERING INFORMATION

| Package                   | Device type                                       | Grade      | Level                    |                       |
|---------------------------|---------------------------------------------------|------------|--------------------------|-----------------------|
| HM1                       | 65767                                             | F          | - 5 : R                  |                       |
|                           | 16 k x 4 high speed static RAM with output enable |            |                          | Tape and Reel Service |
|                           |                                                   |            | - 5 : Commercial         |                       |
|                           |                                                   |            | - 9 : Industrial         |                       |
|                           |                                                   |            | - 2 : Military           |                       |
|                           |                                                   |            | - 8 : Military with B.I. |                       |
|                           |                                                   |            | (B.I. = Burn-In)         |                       |
| 0 - Chip form             |                                                   | E* = 15 ns |                          |                       |
| 1 - Ceramic 24 pins       |                                                   | F = 20 ns  |                          |                       |
| 3 - Plastic 24 pins       |                                                   | H = 25 ns  |                          |                       |
| T - SOIC 24 pins 300 mils |                                                   | K = 35 ns  |                          |                       |
| U - SOJ 24 pins 300 mils  |                                                   | M = 45 ns  |                          |                       |
|                           |                                                   | N = 55 ns  |                          |                       |

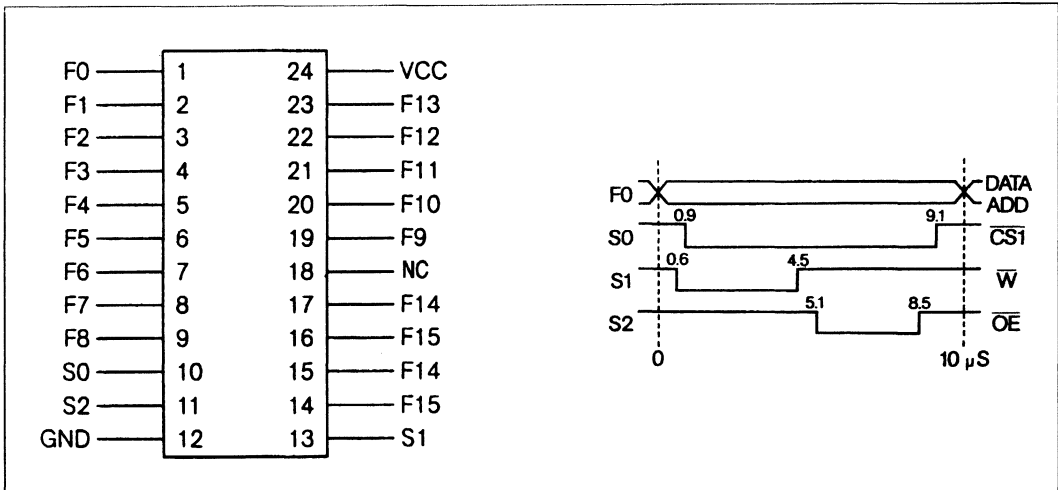
\* Preliminary

## PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins  
SOIC DIL, 300 mils, 24 pins  
Ceramic, 300 mils, 24 pins  
LCC rectangular, 28 pins

## BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)

R = 1 KΩ per pin

FO = 50 KHz ± 20 %

F<sub>n</sub> = 1/2 F<sub>n</sub> − 1

S0 to S2 = programmable signals for write/read cycles

NC = Non connected



## DATA SHEET

## HM 65790

# 16 K x 4 HIGH SPEED CMOS SRAM SEPARATE I/O

## FEATURES

- FAST ACCESS TIME  
MILITARY : 25\*/35/45 ns (max)  
COMMERCIAL : 15\*/20/25/35/45 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 267 mW (typ)  
STANDBY : 75 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN  
2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY
- SEPARATE INPUTS/OUTPUTS
- OUTPUT ENABLE

4

## DESCRIPTION

The HM 65790 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.

The HM 65790 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip select (CS1, CS2), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65790 are TTL compatible and operate from single 5 V supply thus simplifying system design.

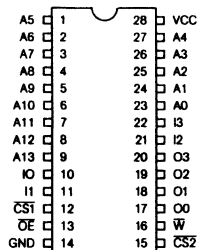
The HM 65790 is processed following the test methods of MIL STD 883C.

## PACKAGES

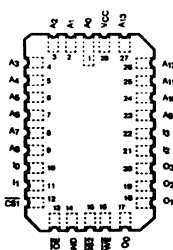
Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins, DIL.  
Tape and Reel Service.

SOIC 300 mils, 28 pins  
LCC 28 pins.

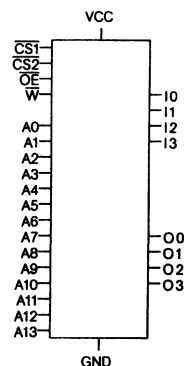
## Pinout DIL 28 pins (top view)



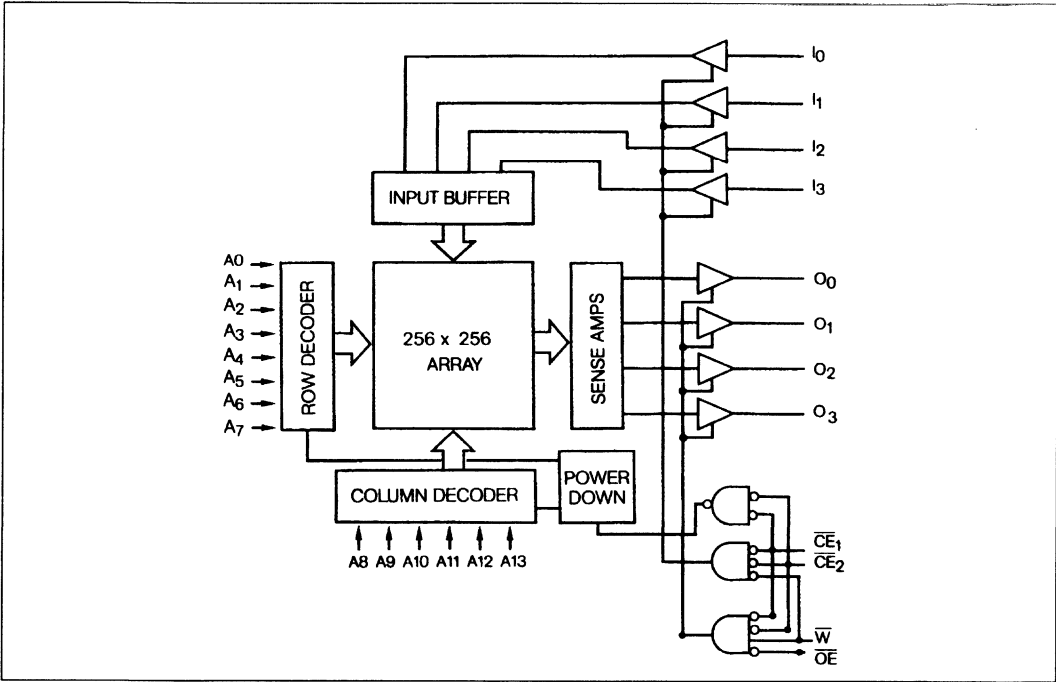
## Pinout LCC 28 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                         |                                                 |
|-------------------------|-------------------------------------------------|
| A0-A13 : Address inputs | $\overline{CS1}$ $\overline{CS2}$ : Chip Select |
| I0-I3 : Inputs          | $\overline{OE}$ : Output enable                 |
| O0-O3 : Outputs         | $\overline{W}$ : Write enable                   |
| VCC : Power             | GND : Ground                                    |

TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|-----------------|----------------|---------|----------|----------|
| H               | X               | X              | Z       | Z        | Deselect |
| L               | L               | H              | Z       | Valid    | Read     |
| L               | X               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }+7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$   
 Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$

Output current into outputs (low) : 20 mA  
 Electro static discharge voltage :  $> 2001\text{ V (MIL STD 883C method 3015.2)}$

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | —       | VCC     | V    |

4

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

Note : 1.  $T_A = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{cc} = 5.0\text{ V}$ , these parameters are not 100 % tested.

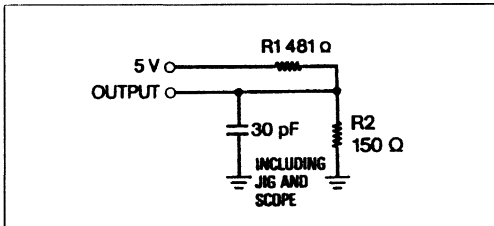
**AC TEST LOADS WAVEFORMS**

Fig. 1a.

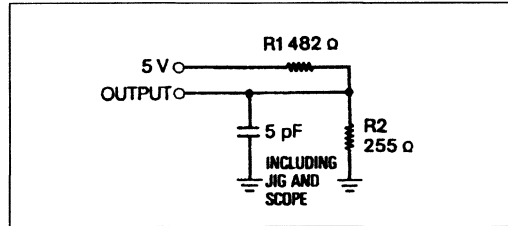


Fig. 1b.

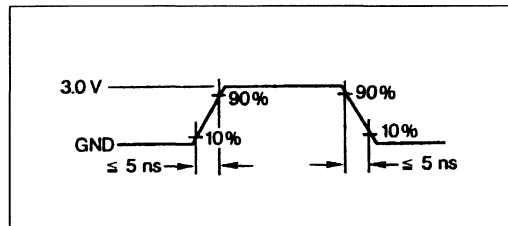
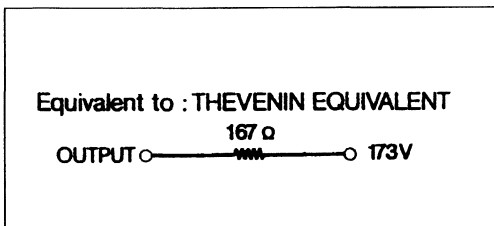


Fig. 2.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
  3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4. Vcc min, IOL = 8.0 mA.
  5. Vcc min, IOH = - 4.0 mA.

**Consumption for Commercial specification :**

| SYMBOL |     | PARAMETER                 | 65790<br>E*-5 | 65790<br>F-5 | 65790<br>H-5 | 65790<br>K-5 | 65790<br>M-5 | UNIT | VALUE |
|--------|-----|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40            | 40           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 115           | 100          | 100          | 100          | 100          | mA   | max   |

**Consumption for Military specification :**

| SYMBOL |     | PARAMETER                 | 65790<br>H-2 | 65790<br>K-2 | 65790<br>M-2 | UNIT | VALUE |
|--------|-----|---------------------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40           | 30           | 30           | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 100          | 100          | 100          | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$  min duty cycle = 100 %, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
  7.  $\overline{CS} = V_{cc} - 0.3 V$  Iout = 0 mA.
  8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
- \* Preliminary.



## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input risqce : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

## WRITE CYCLE : Commercial specification

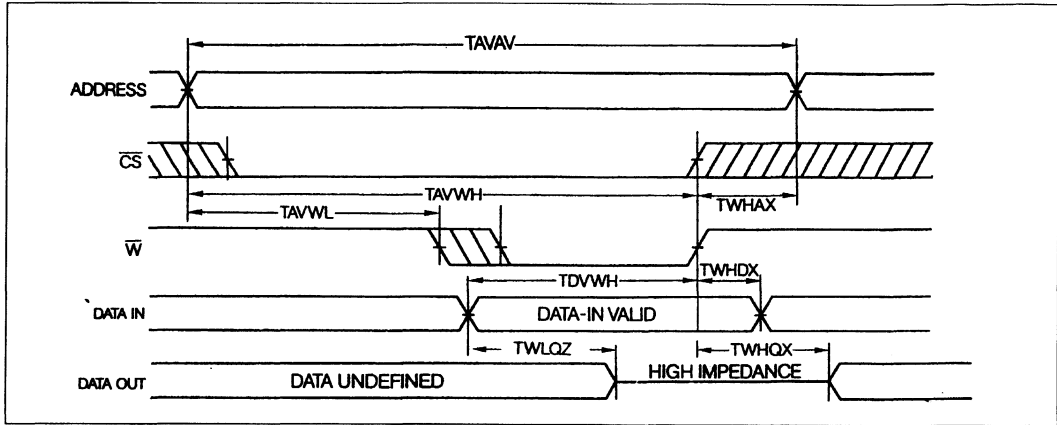
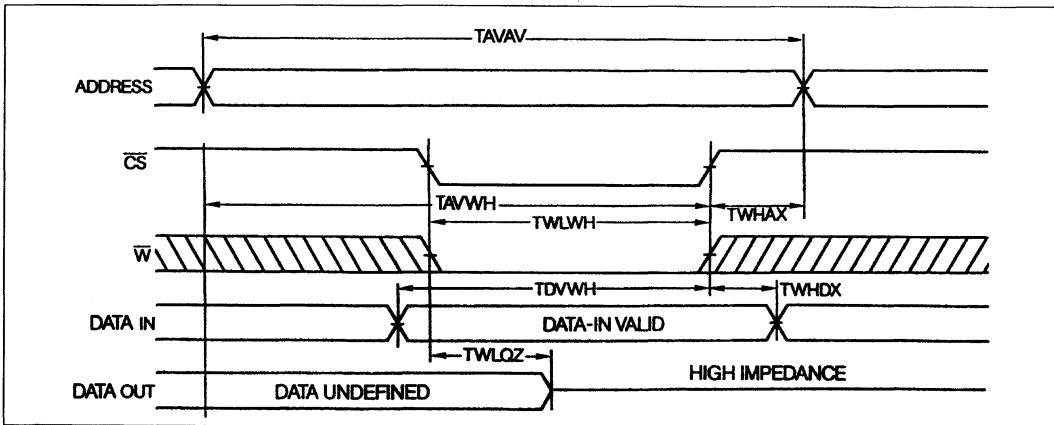
| SYMBOL    | PARAMETER                        | 65790<br>E-5* | 65790<br>F-5 | 65790<br>H-5 | 65790<br>K-5 | 65790<br>M-5 | UNIT | VALUE |
|-----------|----------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                 | 15            | 20           | 20           | 25           | 40           | ns   | min   |
| TAVWL     | Address set-up time              | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address valid to end of write    | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TDVWH     | Data set-up time                 | 10            | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TWLQZ     | Write low to high Z              | 7             | 7            | 7            | 10           | 15           | ns   | max   |
| TWLWH     | Write pulse width                | 12            | 15           | 15           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold from end of write   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX     | Data hold time                   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5             | 5            | 5            | 5            | 5            | ns   | min   |

4

## WRITE CYCLE : Military specification

| SYMBOL    | PARAMETER                        | 65790<br>H-2 | 65790<br>K-2 | 65790<br>M-2 | UNIT | VALUE |
|-----------|----------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV     | Write cycle time                 | 20           | 25           | 40           | ns   | min   |
| TAVWL     | Address set-up time              | 0            | 0            | 0            | ns   | min   |
| TAVWH     | Address Valid to end of write    | 20           | 25           | 30           | ns   | min   |
| TDVWH     | Data set-up time                 | 10           | 15           | 15           | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 20           | 25           | 30           | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 7            | 10           | 15           | ns   | max   |
| TWLWH     | Write pulse width                | 15           | 20           | 20           | ns   | min   |
| TWHAX     | Address hold from end of write   | 0            | 0            | 0            | ns   | min   |
| TWHDX     | Data hold time                   | 0            | 0            | 0            | ns   | min   |
| TWHQX (8) | Write high to low Z              | 5            | 5            | 5            | ns   | min   |

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.  
 \* Preliminary.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)

**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER                          | 65790<br>E*-5 | 65790<br>F-5 | 65790<br>H-5 | 65790<br>K-5 | 65790<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 15            | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5             | 5            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8             | 8            | 10           | 12           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15            | 20           | 20           | 20           | 25           | ns   | max   |
| TGLQV  | Output enable access time          | 10            | 10           | 12           | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TGHQX  | $\overline{OE}$ high to high Z     | 15            | 15           | 15           | 15           | 15           | ns   | max   |

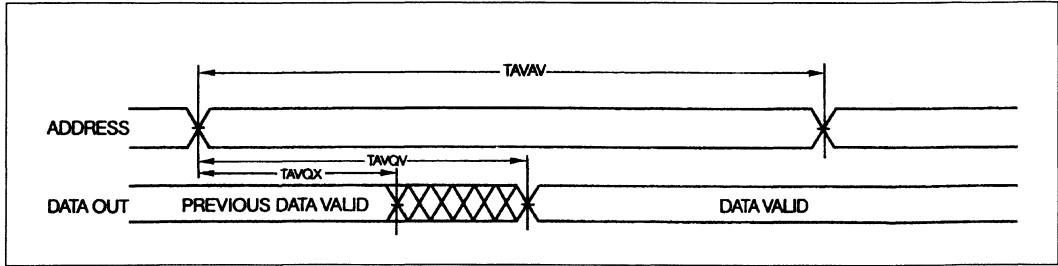
4

**READ CYCLE : Military specification**

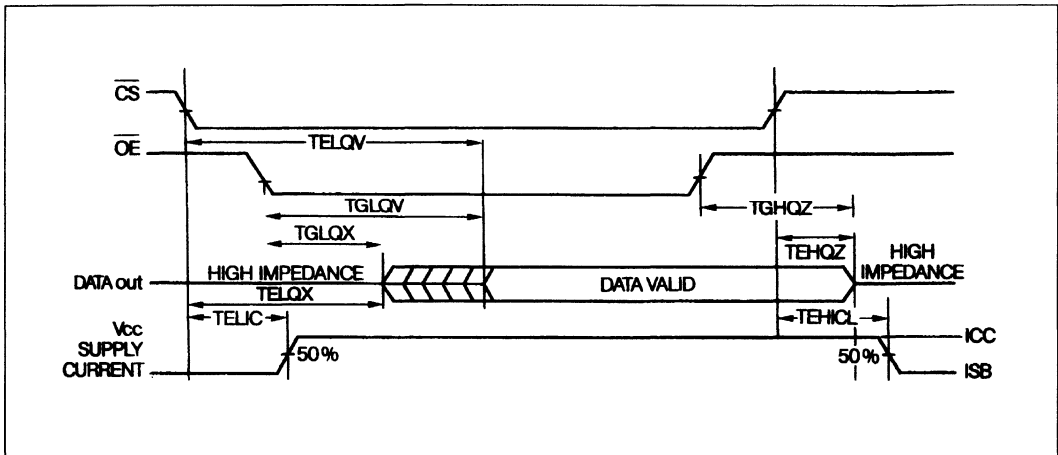
| SYMBOL | PARAMETER                          | 65790<br>H*-2 | 65790<br>K-2 | 65790<br>M-2 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 25            | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 25            | 35           | 45           | ns   | max   |
| TAVQX  | Address valid to low Z             | 3             | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 25            | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5             | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 10            | 12           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20            | 20           | 25           | ns   | max   |
| TGLQV  | Output enable access time          | 12            | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3             | 3            | 3            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 10            | 12           | 15           | ns   | min   |

\* Preliminary

## READ CYCLE nb 1 (notes 9, 10)



## READ CYCLE nb 2 (notes 9, 11)



Notes : 9.  $\overline{W}$  is high for read cycle.

10. Device is continuously selected,  $\overline{CS}_1, \overline{CS}_2 = \text{VIL}$ .

11. Address valid prior to or coincident with  $\overline{CS}_1, \overline{CS}_2$  transition low.

ORDERING INFORMATION

| Package                                                                                                                                                                      | Device type                                                                                        | Grade                                                                                                                                    | Level                                                                                                                                                                   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HM1                                                                                                                                                                          | 65790                                                                                              | H                                                                                                                                        | - 5                                                                                                                                                                     |
| <ul style="list-style-type: none"> <li>0 - Chip form</li> <li>1 - Ceramic 28 pins</li> <li>3 - Plastic 28 pins</li> <li>4 - LCC 28 pins</li> <li>T - SOIC 28 pins</li> </ul> | <ul style="list-style-type: none"> <li>16 k x 4 high speed static RAM with separate I/O</li> </ul> | <ul style="list-style-type: none"> <li>E* = 15 ns</li> <li>F = 20 ns</li> <li>H = 25 ns</li> <li>K = 35 ns</li> <li>M = 45 ns</li> </ul> | <ul style="list-style-type: none"> <li>- 5 : Commercial</li> <li>- 9 : Industrial</li> <li>- 2 : Military</li> <li>- 8 : Military with B.I. (B.I. = Burn-in)</li> </ul> |

\* Preliminary.

4

PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins  
 SOIC DIL, 300 mils, 28 pins  
 Ceramic, 300 mils, 28 pins  
 LCC rectangular, 32 pins



## DATA SHEET

## HM 65791

# 16 K x 4 HIGH SPEED CMOS SRAM SEPARATE I/O AND TRANSPARENT WRITE

## FEATURES

- FAST ACCESS TIME  
MILITARY : 20/35/45 ns (max)  
COMMERCIAL : 15\*/20/25/35/45 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 267 mW (typ)  
STANDBY : 75 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY
- SEPARATE INPUTS/OUTPUTS
- TRANSPARENT WRITE
- OUTPUT ENABLE

4

## DESCRIPTION

The HM 65791 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.

The HM 65791 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip select (CS1, CS2), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65791 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65791 is processed following the test methods of MIL STD 883C.

## PACKAGES

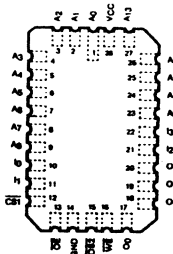
Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins, DIL.  
Tape and Reel Service.

LCC 28 pins.

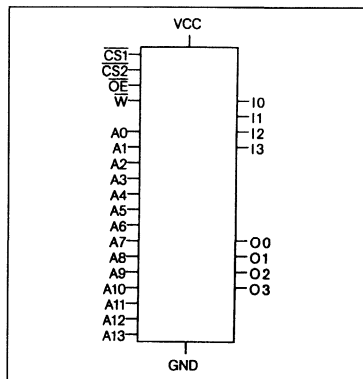
## Pinout DIL 28 pins (top view)

|     |    |    |     |
|-----|----|----|-----|
| A5  | 1  | 28 | VCC |
| A6  | 2  | 27 | A4  |
| A7  | 3  | 26 | A3  |
| A8  | 4  | 25 | A2  |
| A9  | 5  | 24 | A1  |
| A10 | 6  | 23 | A0  |
| A11 | 7  | 22 | I3  |
| A12 | 8  | 21 | I2  |
| A13 | 9  | 20 | O3  |
| I0  | 10 | 19 | O2  |
| I1  | 11 | 18 | O1  |
| CS1 | 12 | 17 | O0  |
| OE  | 13 | 16 | W   |
| GND | 14 | 15 | CS2 |

## Pinout LCC 28 pins (top view)

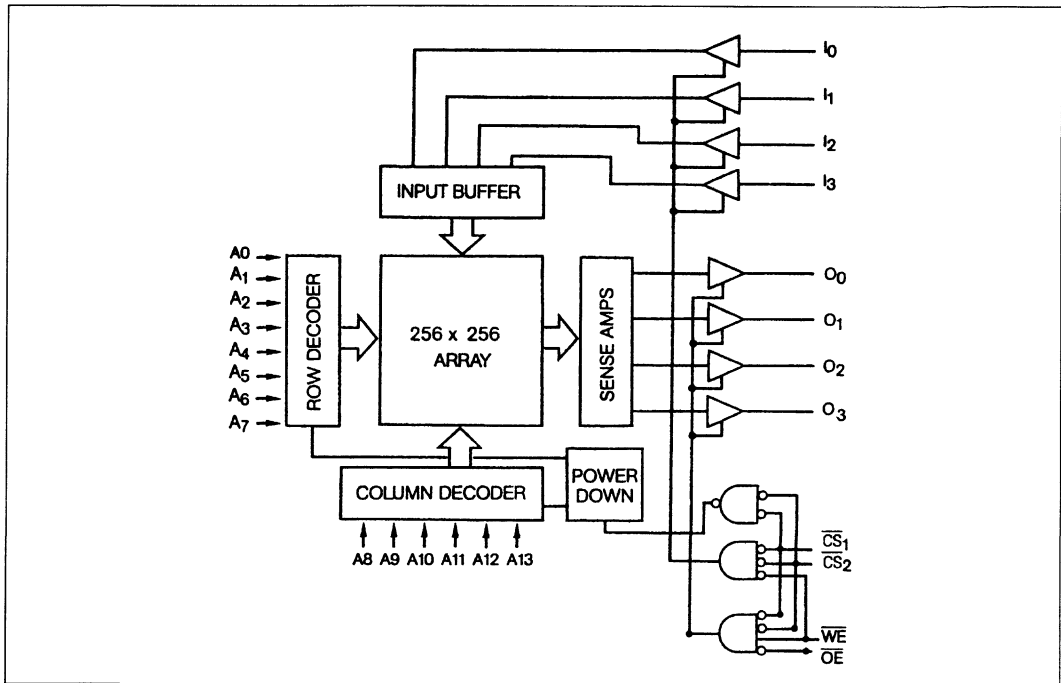


## LOGIC SYMBOL



\* Preliminary

## BLOCK DIAGRAM



## PIN NAMES

|                         |                       |
|-------------------------|-----------------------|
| A0-A13 : Address inputs | CS1-CS2 : Chip-Select |
| I0-I3 : Inputs          | OE : Output enable    |
| O0-O3 : Outputs         | WE : Write enable     |
| VCC : Power             | GND : Ground          |

## TRUTH TABLE

| CS | OE | WE | DATA-IN | DATA-OUT | MODE     |
|----|----|----|---------|----------|----------|
| H  | X  | X  | Z       | Z        | Deselect |
| L  | L  | H  | Z       | Valid    | Read     |
| L  | H  | L  | Valid   | Valid    | Write    |
| L  | L  | L  | Valid   | Valid    | Write    |

L = low, H = high, or L, Z = high impedance.



## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential :  $-0.5\text{ V to }+7.0\text{ V}$   
 DC input voltage :  $-3.0\text{ V to }7.0\text{ V}$   
 DC output voltage in high Z state :  $-0.5\text{ V to }+7.0\text{ V}$   
 Storage temperature :  $-65^{\circ}\text{C to }+150^{\circ}\text{C}$

Output current into outputs (low) :  $20\text{ mA}$   
 Electro static discharge voltage :  $> 2001\text{ V (MIL STD 883C method 3015.2)}$

## OPERATING RANGE

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                         |
|------------|-------|-----------------------|-----------------------------------------------|
| Military   | (- 2) | $5\text{ V} \pm 10\%$ | $-55^{\circ}\text{C to }+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $5\text{ V} \pm 10\%$ | $-40^{\circ}\text{C to }+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $5\text{ V} \pm 10\%$ | $0^{\circ}\text{C to }+70^{\circ}\text{C}$    |

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | $-3.0$  | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | —       | VCC     | V    |

## CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (1)  | Output capacitance | —       | —       | 7       | pF   |

Note : 1.  $T_A = 25^{\circ}\text{C}$  -  $f = 1\text{ MHz}$  -  $V_{CC} = 5.0\text{ V}$ , these parameters are not 100 % tested.

## AC TEST LOADS WAVEFORMS

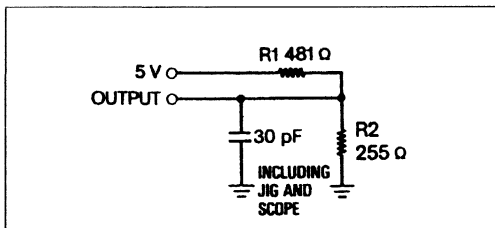


Fig. 1a.

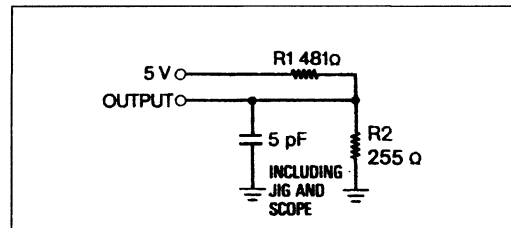


Fig. 1b.

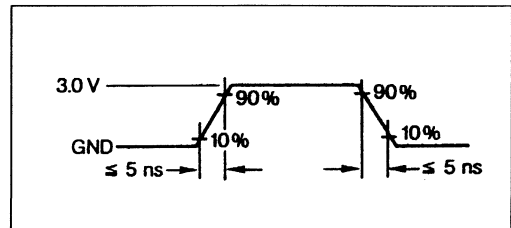
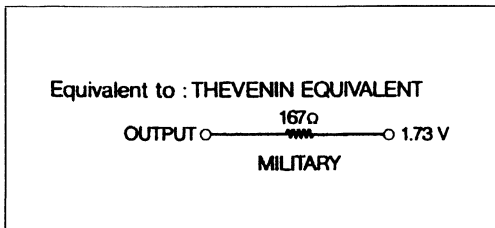


Fig. 2.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|-----|------------------------------|---------|---------|---------|------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | μA   |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | μA   |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA   |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V    |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V    |

- Notes :**
2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
  3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4. Vcc min, IOL = 8.0 mA.
  5. Vcc min, IOH = - 4.0 mA.

**Consumption for Commercial specification (– 5) :**

| SYMBOL |     | PARAMETER                 | 65791<br>E-5* | 65791<br>F-5 | 65791<br>H-5 | 65791<br>K-5 | 65791<br>M-5 | UNIT | VALUE |
|--------|-----|---------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40            | 40           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (8) | Dynamic Operating current | 115           | 100          | 100          | 100          | 100          | mA   | max   |

**Consumption for Industrial (– 9) and Military specification (2) :**

| SYMBOL |     | PARAMETER                 | 65791<br>H-9/2 | 65791<br>K-9/2 | 65791<br>M-9/2 | UNIT | VALUE |
|--------|-----|---------------------------|----------------|----------------|----------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 40             | 30             | 30             | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20             | 20             | 20             | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 100            | 100            | 100            | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$  min duty cycle = 100 %. A pull-up resistor to VCC on the  $\overline{CS}$  is required to keep the device unselected during VCC power-up. Otherwise ICC SB will exceed above values.
  7.  $\overline{CS} = V_{CC} - 0.3V$  Iout = 0 mA.
  8. Vcc max, Output current = 0mA, f = max, Vin = Vcc or Gnd.
- \* Preliminary.

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

## WRITE CYCLE : Commercial specification

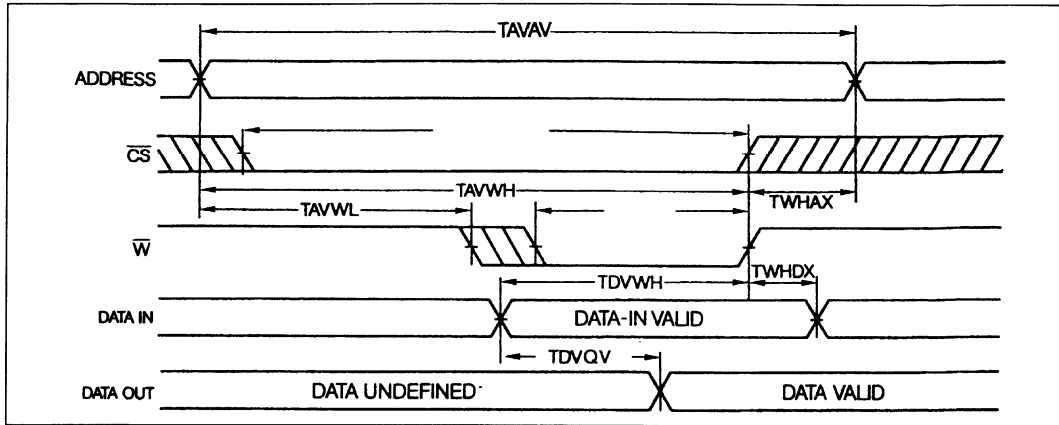
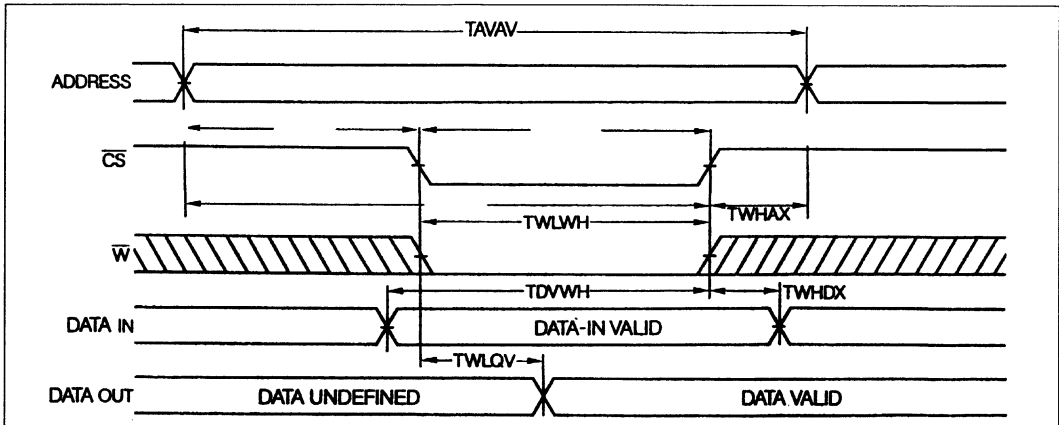
| SYMBOL | PARAMETER                        | 65791<br>E-5* | 65791<br>F-5 | 65791<br>H-5 | 65791<br>K-5 | 65791<br>M-5 | UNIT | VALUE |
|--------|----------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | Write cycle time                 | 15            | 20           | 20           | 25           | 40           | ns   | min   |
| TAVWL  | Address set-up time              | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH  | Address Valid to end of write    | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TDVWH  | Data set-up time                 | 10            | 10           | 10           | 15           | 15           | ns   | min   |
| TELWH  | CS low to write end              | 12            | 15           | 20           | 25           | 30           | ns   | min   |
| TWLQZ  | Write low to high Z              | 7             | 7            | 7            | 10           | 15           | ns   | max   |
| TWLWH  | Write pulse width                | 12            | 15           | 15           | 20           | 20           | ns   | min   |
| TWHAX  | Address hold from end of write   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX  | Data hold time                   | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TWLQV  | $\overline{W}$ low to data valid | 15            | 20           | 25           | 30           | 35           | ns   | max   |
| TDVQV  | Data valid to output valid       | 15            | 20           | 20           | 30           | 35           | ns   | max   |

## WRITE CYCLE : Industrial and military specification

| SYMBOL    | PARAMETER                        | 65791<br>H-9/2 | 65791<br>K-9/2 | 65791<br>M-9/2 | UNIT | VALUE |
|-----------|----------------------------------|----------------|----------------|----------------|------|-------|
| TAVAV     | Write cycle time                 | 20             | 25             | 40             | ns   | min   |
| TAVWL     | Address set-up time              | 0              | 0              | 0              | ns   | min   |
| TAVWH     | Address valid to end of write    | 20             | 25             | 30             | ns   | min   |
| TDVWH     | Data set-up time                 | 10             | 15             | 15             | ns   | min   |
| TELWH     | $\overline{CS}$ low to write end | 20             | 25             | 30             | ns   | min   |
| TWLQZ (8) | Write low to high Z              | 7              | 10             | 15             | ns   | max   |
| TWLWH     | Write pulse width                | 15             | 20             | 20             | ns   | min   |
| TWHAX     | Address hold from end of write   | 0              | 0              | 0              | ns   | min   |
| TWHDX     | Data hold time                   | 0              | 0              | 0              | ns   | min   |
| TWLQV     | $\overline{W}$ low to data valid | 25             | 30             | 35             | ns   | max   |
| TDVQV     | Data valid to output valid       | 20             | 30             | 35             | ns   | max   |

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

\* Preliminary.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED)

4

**READ CYCLE : Commercial specification**

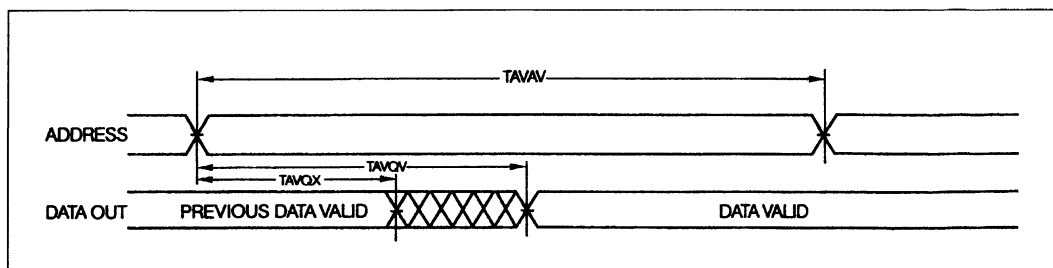
| SYMBOL | PARAMETER                          | 65791<br>E-5* | 65791<br>F-5 | 65791<br>H-5 | 65791<br>K-5 | 65791<br>M-5 | UNIT | VALUE |
|--------|------------------------------------|---------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV  | READ cycle time                    | 15            | 20           | 25           | 35           | 45           | ns   | min   |
| TAVQV  | Address access time                | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TAVQX  | Address Valid to low Z             | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TELQV  | Chip-select access time            | 15            | 20           | 25           | 35           | 45           | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5             | 5            | 5            | 5            | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 8             | 8            | 10           | 12           | 15           | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0             | 0            | 0            | 0            | 0            | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 15            | 20           | 20           | 20           | 25           | ns   | max   |
| TGLQV  | Output enable access time          | 10            | 10           | 12           | 15           | 20           | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3             | 3            | 3            | 3            | 3            | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 8             | 8            | 10           | 12           | 15           | ns   | max   |

**READ CYCLE : Industrial and Military specification**

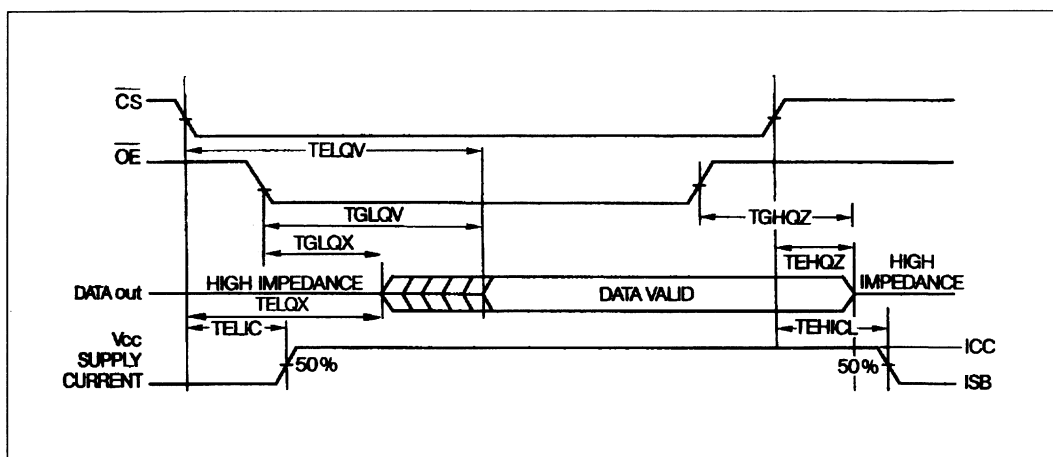
| SYMBOL | PARAMETER                          | 65791<br>H-9/2 | 65791<br>K-9/2 | 65791<br>M-9/2 | UNIT | VALUE |
|--------|------------------------------------|----------------|----------------|----------------|------|-------|
| TAVAV  | READ cycle time                    | 25             | 35             | 45             | ns   | min   |
| TAVQW  | Address access time                | 25             | 35             | 45             | ns   | max   |
| TAVQX  | Address Valid to low Z             | 3              | 3              | 3              | ns   | min   |
| TELQV  | Chip-select access time            | 25             | 35             | 45             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 5              | 5              | 5              | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 10             | 12             | 15             | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0              | 0              | 0              | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20             | 20             | 25             | ns   | max   |
| TGLQV  | Output enable access time          | 12             | 15             | 20             | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3              | 3              | 3              | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 10             | 12             | 15             | ns   | min   |

\* Preliminary

## READ CYCLE nb 1



## READ CYCLE nb 2



## ORDERING INFORMATION

| Package                                                                        | Device                                                                          | Grade                                                          | Level                                                                                                  |
|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| <u>HM1</u>                                                                     | <u>65791</u>                                                                    | <u>H</u>                                                       | <u>- 5</u>                                                                                             |
| 0 - Chip form<br>1 - Ceramic 24 pins<br>3 - Plastic 28 pins<br>4 - LCC 28 pins | 16 k x 4 high speed<br>static RAM<br>with separate I/O<br>and transparent write | E* = 15 ns<br>F = 20 ns<br>H = 25 ns<br>K = 35 ns<br>M = 45 ns | - 5 : Commercial<br>- 9 : Industrial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

\* Preliminary.

4

## PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins  
 SOIC DIL, 300 mils, 28 pins  
 Ceramic, 300 mils, 28 pins  
 LCC rectangular, 28 pins





## DATA SHEET

## HM 65764

# 8 k x 8 HIGH SPEED CMOS SRAM

## FEATURES

- FAST ACCESS TIME  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 15\*/20/25/35/45/55 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 380 mW (typ)  
STANDBY : 110mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO 125°C
- 300 AND 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

## DESCRIPTION

The HM 65764 is a high speed CMOS static RAM organized as 8192x8 bits. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 550 mW.

The HM 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

Easy memory expansion is provided by active low chip select (CS1), an active high chip select (CS2), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65764 are TTL compatible and operate from single 5 V supply thus simplifying system design.

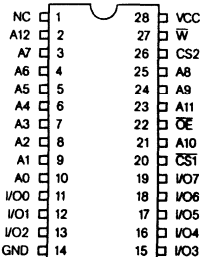
The HM 65764 is processed following the test methods of MIL STD 883C.

## PACKAGES

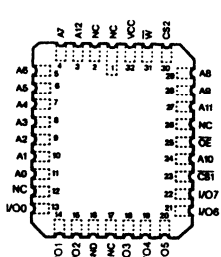
Plastic 300 & 600 mil, 28 pins, DIL.  
Ceramic 300 mils, 600 mils, 28 pins, DIL

SOIC & SOJ 300 mils, 28 pins, DIL.  
SOIC 330 mils, 28 pins  
LCC 32 pins.

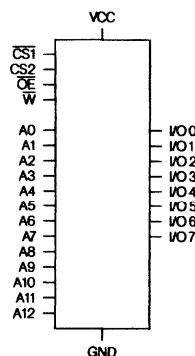
## Pinout DIL 28 pins (top view)



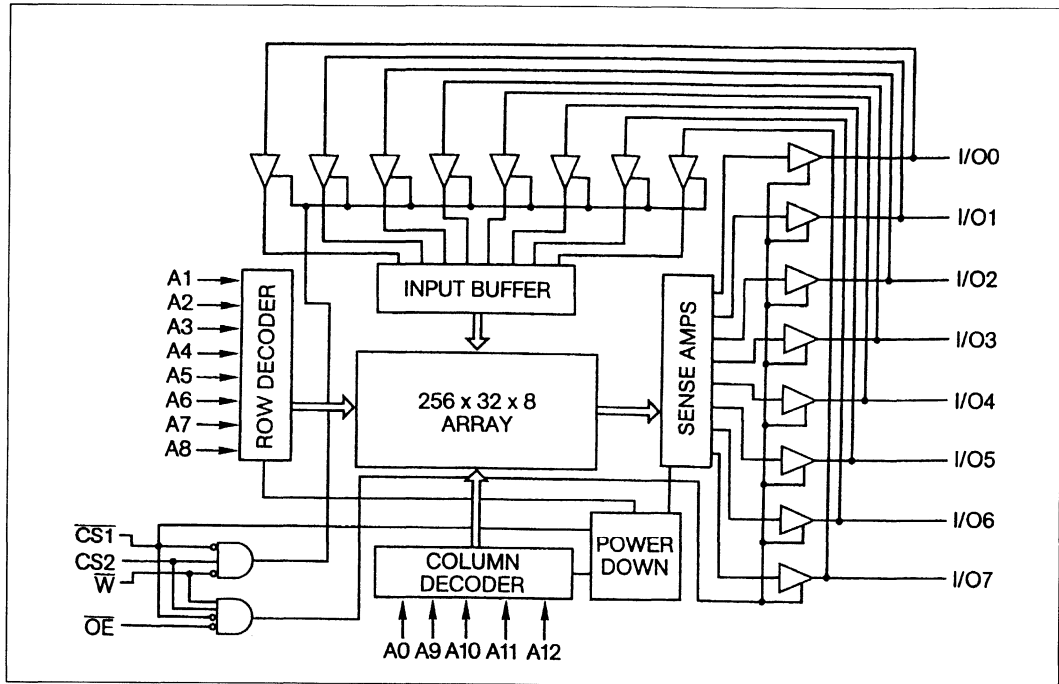
## Pinout LCC 32 pins (top view)



## LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN NAMES

|                            |                                         |
|----------------------------|-----------------------------------------|
| A0-A13 : Address inputs    | $\overline{\text{CS1}}$ : Chip Select 1 |
| I/O0-I/O7 : Inputs/Outputs | $\text{CS2}$ : Chip Select 2            |
| VCC : Power                | $\overline{\text{OE}}$ : Output enable  |
| GND : Ground               | $\overline{\text{W}}$ : Write enable    |

## TRUTH TABLE

| $\overline{\text{CS1}}$ | $\text{CS2}$ | $\overline{\text{OE}}$ | $\overline{\text{W}}$ | DATA-IN | DATA-OUT | MODE           |
|-------------------------|--------------|------------------------|-----------------------|---------|----------|----------------|
| H                       | X            | X                      | X                     | Z       | Z        | Deselect       |
| L                       | H            | L                      | H                     | Z       | Valid    | Read           |
| L                       | H            | X                      | L                     | Valid   | Z        | Write          |
| L                       | H            | H                      | H                     | Z       | Z        | Output disable |

L = low - H = high - X = H or L - Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V  
DC input voltage : - 3.0 V to 7.0 V  
DC output voltage in high Z state : - 0.5 V to + 7.0 V  
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA  
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

4

CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (1)  | Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

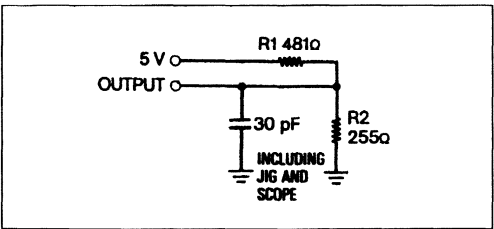


Fig. 1a.

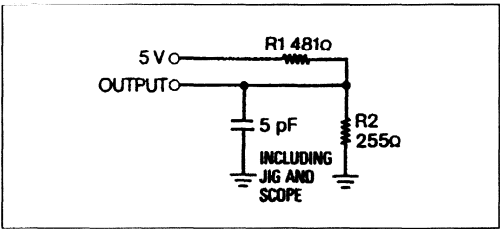


Fig. 1b.

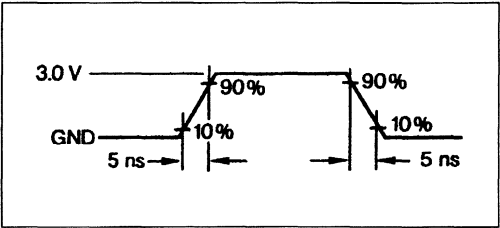
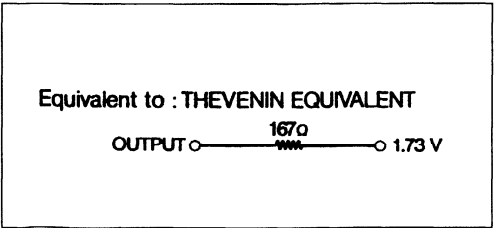


Fig. 2

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|------------------------------|---------|---------|---------|---------|
| IIX (2)   | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ (3)   | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS (3)   | Output short circuit current | -       | -       | - 300.0 | mA      |
| VOL (4)   | Output low voltage           | -       | -       | 0.4     | V       |
| VOH (5)   | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
  3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4. Vcc min, IOL = 8.0 mA.
  5. Vcc min, IOH = - 4.0 mA.

## Consumption for Commercial specification (- 5) :

| SYMBOL     | PARAMETER                 | 65764<br>E-5* | 65764<br>F-5 | 65764<br>H-5 | 65764<br>K-5 | 65764<br>M-5 | 65764<br>N-5 | UNIT | VALUE |
|------------|---------------------------|---------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 40            | 40           | 30           | 30           | 30           | 30           | mA   | max   |
| ICCSB1 (7) | Standby supply current    | 20            | 20           | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (8)  | Dynamic operating current | 135           | 125          | 125          | 125          | 125          | 125          | mA   | max   |

## Consumption for Industrial (- 9) and Military specification (2) :

| SYMBOL     | PARAMETER                | 65764<br>H-9/2 | 65764<br>K-9/2 | 65764<br>M-9/2 | 65764<br>N-9/2 | UNIT | VALUE |
|------------|--------------------------|----------------|----------------|----------------|----------------|------|-------|
| ICCSB (6)  | Standby supply current   | 40             | 30             | 30             | 30             | mA   | max   |
| ICCSB1 (7) | Standby supply current   | 20             | 20             | 20             | 20             | mA   | max   |
| ICCOP (8)  | Operating supply current | 125            | 125            | 125            | 125            | mA   | max   |

- Notes :**
6. CS1  $\geq$  VIH, CS2  $\leq$  VIL min duty cycle = 100 %, a pull-up resistor to VCC on the CS is required to keep the device unselected during Vcc power-up.  
Otherwise IocSB will exceed above values.
  7. CS1  $\geq$  Vcc - 0.3 V CS2 < 0.3 V Iout = 0 mA.
  8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
- \* Preliminary.

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 10 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH (see figure 1 and 1b) : + 30 pF

**WRITE CYCLE : Commercial specification**

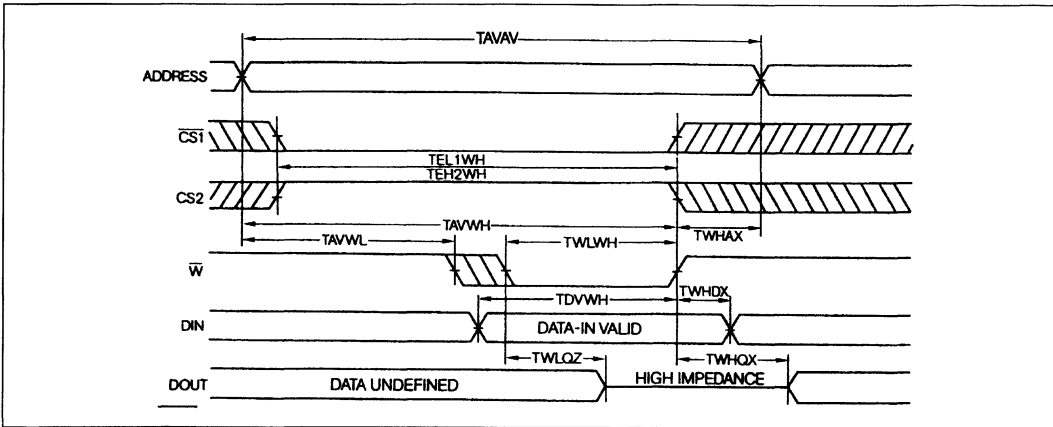
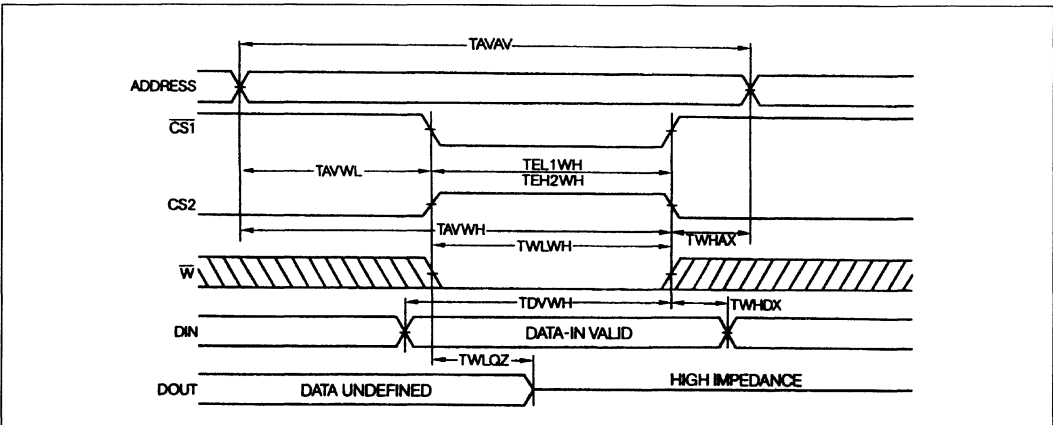
| SYMBOL       | PARAMETER                         | 65764<br>E-5* | 65764<br>F-5 | 65764<br>H-5 | 65764<br>K-5 | 65764<br>M-5 | 65764<br>N-5 | UNIT | VALUE |
|--------------|-----------------------------------|---------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV        | Write cycle time                  | 15            | 20           | 20           | 25           | 40           | 50           | ns   | min   |
| TAVWL        | Address set-up time               | 0             | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TAVWH        | Address valid to end of write     | 10            | 15           | 20           | 25           | 30           | 40           | ns   | min   |
| TDVWH        | Data set-up time                  | 8             | 10           | 10           | 15           | 15           | 25           | ns   | min   |
| TEL1WH       | $\overline{CS1}$ low to write end | 10            | 15           | 20           | 25           | 30           | 40           | ns   | min   |
| TEH2WH       | CS2 high to write end             | 10            | 15           | 20           | 20           | 25           | 30           | ns   | min   |
| TWLQZ (9)    | Write low to high Z               | 7             | 7            | 7            | 10           | 15           | 20           | ns   | max   |
| TWLWH        | Write pulse width                 | 10            | 15           | 25           | 20           | 20           | 25           | ns   | min   |
| TWHAX        | Address hold from end of write    | 0             | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TWHDX        | Data hold time                    | 0             | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TWHQX (8, 9) | Write high to low Z               | 3             | 5            | 5            | 5            | 5            | 5            | ns   | min   |

\* Preliminary.

**WRITE CYCLE : Industrial and Military specification**

| SYMBOL       | PARAMETER                         | 65764<br>H-9/-2 | 65764<br>K-9/-2 | 65764<br>M-9/-2 | 65764<br>N-9/-2 | UNIT | VALUE |
|--------------|-----------------------------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV        | Write cycle time                  | 20              | 25              | 40              | 50              | ns   | min   |
| TAVWL        | Address set-up time               | 0               | 0               | 0               | 0               | ns   | min   |
| TAVWH        | Address valid to end of write     | 20              | 25              | 30              | 40              | ns   | min   |
| TDVWH        | Data set-up time                  | 10              | 15              | 15              | 25              | ns   | min   |
| TEL1WH       | $\overline{CS1}$ low to write end | 20              | 25              | 30              | 40              | ns   | min   |
| TEH2WH       | CS2 high to write end             | 20              | 20              | 25              | 30              | ns   | min   |
| TWLQZ (8)    | Write low to high Z               | 7               | 10              | 15              | 20              | ns   | max   |
| TWLWH        | Write pulse width                 | 25              | 20              | 20              | 25              | ns   | min   |
| TWHAX        | Address hold to end from write    | 0               | 0               | 0               | 0               | ns   | min   |
| TWHDX        | Data hold time                    | 0               | 0               | 0               | 0               | ns   | min   |
| TWHQX (8, 9) | Write high to low Z               | 5               | 5               | 5               | 5               | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 9)WRITE CYCLE 2  $\overline{CS1}$  CONTROLLED (note 9)

**Note :** 9. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if OE = VIH.

**READ CYCLE : Commercial specification**

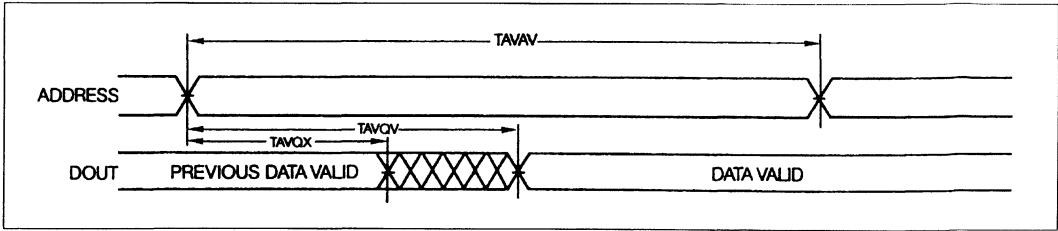
| SYMBOL      | PARAMETER                        | 65764<br>E-5* | 65764<br>F-5 | 65764<br>H-5 | 65764<br>K-5 | 65764<br>M-5 | 65764<br>N-5 | UNIT | VALUE |
|-------------|----------------------------------|---------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV       | READ cycle time                  | 15            | 20           | 25           | 35           | 45           | 55           | ns   | min   |
| TAVQV       | Address access time              | 15            | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TAVQX       | Address valid to low Z           | 3             | 3            | 3            | 3            | 3            | 3            | ns   | min   |
| TEL1QV      | Chip-select 1 access time        | 15            | 20           | 25           | 35           | 45           | 55           | ns   | max   |
| TEH2QV      | Chip-select 2 access time        | 15            | 20           | 25           | 25           | 30           | 40           | ns   | max   |
| TEL1QX      | $\overline{CS1}$ low to low Z    | 3             | 5            | 5            | 5            | 5            | 5            | ns   | min   |
| TEH2QX      | CS2 high to high Z               | 3             | 3            | 3            | 3            | 3            | 3            | ns   | min   |
| TEH1QZ (11) | $\overline{CS1}$ high to high Z  | 8             | 8            | 10           | 15           | 15           | 20           | ns   | max   |
| TEL2QZ (11) | CS2 low to high Z                | 8             | 8            | 10           | 15           | 15           | 20           | ns   | max   |
| TEL1IC      | $\overline{CS1}$ low to power up | 0             | 0            | 0            | 0            | 0            | 0            | ns   | min   |
| TEL1ICCL    | CS1 high to power down           | 15            | 20           | 20           | 20           | 25           | 25           | ns   | max   |
| TGLQV       | Output enable access time        | 10            | 10           | 12           | 15           | 20           | 25           | ns   | max   |
| TGLQX       | $\overline{OE}$ low to low Z     | 3             | 3            | 3            | 3            | 3            | 3            | ns   | min   |
| TGHQZ       | $\overline{OE}$ high to high Z   | 8             | 8            | 10           | 12           | 15           | 20           | ns   | max   |

\* Preliminary.

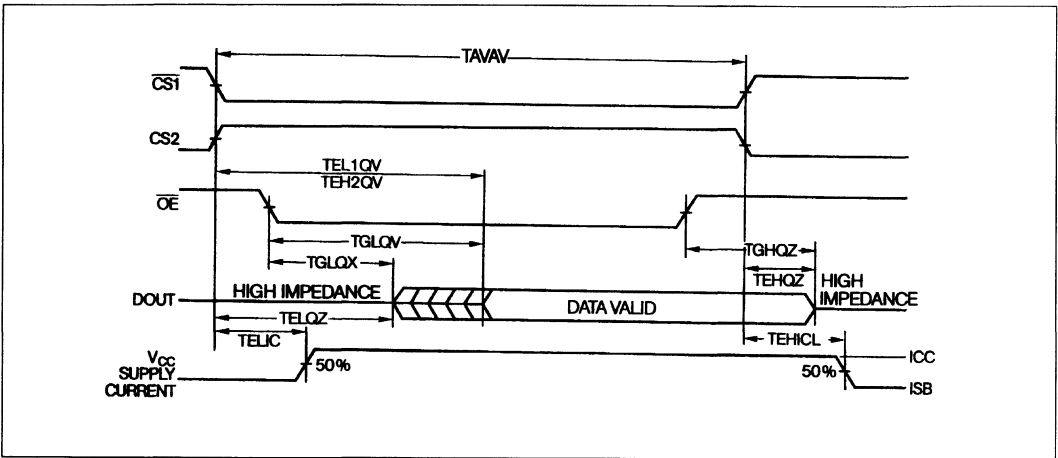
**READ CYCLE : Industrial and Military specification**

| SYMBOL      | PARAMETER                        | 65764<br>H-9/-2 | 65764<br>K-9/-2 | 65764<br>M-9/-2 | 65764<br>N-9/-2 | UNIT | VALUE |
|-------------|----------------------------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV       | READ cycle time                  | 25              | 35              | 45              | 55              | ns   | min   |
| TAVQV       | Address access time              | 25              | 35              | 45              | 55              | ns   | max   |
| TAVQX       | Address valid to low Z           | 3               | 3               | 3               | 3               | ns   | min   |
| TEL1QV      | Chip-select 1 access time        | 25              | 35              | 45              | 55              | ns   | max   |
| TEH2QV      | Chip-select 2 access time        | 25              | 25              | 30              | 40              | ns   | max   |
| TEL1QX      | $\overline{CS1}$ low to low Z    | 5               | 5               | 5               | 5               | ns   | min   |
| TEH2QX      | CS2 high to high Z               | 3               | 3               | 3               | 3               | ns   | min   |
| TEH1QZ (11) | $\overline{CS1}$ high to high Z  | 10              | 15              | 15              | 20              | ns   | max   |
| TEL2QZ (11) | CS2 high to high Z               | 10              | 15              | 15              | 20              | ns   | max   |
| TEL1IC      | $\overline{CS1}$ low to power up | 0               | 0               | 0               | 0               | ns   | min   |
| TEH1ICCL    | CS1 high to power down           | 20              | 20              | 25              | 25              | ns   | max   |
| TGLQV       | Output enable access time        | 12              | 15              | 20              | 25              | ns   | max   |
| TGLQX       | $\overline{OE}$ low to low Z     | 3               | 3               | 3               | 3               | ns   | min   |
| TGHQZ       | $\overline{OE}$ high to high Z   | 10              | 12              | 15              | 20              | ns   | min   |

READ CYCLE nb 1 (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



- Notes : 10. W is HIGH for read cycle.  
 11. Device is continuously selected.  $\overline{CS}_1$  &  $\overline{OE}$  = VIL and  $CS_2$  = VIH.  
 12. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.



## ORDERING INFORMATION

## Package

HM1

## Device type

65764

## Grade

H

## Level

- 5 : R

Tape and Reel  
Service8 k x 4 High speed  
static RAM

0 - Chip form

1 - Ceramic 28 pins 300 mils

1E - Ceramic 28 pins 600 mils

3 - Plastic 28 pins 300 mils

3E - Plastic 28 pins 600 mils

4 - LCC 32 pins

T - SOIC 28 pins 300 mils

TP - SOIC 28 pins 330 mils

U - SOJ 28 pins

E\* = 15 ns

F = 20 ns

H = 25 ns

K = 35 ns

M = 45 ns

N = 55 ns

- 5 : Commercial

- 9 : Industrial

- 2 : Military

- 8 : Military with B.I.

(B.I. = Burn-In)

\* Preliminary

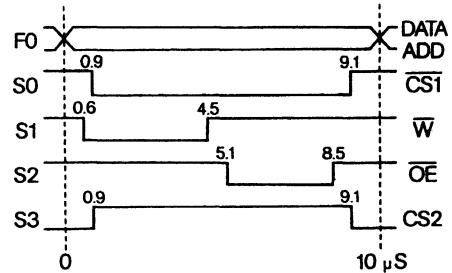
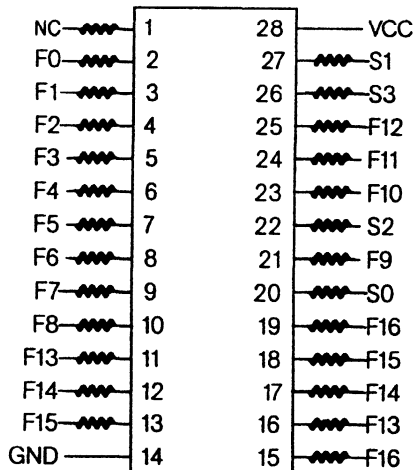
4

## PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins  
 Plastic DIL, 600 mils, 28 pins  
 SOIC DIL, 300 mils, 28 pins  
 Ceramic, 300 mils, 28 pins  
 LCC rectangular, 32 pins

## BURN-IN SCHEMATICS



VCC = 5 V (− 0, + 0.5)

R = 1 KΩ per pin

FO = 50 KHz ± 20 %

Fn = 1/2 Fn-1

S0 to S3 : programmable signals for write / read cycles

NC = Not connected



DATA SHEET

HM 65779

8 K x 9  
HIGH SPEED CMOS SRAM

FEATURES

- FAST ACCESS TIME  
COMMERCIAL : 25\*/35/45/55 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 850 mW (max)  
STANDBY : 125 mW (max)
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

4

DESCRIPTION

The HM 65779 is a high speed CMOS static RAM organized as 8192 x 9 bits. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 850 mW. The HM 65779 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 68 % when the circuit is deselected. Easy memory expansion is provided by an active low chip select

(CS1), an active high chip select (CS2), an active low output enable (OE) and three state drivers. All inputs and outputs of the HM 65779 are TTL compatible and operate from a single 5 V supply thus simplifying system design. The HM-65779 is processed following the test methods of MIL STD 883C. The HM 65779 is cache memory application oriented. It can be used either as cache disk (RAM disk) or cache memory in the main frame.

PACKAGES

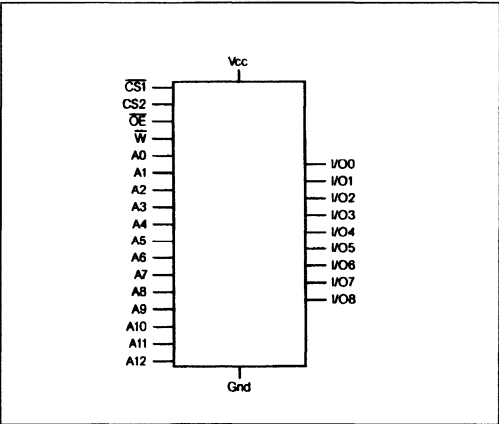
Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins, DIL.  
SOIC 300/330 mils and SOJ 300 mils, 28 pins  
Tape and Reel Service.

**Pinout DIL 28 pins (top view)**

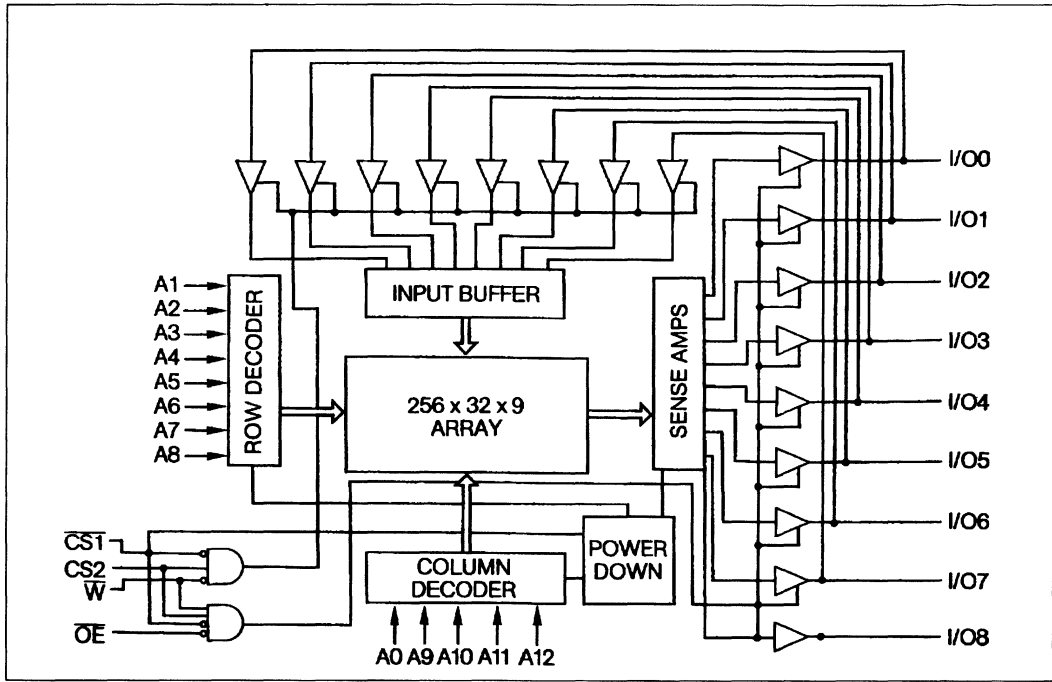
|      |    |    |      |
|------|----|----|------|
| A4   | 1  | 28 | VCC  |
| A5   | 2  | 27 | W    |
| A6   | 3  | 26 | CS2  |
| A7   | 4  | 25 | A3   |
| A8   | 5  | 24 | A2   |
| A9   | 6  | 23 | A1   |
| A10  | 7  | 22 | OE   |
| A11  | 8  | 21 | A0   |
| A12  | 9  | 20 | CS1  |
| I/O0 | 10 | 19 | I/O8 |
| I/O1 | 11 | 18 | I/O7 |
| I/O2 | 12 | 17 | I/O6 |
| I/O3 | 13 | 16 | I/O5 |
| GND  | 14 | 15 | I/O4 |

\* Preliminary

LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN NAMES

|                            |                                  |
|----------------------------|----------------------------------|
| A0-A13 : Address inputs    | $\overline{CS1}$ : Chip Select 1 |
| I/O0-I/O8 : Inputs/Outputs | CS2 : Chip Select 2              |
| VCC : Power                | $\overline{OE}$ : Output Enable  |
| GND : Ground               | $\overline{W}$ : Write enable    |

## TRUTH TABLE

| $\overline{CS1}$ | CS2 | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE                  |
|------------------|-----|-----------------|----------------|---------|----------|-----------------------|
| H                | X   | X               | X              | Z       | Z        | Deselect (power down) |
| L                | H   | L               | H              | Z       | Valid    | Read                  |
| L                | H   | X               | L              | Valid   | Z        | Write                 |
| L                | H   | H               | H              | Z       | Z        | Output disable        |
| X                | L   | X               | X              | Z       | Z        | Deselect              |

L = low - H = high - X = H or L - Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V  
DC input voltage : - 3.0 V to + 7.0 V  
DC output voltage in high Z state : - 0.5 V to + 7.0 V  
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA  
Electro Static Discharge voltage > 2000 V (MIL STD 883C method 3015.)

OPERATING RANGE

|            |           | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-----------|-------------------|-----------------------|
| Commercial | (- 5)     | 5 V ± 10 %        | 0°C to + 70°C         |
| Military   | (- 2/- 8) | 5 V ± 10 %        | - 55°C to + 125°C     |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (1)  | Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

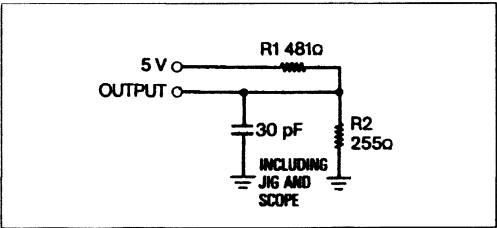


Fig. 1a.

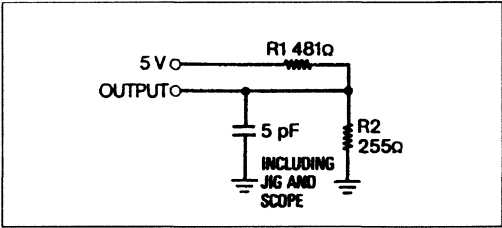


Fig. 1b.

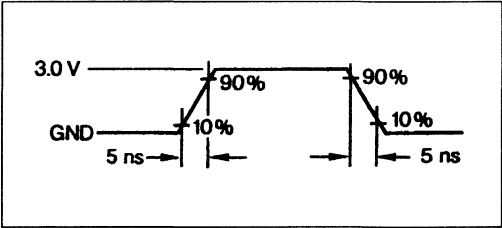
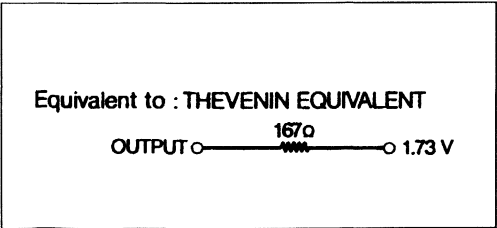


Figure 2 : All Input Pulses.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 300.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**Consumption for Commercial specification :**

| SYMBOL |     | PARAMETER                 | 65779<br>H-5* | 65779<br>K-5 | 65779<br>M-5 | 65779<br>N-5 | UNIT | VALUE |
|--------|-----|---------------------------|---------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 20            | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (7) | Dynamic operating current | 120           | 120          | 120          | 120          | mA   | max   |

**CONSUMPTION FOR MILITARY (-2) SPECIFICATION :**

| SYMBOL |     | PARAMETER                | 65779<br>K-2 | 65764<br>M-2 | 65779<br>N-2 | UNIT | VALUE |
|--------|-----|--------------------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current   | 30           | 30           | 30           | mA   | max   |
| ICCOP  | (7) | Operating supply current | 140          | 140          | 140          | mA   | max   |

- Notes :**
6.  $CS1 \geq V_{IH}$ ,  $CS2 \leq V_{IL}$ , a pull-up resistor to  $V_{cc}$  on the  $\overline{CS}$  input is required to keep the device deselected during  $V_{cc}$  power-up otherwise ICCSB will exceed above values.
  7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .
- \* Preliminary

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output loading IOL/IOH : + 30 pF

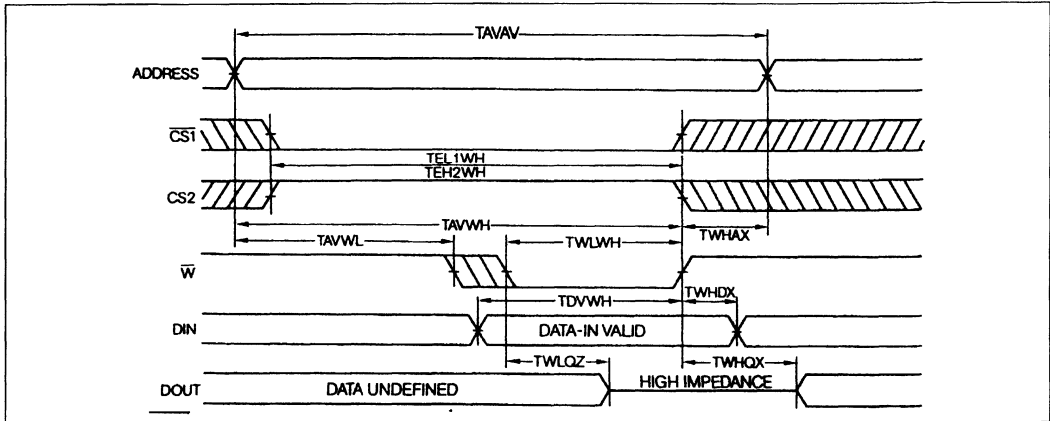
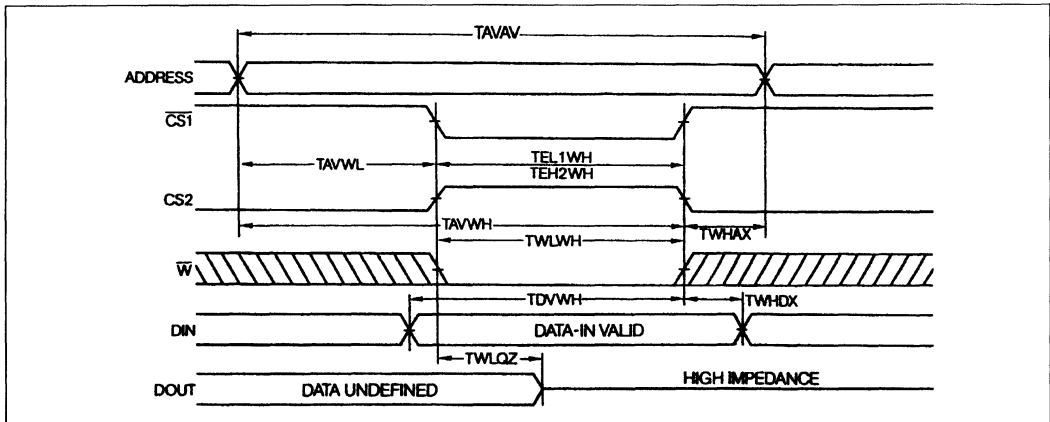
**WRITE CYCLE : Commercial specification**

| SYMBOL       | PARAMETER                         | 65779<br>H-5* | 65779<br>K-5 | 65779<br>M-5 | 65779<br>N-5 | UNIT | VALUE |
|--------------|-----------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV        | Write cycle time                  | 25            | 35           | 45           | 50           | ns   | min   |
| TAVWL        | Address set-up time               | 0             | 0            | 0            | 0            | ns   | min   |
| TAVWH        | Address valid to end of write     | 20            | 30           | 40           | 50           | ns   | min   |
| TDVWH        | Data set-up time                  | 15            | 20           | 25           | 30           | ns   | min   |
| TEL1WH       | $\overline{CS1}$ low to write end | 20            | 30           | 40           | 50           | ns   | min   |
| TEH2WH       | CS2 high to write end             | 20            | 30           | 40           | 50           | ns   | min   |
| TWLQZ (9)    | Write low to high Z               | 13            | 15           | 20           | 25           | ns   | max   |
| TWLWH        | Write pulse width                 | 20            | 25           | 30           | 35           | ns   | min   |
| TWHAX        | Address hold from end of write    | 5             | 5            | 5            | 5            | ns   | min   |
| TWHDX        | Data hold time                    | 0             | 0            | 0            | 0            | ns   | min   |
| TWHQX (8, 9) | Write high to low Z               | 3             | 3            | 3            | 3            | ns   | min   |

**WRITE CYCLE : Military specification**

| SYMBOL       | PARAMETER                         | 65779<br>K-2 | 65779<br>M-2 | 65779<br>N-2 | UNIT | VALUE |
|--------------|-----------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV        | Write cycle time                  | 35           | 45           | 50           | ns   | min   |
| TAVWL        | Address set-up time               | 0            | 0            | 0            | ns   | min   |
| TAVWH        | Address valid to end of write     | 30           | 40           | 50           | ns   | min   |
| TDVWH        | Data set-up time                  | 20           | 25           | 30           | ns   | min   |
| TEL1WH       | $\overline{CS1}$ low to write end | 30           | 40           | 50           | ns   | min   |
| TEH2WH       | CS2 high to write end             | 30           | 40           | 50           | ns   | min   |
| TWLQZ (9)    | Write low to high Z               | 15           | 20           | 25           | ns   | max   |
| TWLWH        | Write pulse width                 | 25           | 30           | 35           | ns   | min   |
| TWHAX        | Address hold to end of write      | 5            | 5            | 5            | ns   | min   |
| TWHDX        | Data hold time                    | 0            | 0            | 0            | ns   | min   |
| TWHQX (8, 9) | Write high to low Z               | 3            | 3            | 3            | ns   | min   |

- Note :**
- The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
  - At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.
- \* Preliminary

WRITE CYCLE 1  $\overline{W}$  CONTROLLED (note 10)WRITE CYCLE 2  $\overline{CS1}$  CONTROLLED (note 10)

**Note : 10.** The internal write of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
Data-out is HIGH impedance if  $\overline{OE} = \text{VIH}$ .



**READ CYCLE : Commercial specification**

| SYMBOL      | PARAMETER                           | 65779<br>H-5* | 65779<br>K-5 | 65779<br>M-5 | 65779<br>N-5 | UNIT | VALUE |
|-------------|-------------------------------------|---------------|--------------|--------------|--------------|------|-------|
| TAVAV       | READ cycle time                     | 25            | 35           | 45           | 55           | ns   | min   |
| TAVQV       | Address access time                 | 25            | 35           | 45           | 55           | ns   | max   |
| TAVQX       | Address valid to low Z              | 3             | 3            | 3            | 3            | ns   | min   |
| TEL1QV      | Chip-select 1 access time           | 25            | 35           | 45           | 55           | ns   | max   |
| TEH2QV      | Chip-select 2 access time           | 15            | 15           | 20           | 25           | ns   | max   |
| TEL1QX      | $\overline{CS1}$ low to low Z       | 5             | 5            | 5            | 5            | ns   | min   |
| TEH2QX      | CS2 high to low Z                   | 5             | 5            | 5            | 5            | ns   | min   |
| TEH1QZ (10) | $\overline{CS1}$ high to high Z     | 20            | 20           | 25           | 25           | ns   | max   |
| TEL2QZ (10) | CS2 high to high Z                  | 20            | 20           | 25           | 25           | ns   | max   |
| TEL1IC      | $\overline{CS1}$ low to power up    | 0             | 0            | 0            | 0            | ns   | min   |
| TEH1ICCL    | $\overline{CS1}$ high to power down | 20            | 20           | 25           | 25           | ns   | max   |
| TGLQV       | Output enable access time           | 15            | 15           | 20           | 25           | ns   | max   |
| TGLQX       | $\overline{OE}$ low to low Z        | 3             | 3            | 3            | 3            | ns   | min   |
| TGHQZ       | $\overline{OE}$ high to high Z      | 20            | 20           | 25           | 30           | ns   | max   |

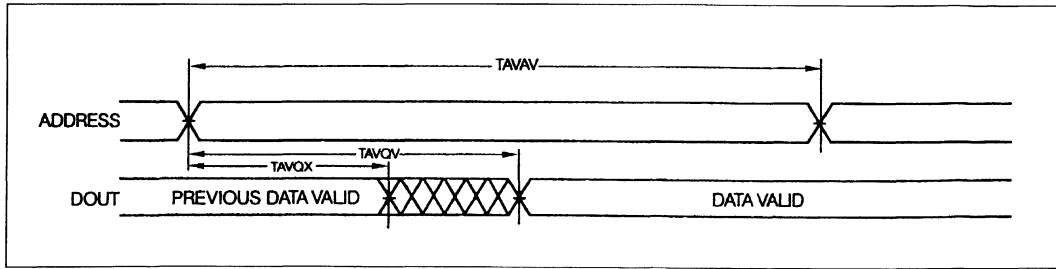
**READ CYCLE : Military specification**

| SYMBOL      | PARAMETER                           | 65779<br>K-2 | 65779<br>M-2 | 65779<br>N-2 | UNIT | VALUE |
|-------------|-------------------------------------|--------------|--------------|--------------|------|-------|
| TAVAV       | READ cycle time                     | 35           | 45           | 55           | ns   | min   |
| TAVQV       | Address access time                 | 35           | 45           | 55           | ns   | max   |
| TAVQX       | Address valid to low Z              | 3            | 3            | 3            | ns   | min   |
| TEL1QV      | Chip-select 1 access time           | 35           | 45           | 55           | ns   | max   |
| TEH2QV      | Chip-select 2 access time           | 20           | 20           | 25           | ns   | max   |
| TEL1QX      | $\overline{CS1}$ low to low Z       | 5            | 5            | 5            | ns   | min   |
| TEH2QX      | CS2 high to low Z                   | 5            | 5            | 5            | ns   | min   |
| TEH1QZ (10) | $\overline{CS1}$ high to high Z     | 20           | 25           | 25           | ns   | max   |
| TEL2QZ (10) | CS2 high to high Z                  | 20           | 25           | 25           | ns   | max   |
| TEL1IC      | $\overline{CS1}$ low to power up    | 0            | 0            | 0            | ns   | min   |
| TEH1ICCL    | $\overline{CS1}$ high to power down | 20           | 25           | 25           | ns   | max   |
| TGLQV       | Output enable access time           | 20           | 20           | 25           | ns   | max   |
| TGLQX       | $\overline{OE}$ low to low Z        | 3            | 3            | 3            | ns   | min   |
| TGHQZ       | $\overline{OE}$ high to high Z      | 20           | 25           | 30           | ns   | max   |

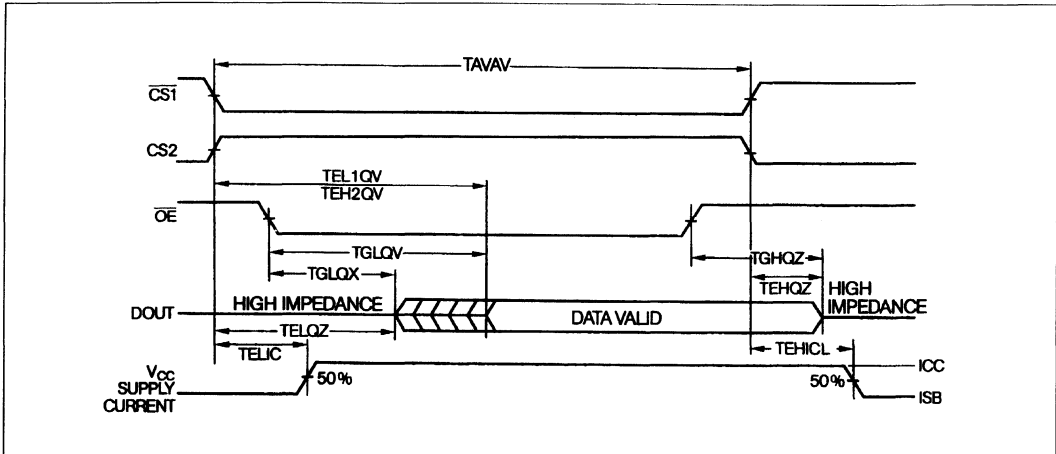
**Note :** 10. TEHQZ and TWLQZ are specified with C1 = 5 pF. Transition is measured  $\pm 500$  mV from steady state voltage.

\* Preliminary

## READ CYCLE nb 1 (notes 12, 13)



## READ CYCLE nb 2 (note 12,14)



**Notes :** 12.  $\bar{w}$  is high for read cycle.

13. Device is continuously selected,  $\overline{CS_1}/\overline{OE}_i = V_{IL}$ ,  $CS_2 = V_{IH}$ .

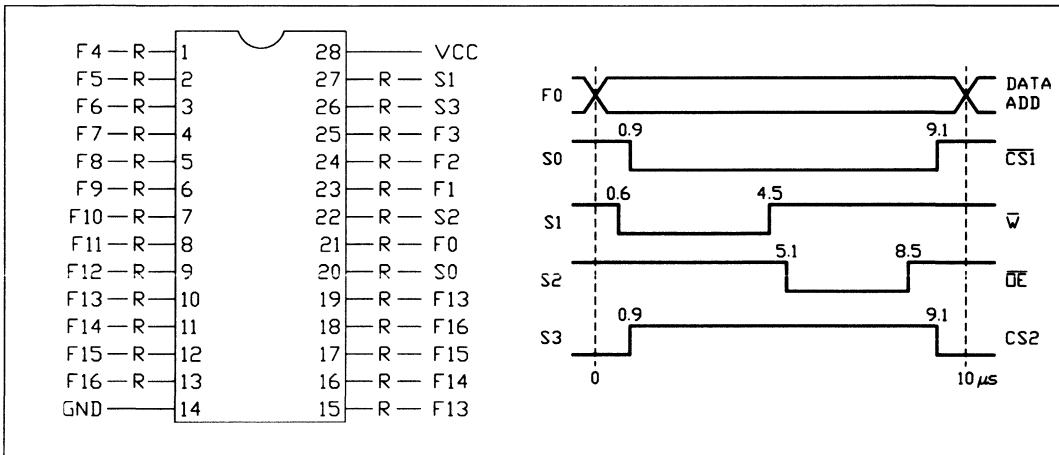
14. Address valide prior to or coincident with CS transition LOW.

## HM 65779

### ORDERING INFORMATION

| Package                        | Device type                   | Grade     | Level                    |                       |
|--------------------------------|-------------------------------|-----------|--------------------------|-----------------------|
| HM1                            | 65779                         | H         | - 5 : R                  | Tape and Reel Service |
|                                | 8 k x 9 high speed static RAM |           | - 5 : Commercial         |                       |
|                                |                               |           | - 2 : Military           |                       |
|                                |                               |           | - 8 : Military with B.I. |                       |
|                                |                               |           | (B.I. = Burn-In)         |                       |
| I - Ceramic 28 pins, 300 mils. |                               | H = 25 ns |                          |                       |
| 3 - Plastic 28 pins, 300 mils. |                               | K = 35 ns |                          |                       |
| T - SO 300 mils, 28 pins.      |                               | M = 45 ns |                          |                       |
| TP - SO 330 mils, 28 pins.     |                               | N = 55 ns |                          |                       |
| U - SOJ 300 mils, 28 pins.     |                               |           |                          |                       |
| * Preliminary                  |                               |           |                          |                       |

### BURN-IN SCHEMATICS



VCC = + 5 V (– 0, + 0.5)

R = 1 KΩ per pin

F0 = 50 KHz ± 20 %

Fn = 1/2 Fn – 1

S0 to S3 = Programmable signal for read/write cycles.

4



## DATA SHEET

## HM 65797

## 256 K x 1 HIGH SPEED CMOS SRAM

## FEATURES

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**  
ACTIVE : 550 mW  
STANDBY : 193 mW
- **WIDE TEMPERATURE RANGE :**  
- 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE SINGLE 5 VOLT SUPPLY**

4

## DESCRIPTION

The HM-65797 is a high speed CMOS static RAM organised as 262, 144 X 1 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25ns are available with maximum power consumption of only 550mW.

The HM-65797 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 67 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

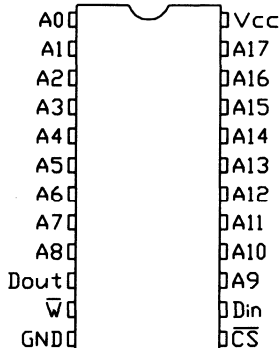
All inputs and outputs of the HM-65797 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65797 is 100 % processed following the test methods of MIL STD 883C.

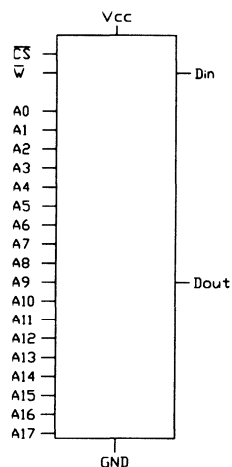
## PACKAGES

Plastic 300 mils, 24 pins, DIL.  
Ceramic 300 mils, 24 pins, DIL.  
SO/SOJ 300 and 330 mils, 24 pins  
LCC 28 pins.  
Tape and Reel Service

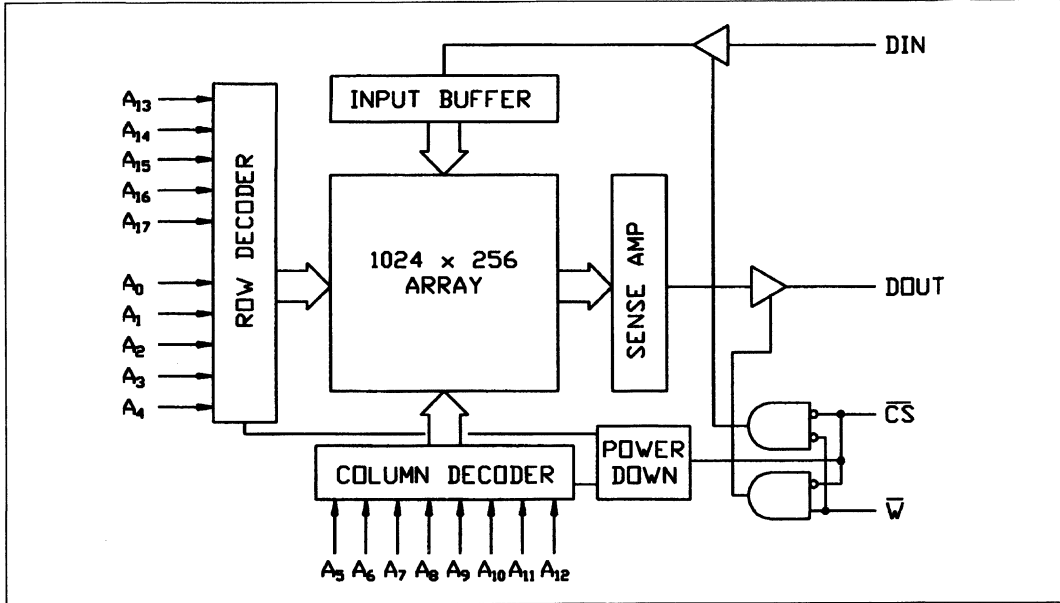
## Pinout DIL 24 pins (top view)



## LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN NAMES

|        |                  |                |                |
|--------|------------------|----------------|----------------|
| A0-A17 | : Address inputs | $\overline{W}$ | : Write enable |
| Din    | : Input          | Vcc            | : Power        |
| Dout   | : Output         | GND            | : Ground       |
| CS     | : Chip Select    |                |                |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{W}$ | INPUT | OUTPUT | MODE                |
|-----------------|----------------|-------|--------|---------------------|
| H               | X              | Z     | Z      | Deselect/Power Down |
| L               | H              | Z     | Valid  | Read                |
| L               | L              | Valid | Z      | Write               |
|                 |                | Z     | Z      |                     |

L = Low, H = High, X = H or L, Z = High Impedance.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential..... - 0.5 V to + 7.0 V  
 DC input voltage..... - 3.0 V to + 7.0 V  
 DC output voltage in high Z state..... - 0.5 V to + 7.0 V  
 Storage temperature..... - 65°C + 150°C  
 Output current into outputs (low)..... 20 mA  
 Electro static discharge voltage ..... > 2000 V (MIL STD 883C method 3015.2)

**OPERATING RANGE**

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V $\pm$ 10 %    | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V $\pm$ 10 %    | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V $\pm$ 10 %    | 0°C to + 70°C         |

**RECOMMENDED DC OPERATING CONDITIONS**

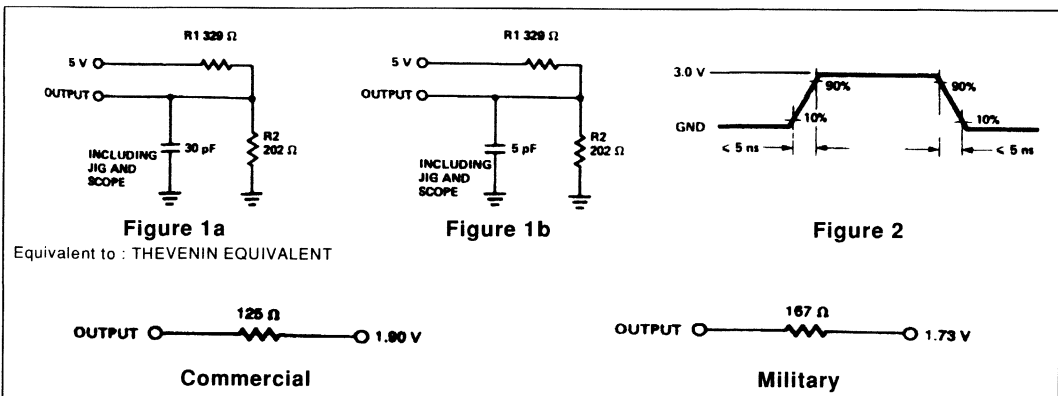
| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

4

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (1)  | Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

**AC TEST LOADS AND WAVEFORMS**

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 50.0  | -       | 50.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V       |

**Notes :** 2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.

3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.

4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$  (military),  $I_{OL} = 12.0 \text{ mA}$  (commercial)

5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65797<br>H-5 | 65797<br>K-5 | 65797<br>M-5 | 65797<br>N-5 | UNIT | VALUE |
|--------|-----|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35           | 35           | 35           | 35           | mA   | max   |
| ICCSB1 | (8) | Standby supply current    | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (7) | Dynamic operating current | 100          | 100          | 100          | 100          | mA   | max   |

**CONSUMPTION FOR INDUSTRIAL (- 9) AND MILITARY (-2) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65797<br>K-9/-2 | 65797<br>M-9/-2 | 65797<br>N-9/-2 | UNIT | VALUE |
|--------|-----|---------------------------|-----------------|-----------------|-----------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35              | 35              | 35              | mA   | max   |
| ICCSB1 | (8) | Standby supply current    | 20              | 20              | 20              | mA   | max   |
| ICCOP  | (7) | Dynamic operating current | 110             | 110             | 110             | mA   | max   |

**Notes :** 6.  $\overline{CS} \geq V_{IH}$ , a pull-up resistor to  $V_{cc}$  on the  $\overline{CS}$  is required to keep the devices unselected during the  $V_{cc}$  power-up. Otherwise  $I_{ccSB}$  will exceed the above values. Min duty cycle = 100 %.

7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .

8.  $\overline{CS} \geq V_{cc} - 0.3V$   $I_{out} = 0 \text{ mA}$ .



**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V

Input timing reference levels : 1.5 V

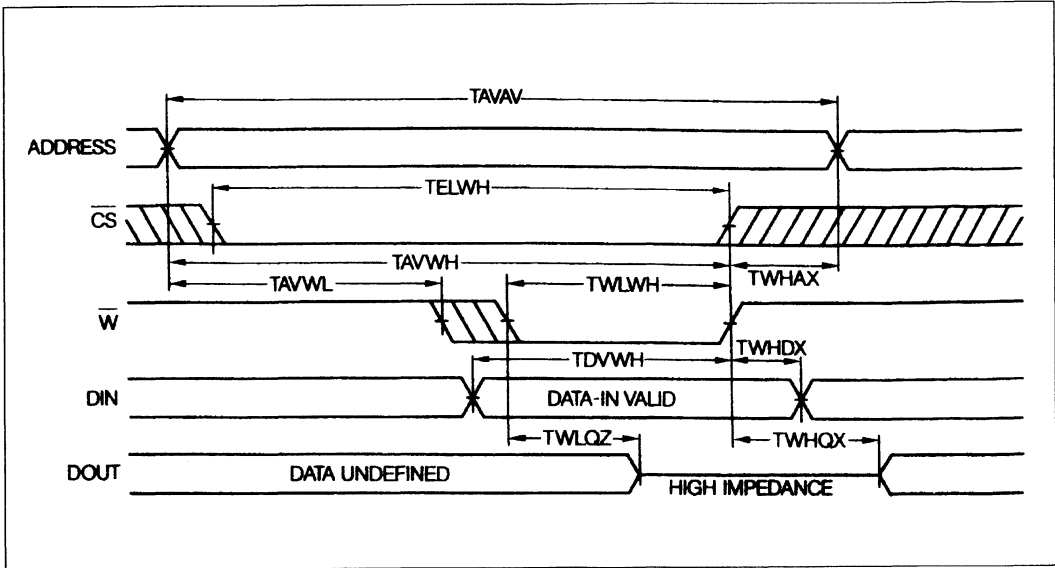
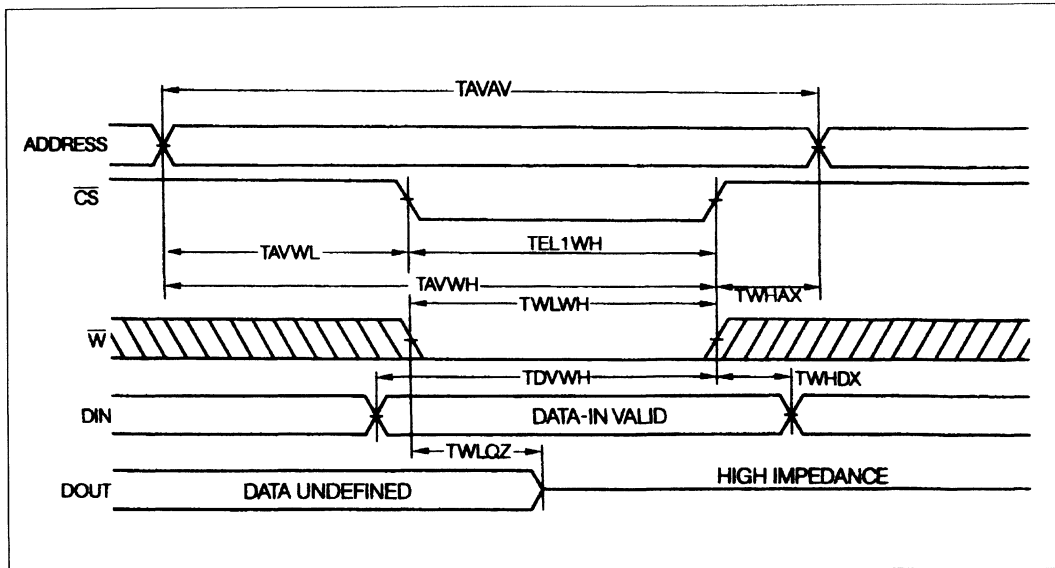
Input rise : 5 ns

Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

**WRITE CYCLE specification : Commercial, Industrial and Military**

| SYMBOL    | PARAMETER                   | 65797<br>H-5/-9/-2 | 65797<br>K-5/-9/-2 | 65797<br>M-5/-9/-2 | 65797<br>N-5/-9/-2 | UNIT | VALUE |
|-----------|-----------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV     | Write cycle time            | 25                 | 35                 | 45                 | 55                 | ns   | min   |
| TAVWL     | Address set-up time         | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TAVWH     | Address valid to write end  | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TDVWH     | Data set-up time            | 15                 | 17                 | 20                 | 25                 | ns   | min   |
| TELWH     | CS low to write end         | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TWLQZ (8) | Write low to high Z         | 13                 | 15                 | 20                 | 25                 | ns   | max   |
| TWLWH     | Write pulse width           | 20                 | 25                 | 30                 | 35                 | ns   | min   |
| TWHAX     | Address hold from write end | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHDX     | Data hold time              | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHQX (8) | Write high to low Z         | 3                  | 3                  | 3                  | 3                  | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

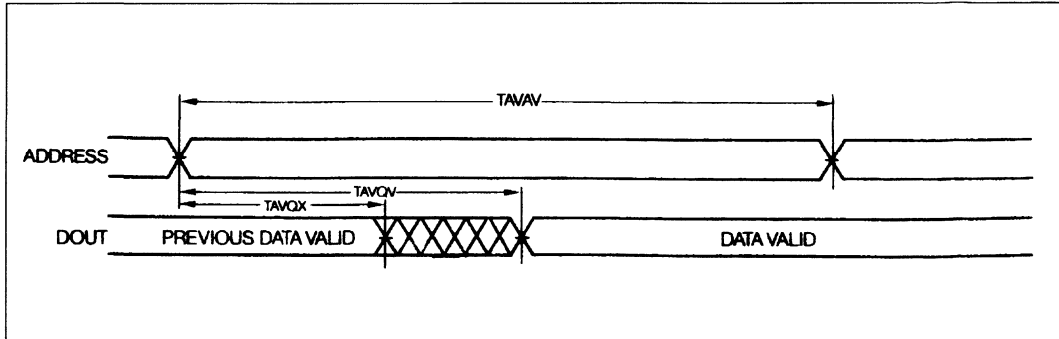
WRITE CYCLE 1 :  $\overline{W}$  controlled (note 9)WRITE CYCLE 2 :  $\overline{CS}$  controlled (note 9)

**Note :** 9. The internal write of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

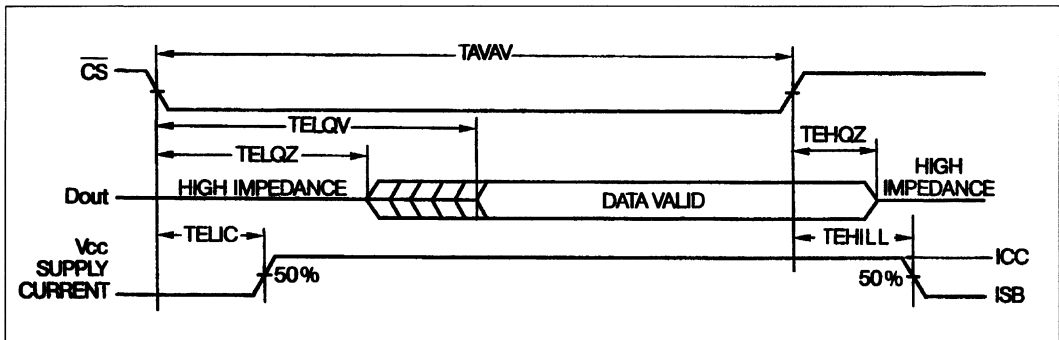
## READ CYCLE : specification : Commercial, Industrial and Military

| SYMBOL | PARAMETER                               | 65797<br>H-5/-9/-2 | 65797<br>K-5/-9/-2 | 65797<br>M-5/-9/-2 | 65797<br>N-5/-9/-2 | UNIT | VALUE |
|--------|-----------------------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV  | READ cycle time                         | 25                 | 35                 | 45                 | 55                 | ns   | min   |
| TAVQV  | Address access time                     | 25                 | 35                 | 45                 | 55                 | ns   | max   |
| TAVQX  | Address valid to low Z                  | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TELQV  | Chip-select access time                 | 25                 | 35                 | 45                 | 55                 | ns   | max   |
| TELQX  | $\overline{\text{CS}}$ low to low Z     | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TEHQZ  | $\overline{\text{CS}}$ high to high Z   | 13                 | 15                 | 20                 | 20                 | ns   | max   |
| TELIC  | $\overline{\text{CS}}$ low to power up  | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TEHICL | $\overline{\text{CS}}$ high to power up | 20                 | 25                 | 30                 | 35                 | ns   | max   |

## READ CYCLE 1 : (note 10, 11, 12)



## READ CYCLE 2 : (note 10, 12)



- Notes : 10.  $\overline{W}$  is high for read cycle.  
 11. Device is continuously selected,  $\overline{CS} = \text{VIL}$ .  
 12. Address valid prior or coincident with  $\overline{CS}$  transition low.

## ORDERING INFORMATION

| Package                      | Device Type                   | Grade     | Level                   |
|------------------------------|-------------------------------|-----------|-------------------------|
| HM1                          | 65797                         | H         | - 5 : R                 |
|                              | 256 x 1 high speed static RAM |           | Tape & Reel Service     |
| 0 - Chip form                |                               | H = 25 ns | - 5 : Commercial        |
| 1 - Ceramic 24 pins 300 mils |                               | K = 35 ns | - 9 : Industrial        |
| 3 - Plastic 24 pins 300 mils |                               | M = 45 ns | - 2 : Military          |
| T - SOIC 24 pins 300 mils    |                               | N = 55 ns | - 8 : Military with B.I |
| U - SOJ 24 pins              |                               |           | (B.I : Burn In)         |
| 4 - LCC 28 pins              |                               |           |                         |

**DATA SHEET****HM 65798****64 K x 4 HIGH SPEED CMOS SRAM****FEATURES**

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 25/35/45/55 ns (max)
- **LOWER POWER CONSUMPTION**  
ACTIVE : 660 mW  
STANDBY : 193 mW
- **WIDE TEMPERATURE RANGE :**  
- 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

**4****DESCRIPTION**

The HM-65798 is a high speed CMOS static RAM organised as 65,536 X 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 660 mW.

The HM-65798 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

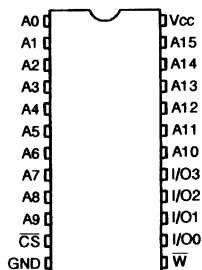
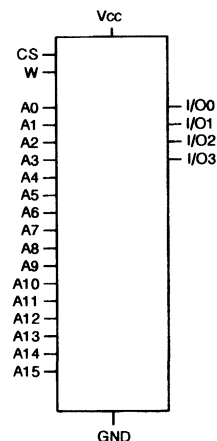
Easy memory expansion is provided by an active low chip select ( $\overline{CS}$ ) and three state drivers.

All inputs and outputs of the HM-65798 are TTL compatible and operate from single 5 V supply thus simplifying system design.

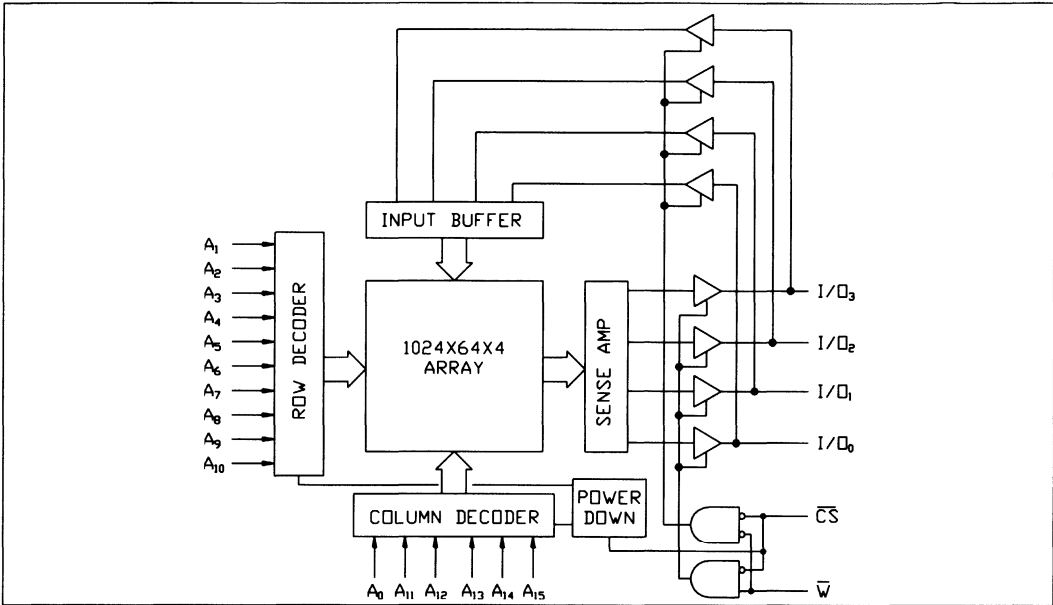
The HM-65798 is 100 % processed following the test methods of MIL STD 883C.

**PACKAGES**

Plastic 300 mils, 24 pins, DIL.  
Ceramic 300 mils, 24 pins, DIL.  
SO/SOJ 300, 24 pins.  
Tape and Reel Service  
LCC 28 pins

**Pinout DIL 24 pins (top view)****LOGIC SYMBOL**

BLOCK DIAGRAM



PIN NAMES

|                          |                          |
|--------------------------|--------------------------|
| A0-A15 : Address inputs  | $\bar{W}$ : Write enable |
| I/O0-I/O3 : Input/Output | Vcc : Power              |
| $\bar{CS}$ : Chip Select | GND : Ground             |

TRUTH TABLE

| $\bar{CS}$ | $\bar{W}$ | INPUT/OUTPUTS | MODE                |
|------------|-----------|---------------|---------------------|
| H          | X         | High Z        | Deselect/Power down |
| L          | H         | Data Out      | Read                |
| L          | L         | Data In       | Write               |

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... - 0.5 V to + 7.0 V  
DC input voltage..... - 3.0 V to + 7.0 V  
CD output voltage in high Z state .... - 0.5 V to + 7.0 V  
Storage temperature ..... - 65°C to + 150°C  
Output current into outputs (low) ..... 20mA  
Electro static discharge voltage ..... > 2000V (MIL STD 883C method 3015.2)

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

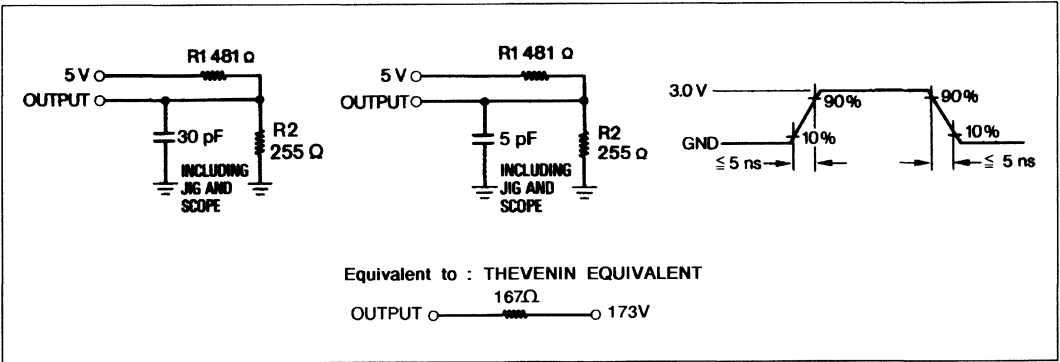
4

CAPACITANCE

| PARAMETER | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|------------------------|---------|---------|---------|------|
| Cin       | (1) Input capacitance  | -       | -       | 5       | pF   |
| Cout      | (1) Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS



**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|------------------------------|---------|---------|---------|---------|
| IIX (2)   | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ (3)   | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS (3)   | Output short circuit current | -       | -       | - 350.0 | mA      |
| VOL (4)   | Output low voltage           | -       | -       | 0.4     | V       |
| VOH (5)   | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION :**

| SYMBOL     | PARAMETER                 | 65798<br>H-5 | 65798<br>K-5 | 65798<br>M-5 | 65798<br>N-5 | UNIT | VALUE |
|------------|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6)  | Standby supply current    | 35           | 35           | 35           | 35           | mA   | max   |
| ICCSB1 (8) | Standby supply current    | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP (7)  | Dynamic operating current | 120          | 120          | 120          | 120          | mA   | max   |

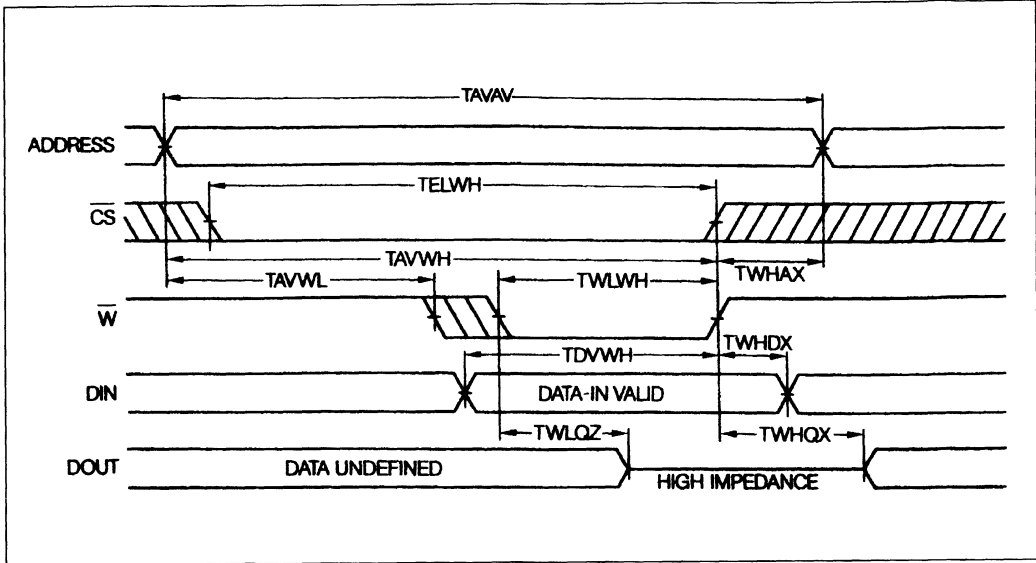
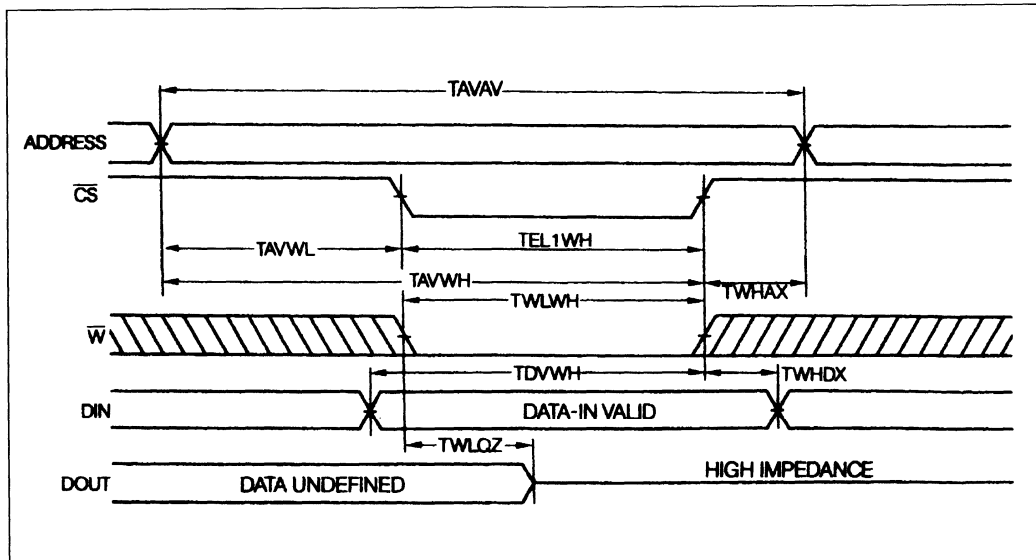
**CONSUMPTION FOR INDUSTRIAL (- 9) AND MILITARY (-2) SPECIFICATION :**

| SYMBOL     | PARAMETER                 | 65798<br>K-9/-2 | 65798<br>M-9/-2 | 65798<br>N-9/-2 | UNIT | VALUE |
|------------|---------------------------|-----------------|-----------------|-----------------|------|-------|
| ICCSB (6)  | Standby supply current    | 35              | 35              | 35              | mA   | max   |
| ICCSB1 (8) | Standby supply current    | 20              | 20              | 20              | mA   | max   |
| ICCOP (7)  | Dynamic operating current | 130             | 130             | 130             | mA   | max   |

- Notes :**
6.  $CS \geq V_{IH}$ , a pull-up resistor to  $V_{cc}$  on the CS is required to keep the device unselected during the  $V_{cc}$  power-up. Otherwise, ICCSB will exceed the above values. Min duty cycle = 100 %.
  7.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or Gnd.
  8.  $CS \geq V_{cc} - 0.3 V_{lout} = 0 \text{ mA}$ .





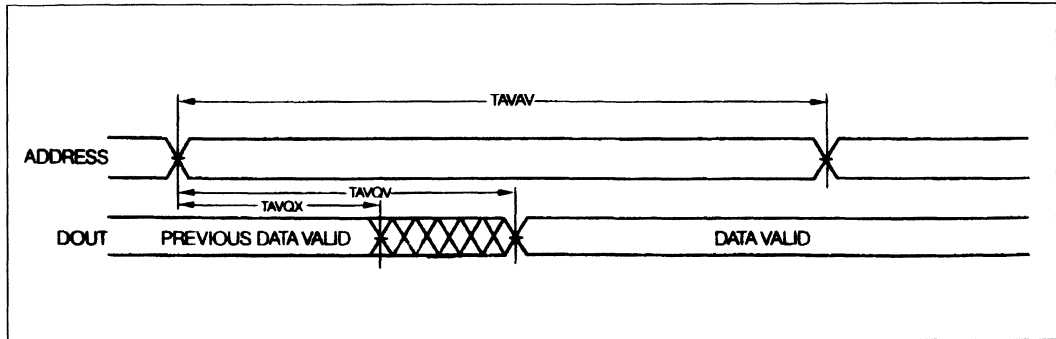
WRITE CYCLE 1 :  $\overline{W}$  controlled (note 9)WRITE CYCLE 2 :  $\overline{CS}$  controlled (note 9)

**Note :** 9. The internal write of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

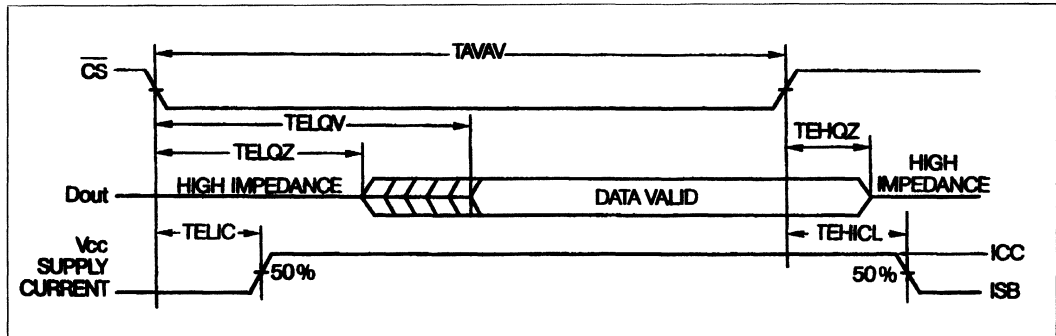
READ CYCLE specification : Commercial, Industrial and Military

| SYMBOL | PARAMETER               | 65798<br>H-5/-9/-2 | 65798<br>K-5/-9/-2 | 65798<br>M-5/-9/-2 | 65798<br>N-5/-9/-2 | UNIT | VALUE |
|--------|-------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV  | READ cycle time         | 25                 | 35                 | 45                 | 55                 | ns   | min   |
| TAVQV  | Address access time     | 25                 | 35                 | 45                 | 55                 | ns   | max   |
| TAVQX  | Address valid to low Z  | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TELQV  | Chip-select access time | 25                 | 35                 | 45                 | 55                 | ns   | max   |
| TELQX  | CS low to low Z         | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TEHQZ  | CS high to high Z       | 13                 | 15                 | 20                 | 25                 | ns   | max   |
| TELIC  | CS low to power up      | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TEHICL | CS high to power down   | 25                 | 35                 | 45                 | 55                 | ns   | max   |

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



- Notes : 10. W is high for read cycle.  
 11. Device is continuously selected,  $\overline{CS} = V_{IL}$ .  
 12. Address valid prior or coincident with CS transition low.

## ORDERING INFORMATION

| Package                      | Device Type                    | Grade     | Level                   |
|------------------------------|--------------------------------|-----------|-------------------------|
| HM1                          | 65798                          | H         | - 5 : R                 |
|                              | 64 k x 4 high speed static RAM |           | Tape & Reel Service     |
| 0 - Chip form                |                                | H = 25 ns | - 5 : Commercial        |
| 1 - Ceramic 24 pins 300 mils |                                | K = 35 ns | - 9 : Industrial        |
| 3 - Plastic 24 pins 300 mils |                                | M = 45 ns | - 2 : Military          |
| T - SOIC 24 pins 300 mils    |                                | N = 55 ns | - 8 : Military with B.I |
| U - SOJ 24 pins              |                                |           |                         |
| 4 - LCC 28 pins              |                                |           | (B.I : Burn-In)         |

4

## DATA SHEET

## HM 65799

64 K x 4 WITH  $\overline{\text{OE}}$  HIGH SPEED CMOS SRAM

## FEATURES

- FAST ACCESS TIME
  - INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  - COMMERCIAL : 25/35/45/55 ns (max)
- LOW POWER CONSUMPTION
  - ACTIVE : 600 mW
  - STANDBY : 193 mW
- WIDE TEMPERATURE RANGE :
  - 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- OUTPUT ENABLE
- SINGLE 5 VOLT SUPPLY

4

## DESCRIPTION

The HM-65799 is a high speed CMOS static RAM organised as 65,536 X 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 660 mW.

The HM-65799 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip selects (CS1, CS2), an active low output enable ( $\overline{\text{OE}}$ ) and three state drivers.

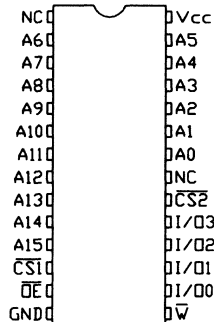
All inputs and outputs of the HM-65799 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65799 is processed following the test methods of MIL STD 883C.

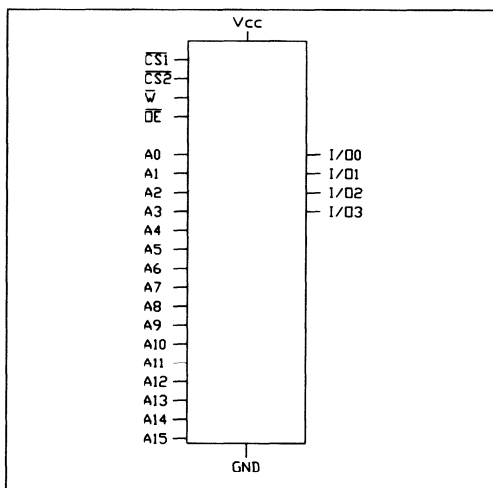
## PACKAGES

Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins, DIL.  
SO/SOJ 300 mils, 28 pins.  
Tape and Reel Service

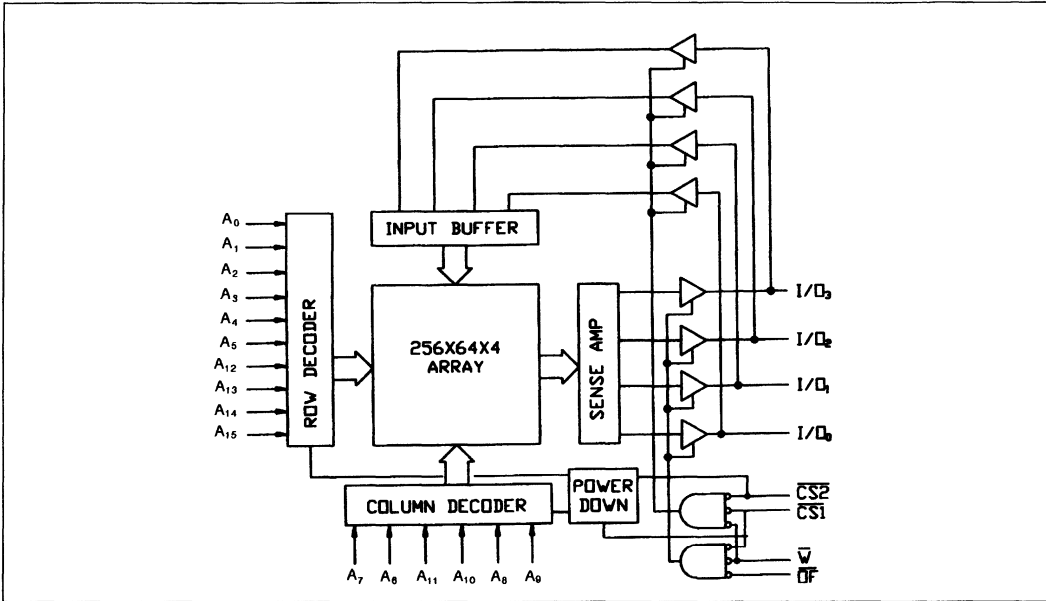
## Pinout DIL 28 pins (top view)



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                  |                  |                 |                 |
|------------------|------------------|-----------------|-----------------|
| A0-A15           | : Address inputs | $\overline{OE}$ | : Output Enable |
| I/O0-I/O3        | : Input/Output   | $\overline{W}$  | : Write enable  |
| $\overline{CS1}$ | : Chip select 1  | Vcc             | : Power         |
| $\overline{CS2}$ | : Chip Select 2  | GND             | : Ground        |

TRUTH TABLE

| CS1 | CS2 | $\overline{W}$ | $\overline{OE}$ | INPUT/OUTPUTS | MODE                |
|-----|-----|----------------|-----------------|---------------|---------------------|
| H   | X   | X              | X               | High Z        | Deselect/Power Down |
| X   | H   | X              | X               |               |                     |
| L   | L   | H              | L               | Data Out      | Read                |
| L   | L   | L              | X               | Data In       | Write               |
| L   | L   | H              | H               | High Z        | Deselect            |

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... - 0.5 V to + 7.0 V  
DC input voltage..... - 3.0 V to + 7.0 V  
DC output voltage in high Z state..... - 0.5 V to + 7.0 V  
Storage temperature..... - 65°C to + 150°C  
Output current into outputs (low)..... 20 mA  
Electro static discharge voltage..... > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

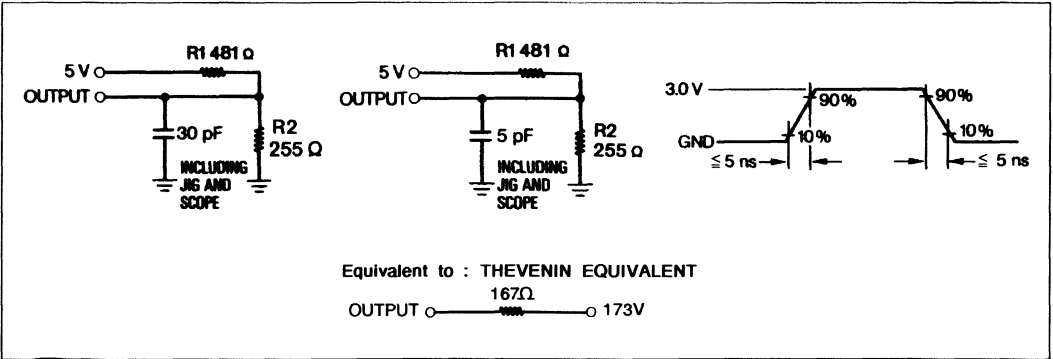
4

CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (1)  | Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS



**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|-----|------------------------------|---------|---------|---------|------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | μA   |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | μA   |
| IOS       | (3) | Output short circuit current | -       | -       | - 350.0 | mA   |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V    |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V    |

**Notes :** 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.

3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.

Not more than 1 output should be shorted at one time.

4. Vcc min, IOL = 8.0 mA.

5. Vcc min, IOH = - 4.0 mA.

**CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65799<br>H-5 | 65799<br>K-5 | 65799<br>M-5 | 65799<br>N-5 | UNIT | VALUE |
|--------|-----|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35           | 35           | 35           | 35           | mA   | max   |
| ICCSB1 | (8) | Standby supply current    |              | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (7) | Dynamic operating current | 120          | 120          | 120          | 120          | mA   | max   |

**CONSUMPTION FOR INDUSTRIAL (- 9) AND MILITARY (-2) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65799<br>K-9/-2 | 65799<br>M-9/-2 | 65799<br>N-9/-2 | UNIT | VALUE |
|--------|-----|---------------------------|-----------------|-----------------|-----------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35              | 35              | 35              | mA   | max   |
| ICCSB1 | (8) | Standby supply current    | 20              | 20              | 20              | mA   | max   |
| ICCOP  | (7) | Dynamic operating current | 130             | 130             | 130             | mA   | max   |

**Notes :** 6. CS ≥ VIH, a pull-up resistor to Vcc on the CS is required to keep the device unselected during the Vcc power-up. Otherwise IccSB will exceed the above values. Min duty cycle = 100 %.

7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

8. CS ≥ Vcc - 0.3 V = 0 mA.



**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels Gnd to 3.0 V  
 Input rise 5 ns

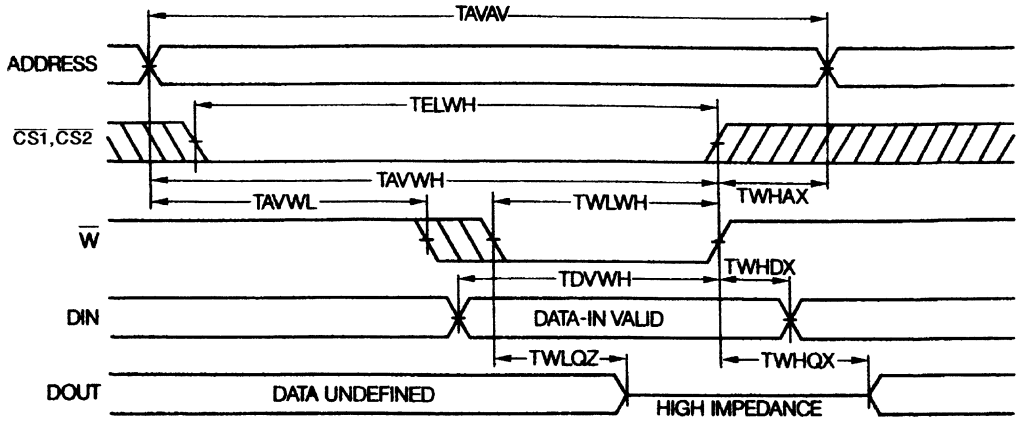
Input timing reference levels 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) + 30 pF

**WRITE CYCLE specification : Commercial, Industrial and Military**

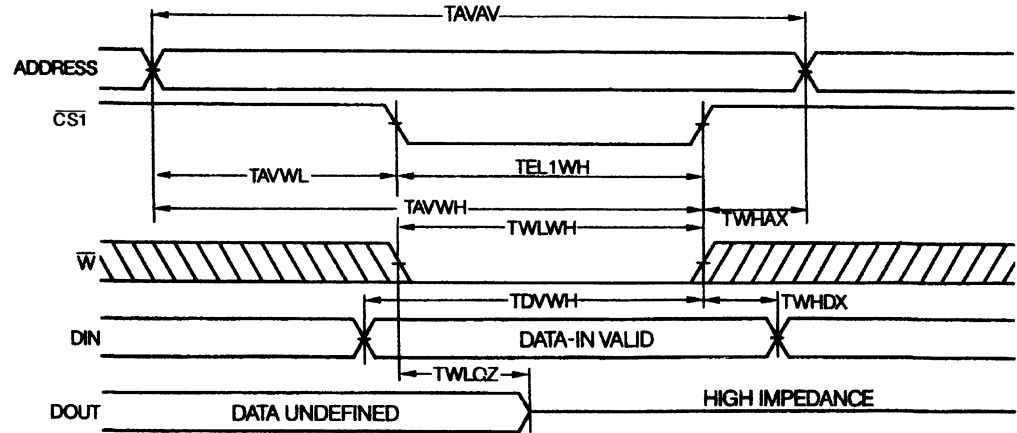
| SYMBOL    | PARAMETER                   | 65799<br>H-5/-9/-2 | 65799<br>K-5/-9/-2 | 65799<br>M-5/-9/-2 | 65799<br>N-5/-9/-2 | UNIT | VALUE |
|-----------|-----------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV     | Write cycle time            | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TAVWL     | Address set-up time         | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TAVWH     | Address valid to write end  | 20                 | 25                 | 35                 | 40                 | ns   | min   |
| TDVWH     | Data set-up time            | 15                 | 17                 | 20                 | 25                 | ns   | min   |
| TELWH     | CS1, CS2 low to write end   | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TWLQZ (8) | Write low to high Z         | 13                 | 15                 | 20                 | 25                 | ns   | max   |
| TWLWH     | Write pulse width           | 20                 | 25                 | 30                 | 35                 | ns   | min   |
| TWHAX     | Address hold from write end | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHDX     | Data hold time              | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHQX (8) | Write high to low Z         | 3                  | 3                  | 3                  | 3                  | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 :  $\overline{W}$  controlled (note 9)



WRITE CYCLE 2 :  $\overline{CS}$  controlled (note 9)

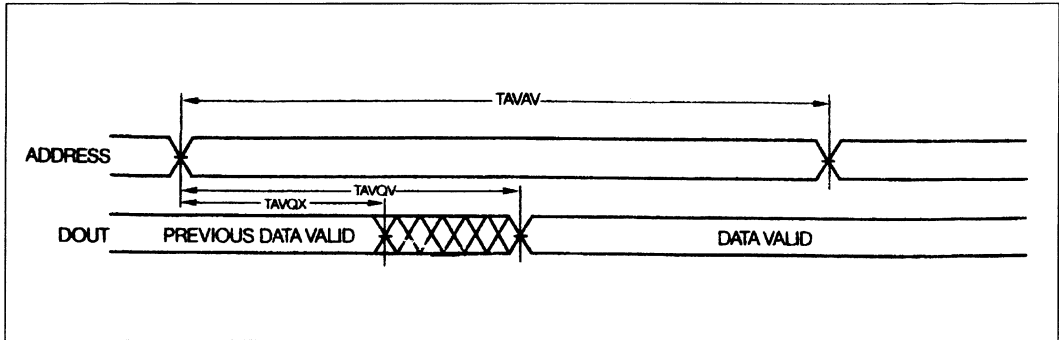


**Note :** 9. The internal write of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if OE = VIH.

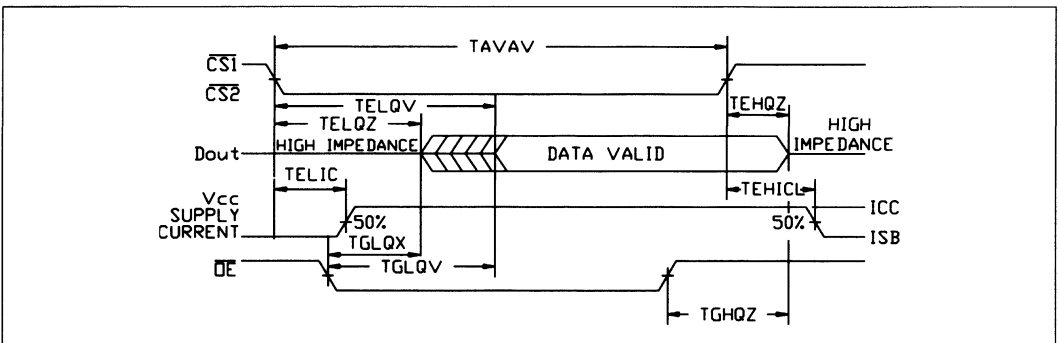
## READ CYCLE specification : Commercial, Industrial and Military

| SYMBOL | PARAMETER                                            | 65799<br>H-5/-9/-2 | 65799<br>K-5/-9/-2 | 65799<br>M-5/-9/-2 | 65799<br>N-5/-9/-2 | UNIT | VALUE |
|--------|------------------------------------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV  | READ cycle time                                      | 25                 | 35                 | 45                 | 55                 | ns   | min   |
| TAVQV  | Address access time                                  | 25                 | 35                 | 45                 | 55                 | ns   | min   |
| TAVQX  | Address valid to low Z                               | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TELQV  | $\overline{CS1}$ and $\overline{CS2}$ access time    | 25                 | 35                 | 45                 | 55                 | ns   | max   |
| TELQX  | $\overline{CS1}$ and $\overline{CS2}$ low to low Z   | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TEHQZ  | $\overline{CS1}$ and $\overline{CS2}$ high to high Z | 13                 | 15                 | 20                 | 25                 | ns   | max   |
| TGLQV  | $\overline{OE}$ access time                          | 15                 | 20                 | 20                 | 25                 | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z                         | 3                  | 3                  | 3                  | 3                  | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z                       | 15                 | 15                 | 20                 | 25                 | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up                      | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down                   | 25                 | 35                 | 45                 | 55                 | ns   | max   |

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



- Notes :** 10.  $\overline{W}$  is high for read cycle.  
 11. Device is continuously selected,  $\overline{CS1} = \text{VIL}$ ,  $\overline{CS2} = \text{VIL}$ ,  $\overline{OE} = \text{VIL}$   
 12. Address valid prior or coincident with  $\overline{CS1}$ ,  $\overline{CS2}$  transition low.

ORDERING INFORMATION

| Package                      | Device Type                            | Grade     | Level                  |
|------------------------------|----------------------------------------|-----------|------------------------|
| HM1                          | 65799                                  | H         | -5 : R                 |
|                              | 64 k x 4 high speed static RAM with OE |           | Tape & Reel Service    |
| 0 - Chip form                |                                        | H = 25 ns | -5 : Commercial        |
| 1 - Ceramic 28 pins 300 mils |                                        | K = 35 ns | -9 : Industrial        |
| 3 - Plastic 28 pins 300 mils |                                        | M = 45 ns | -2 : Military          |
| T - SOIC 28 pins 300 mils    |                                        | N = 55 ns | -8 : Military with B.I |
| U - SOJ 28 pins              |                                        |           |                        |
| (B.I : Burn In)              |                                        |           |                        |

## DATA SHEET

## HM 65795

# 64 K x 4 WITH SEPARATE I/O HIGH SPEED CMOS SRAM

## FEATURES

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**  
ACTIVE : 385 mW (typ)  
STANDBY : 100 mW (typ)
- **WIDE TEMPERATURE RANGE :**  
– 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SEPARATE INPUTS/OUTPUTS**
- **SINGLE 5 VOLT SUPPLY**

4

## DESCRIPTION

The HM-65795 is a high speed CMOS static RAM organised as 65,536 x 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW.

The HM-65795 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

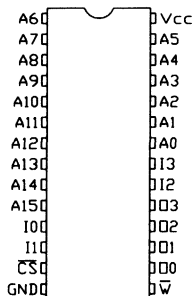
All inputs and outputs of the HM-65795 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65795 is processed following the test methods of MIL STD 883C.

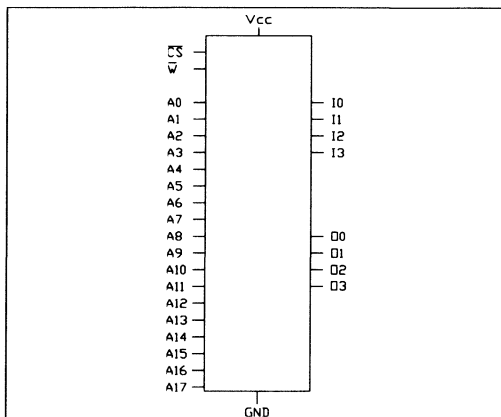
## PACKAGES

Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins.  
SO/SOJ 300, 28 pins  
Tape and Reel Service

## Pinout DIL 28 pins (top view)



## LOGIC SYMBOL





## DATA SHEET

## HM 65796

# 64 K x 4 WITH SEPARATE I/O HIGH SPEED CMOS SRAM AND TRANSPARENT WRITE

## FEATURES

- FAST ACCESS TIME  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 25/35/45/55 ns (max)
- LOW POWER CONSUMPTION  
ACTIVE : 385 mW (typ)  
STANDBY : 100 mW (typ)
- WIDE TEMPERATURE RANGE :  
- 55°C TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SEPARATE INPUTS/OUTPUTS
- TRANSPARENT WRITE
- SINGLE 5 V SUPPLY

4

## DESCRIPTION

The HM-65796 is a high speed CMOS static RAM organised as 65,536 x 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 330 mW

The HM-65796 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ( $\overline{CS}$ ) and three state drivers.

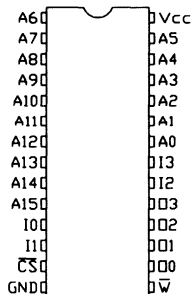
All inputs and outputs of the HM-65796 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65796 is processed following the test methods of MIL STD 883C.

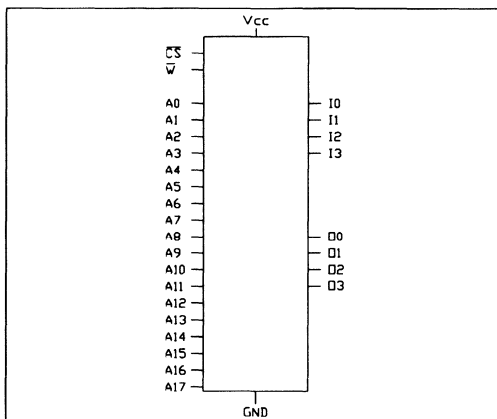
## PACKAGES

Plastic 300 mils, 28 pins, DIL.  
Ceramic 300 mils, 28 pins, DIL.  
SO/SOJ 300, 28 pins, DIL.  
Tape and Reel Service

## Pinout DIL 28 pins (top view)



## LOGIC SYMBOL







## DATA SHEET

## HM 65756

## 32 K x 8 HIGH SPEED CMOS SRAM

## FEATURES

- **FAST ACCESS TIME**  
INDUSTRIAL/MILITARY : 35/45/55 ns (max)  
COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**  
ACTIVE : 825 mW  
STANDBY : 193 mW
- **WIDE TEMPERATURE RANGE :**  
- 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **OUTPUT ENABLE**
- **SINGLE 5 VOLT SUPPLY**

4

## DESCRIPTION

The HM-65756 is a high speed CMOS static RAM organised as 32,768 X 8 bits. It is manufactured using MHS's high performance CMOS technology.

Access time as fast as 25 ns are available with maximum power consumption of only 825 mW.

The HM-65756 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) an active low output enable (OE), and three state drivers.

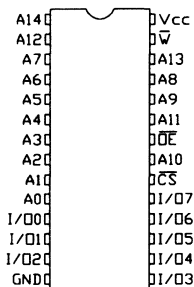
All inputs or outputs of the HM-65756 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65756 is processed following the test methods of MIL STD 883C.

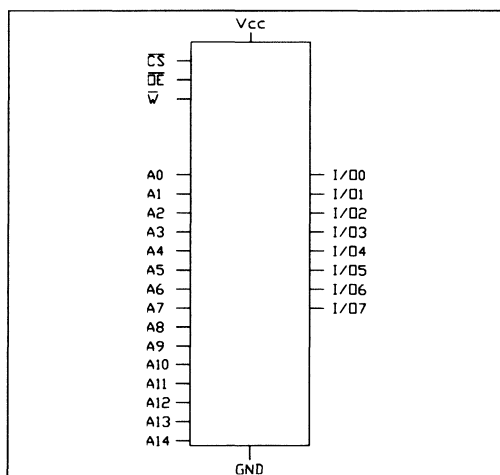
## PACKAGES

Plastic 300 and 600 mils, 28 pins, DIL.  
Ceramic 300 and 600 mils, 28 pins, DIL.  
SOIC 300, 28 pins.  
SOJ 300 mils, 28 pins.  
LCC 28 pins and 32 pins.  
Tape and Reel Service.

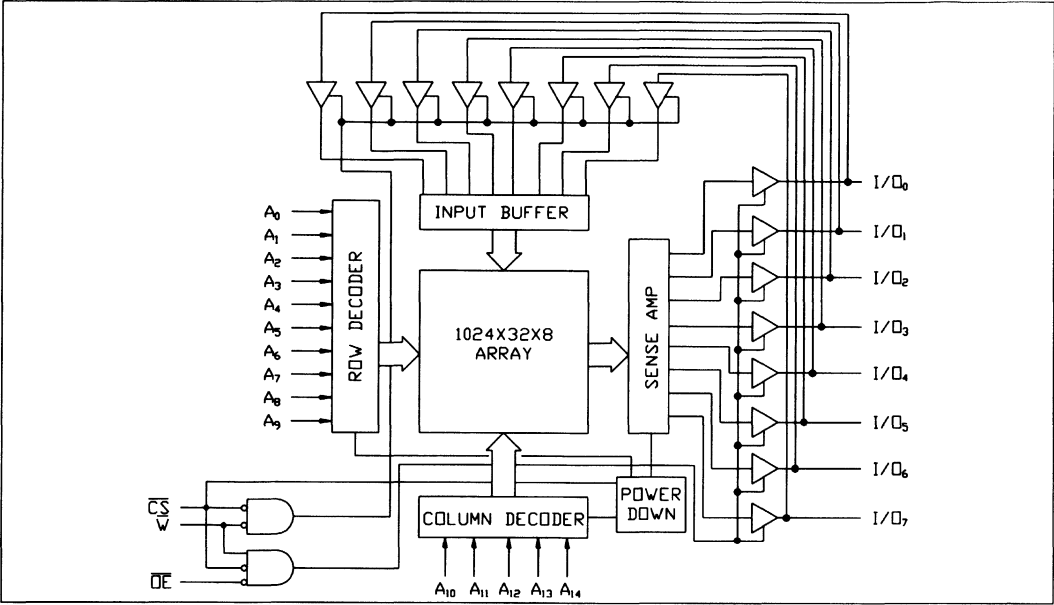
## Pinout DIL 28 pins



## LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

|                            |                                        |
|----------------------------|----------------------------------------|
| A0-A14 : Address inputs    | $\overline{\text{CS}}$ : Chip Select   |
| I/O0-I/O7 : Inputs/Outputs | $\overline{\text{OE}}$ : Output enable |
| VCC : Power                | $\overline{\text{W}}$ : Write enable   |
| GND : Ground               |                                        |

TRUTH TABLE

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{W}}$ | INPUT/OUTPUT | MODE                |
|------------------------|------------------------|-----------------------|--------------|---------------------|
| H                      | X                      | X                     | Z            | Deselect/Power down |
| L                      | L                      | H                     | Output       | Read                |
| L                      | X                      | L                     | Input        | Write               |
| L                      | H                      | H                     | Z            | Output Disable      |

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... - 0.5 V to + 7.0 V  
DC input voltage..... - 3.0 V to + 7.0 V  
DC output voltage in high Z state .... - 0.5 V to + 7.0 V  
Storage temperature ..... - 65°C to + 150°C  
Output current into outputs (low) ..... 20 mA  
Electro static discharge voltage ..... 2000 V ( MIL STD 883C method 3015.2)

OPERATING RANGE

|            |       | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military   | (- 2) | 5 V ± 10 %        | - 55°C to + 125°C     |
| Industrial | (- 9) | 5 V ± 10 %        | - 40°C to + 85°C      |
| Commercial | (- 5) | 5 V ± 10 %        | 0°C to + 70°C         |

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5     | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0     | V    |
| VIL       | Input low voltage  | - 3.0   | 0.0     | 0.8     | V    |
| VIH       | Input high voltage | 2.2     | -       | VCC     | V    |

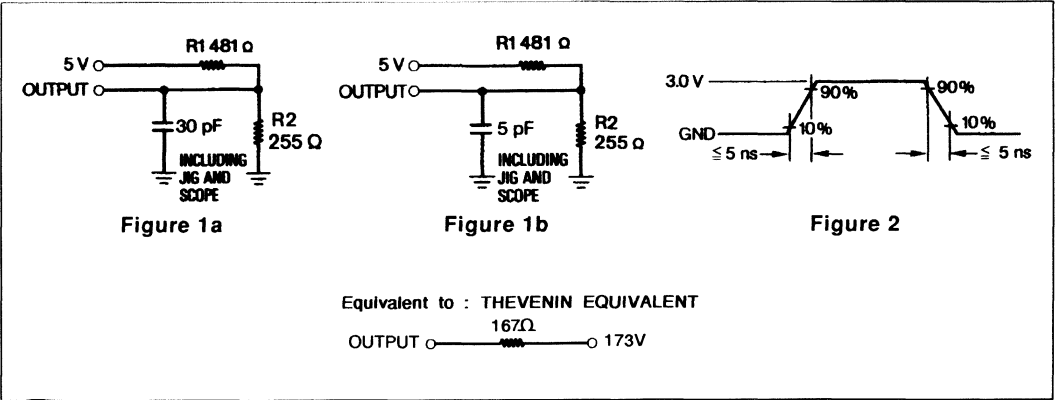
4

CAPACITANCE

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1)   | Input capacitance  | -       | -       | 5       | pF   |
| Cout (1)  | Output capacitance | -       | -       | 7       | pF   |

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS



**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION                  | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------------|---------|---------|---------|---------|
| IIX       | (2) | Input leakage current        | - 10.0  | -       | 10.0    | $\mu$ A |
| IOZ       | (3) | Output leakage current       | - 10.0  | -       | 10.0    | $\mu$ A |
| IOS       | (3) | Output short circuit current | -       | -       | - 300.0 | mA      |
| VOL       | (4) | Output low voltage           | -       | -       | 0.4     | V       |
| VOH       | (5) | Output high voltage          | 2.4     | -       | -       | V       |

- Notes :**
2.  $Gnd < V_{in} < V_{cc}$ ,  $Gnd < V_{out} < V_{cc}$  Output disabled.
  3.  $V_{cc} = \max$ ,  $V_{out} = Gnd$ , duration of the short circuit should not exceed 30 seconds.  
Not more than 1 output should be shorted at one time.
  4.  $V_{cc} \min$ ,  $I_{OL} = 8.0 \text{ mA}$ .
  5.  $V_{cc} \min$ ,  $I_{OH} = - 4.0 \text{ mA}$ .

**CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65756<br>H-5 | 65756<br>K-5 | 65756<br>M-5 | 65756<br>N-5 | UNIT | VALUE |
|--------|-----|---------------------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35           | 35           | 35           | 35           | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20           | 20           | 20           | 20           | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 170          | 150          | 150          | 150          | mA   | max   |

**CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (– 2) SPECIFICATION :**

| SYMBOL |     | PARAMETER                 | 65756<br>K-9/-2 | 65756<br>M-9/-2 | 65756<br>N-9/-2 | UNIT | VALUE |
|--------|-----|---------------------------|-----------------|-----------------|-----------------|------|-------|
| ICCSB  | (6) | Standby supply current    | 35              | 35              | 35              | mA   | max   |
| ICCSB1 | (7) | Standby supply current    | 20              | 20              | 20              | mA   | max   |
| ICCOP  | (8) | Dynamic operating current | 160             | 160             | 160             | mA   | max   |

- Notes :**
6.  $\overline{CS} \geq V_{IH}$ , a pull-up resistor to  $V_{cc}$  on the  $\overline{CS}$  is required to keep the device unselected during the  $V_{cc}$  power-up. Otherwise ICCSB will exceed the above value. Min duty cycle = 100 %.
  7.  $\overline{CS} \geq V_{cc} - 0.3 \text{ V}$ .
  8.  $V_{cc} \max$ , Output current = 0 mA,  $f = \max$ ,  $V_{in} = V_{cc}$  or  $Gnd$ .

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels Gnd to 3.0 V  
 Input rise 5 ns

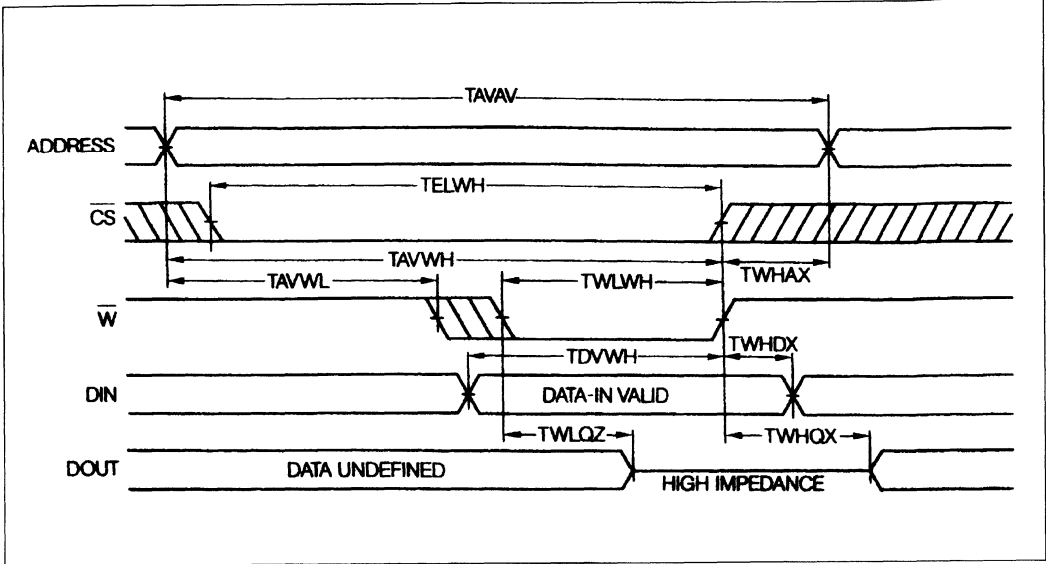
Input timing reference levels 1.5 V  
 Output loading IOL/IOH (see figure 1a and 1b) + 30 pF

**WRITE CYCLE specification : Commercial, Industrial and Military**

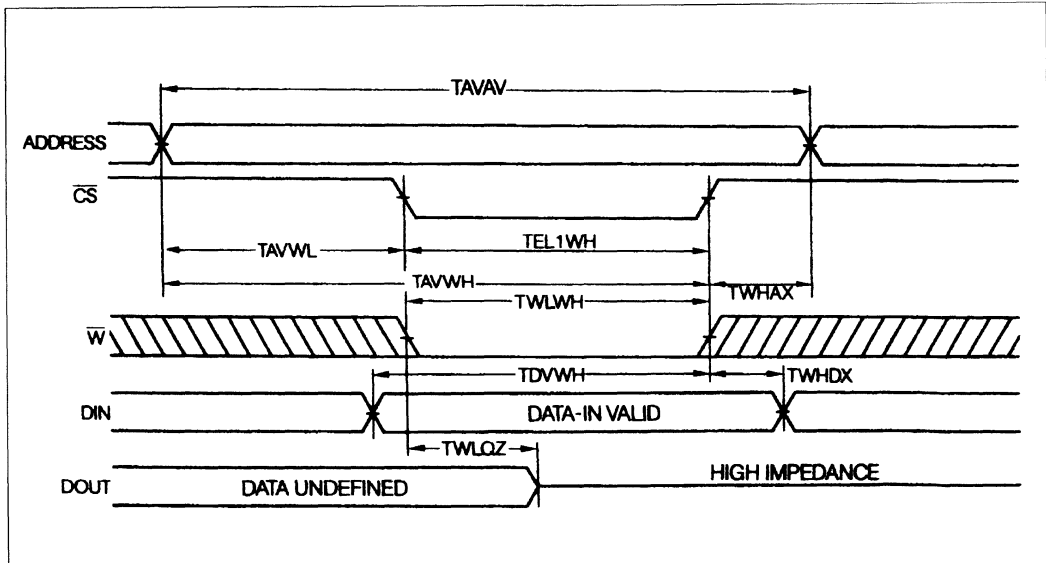
| SYMBOL    | PARAMETER                               | 65756<br>H-5/-9/-2 | 65756<br>K-5/-9/-2 | 65756<br>M-5/-9/-2 | 65756<br>N-5/-9/-2 | UNIT | VALUE |
|-----------|-----------------------------------------|--------------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV     | Write cycle time                        | 25                 | 35                 | 45                 | 50                 | ns   | min   |
| TAVWL     | Address set-up time                     | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TAVWH     | Address Valid to write end              | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TDVWH     | Data set-up time                        | 15                 | 17                 | 20                 | 25                 | ns   | min   |
| TELWH     | $\overline{\text{CS}}$ low to write end | 20                 | 30                 | 40                 | 50                 | ns   | min   |
| TWLQZ (8) | Write low to high Z                     | 13                 | 15                 | 20                 | 25                 | ns   | max   |
| TWLWH     | Write pulse width                       | 20                 | 25                 | 30                 | 40                 | ns   | min   |
| TWHAX     | Address hold from write end             | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHDX     | Data hold time                          | 0                  | 0                  | 0                  | 0                  | ns   | min   |
| TWHQX (8) | Write high to low Z                     | 3                  | 3                  | 3                  | 3                  | ns   | min   |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 :  $\overline{W}$  controlled (note 9)



WRITE CYCLE 2 :  $\overline{CS}$  controlled (note 9)

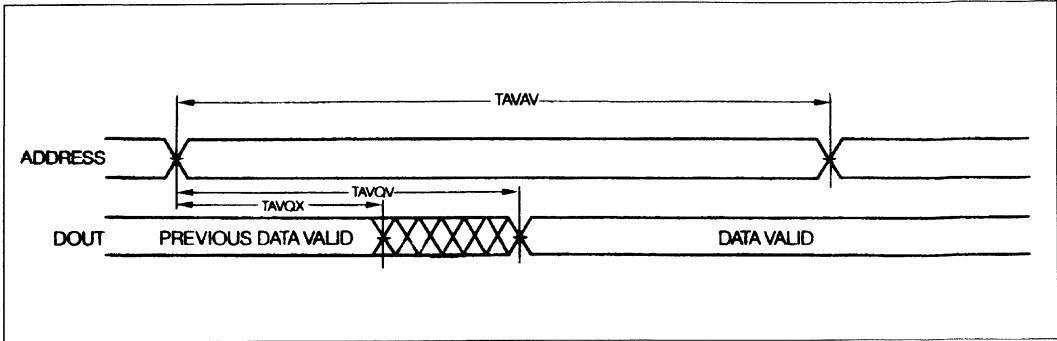


Note : 9. The internal write of the memory is defined by the overlap of CS LOW and  $\overline{W}$  LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if OE = VIH.

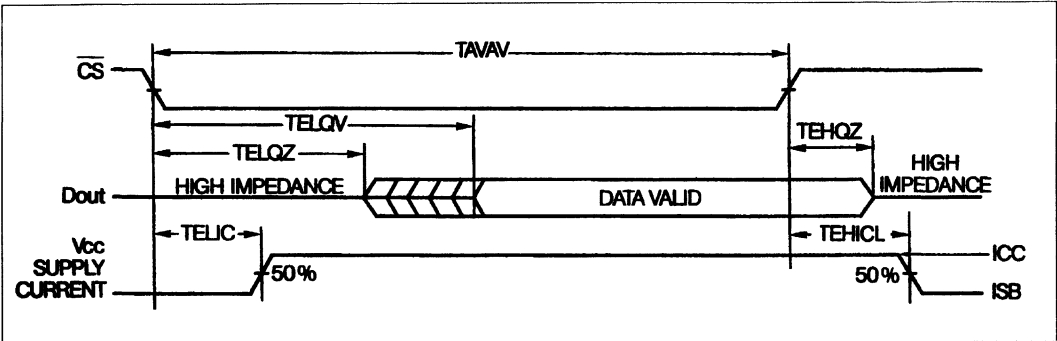
## READ CYCLE specification : Commercial, Industrial and Military

| SYMBOL | PARAMETER                          | 65756<br>H-5 | 65756<br>K-5/-9/-2 | 65756<br>M-5/-9/-2 | 65756<br>N-5/-9/-2 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------------|--------------------|--------------------|------|-------|
| TAVAV  | READ cycle time                    | 25           | 35                 | 45                 | 55                 | ns   | min   |
| TAVQV  | Address access time                | 25           | 35                 | 45                 | 55                 | ns   | max   |
| TAVQX  | Address Valid to low Z             | 3            | 3                  | 3                  | 3                  | ns   | min   |
| TELQV  | Chip-select access time            | 25           | 35                 | 45                 | 55                 | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z       | 3            | 3                  | 3                  | 3                  | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z     | 13           | 15                 | 20                 | 20                 | ns   | max   |
| TELIC  | $\overline{CS}$ low to power up    | 0            | 0                  | 0                  | 0                  | ns   | min   |
| TEHICL | $\overline{CS}$ high to power down | 20           | 20                 | 25                 | 25                 | ns   | max   |
| TGLQV  | Output enable access time          | 15           | 20                 | 20                 | 20                 | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z       | 3            | 3                  | 3                  | 3                  | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z     | 13           | 15                 | 20                 | 25                 | ns   | max   |

READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10.  $\overline{W}$  is high for read cycle.  
11. Device is continuously selected,  $\overline{CS} = \text{VIL}$ ,  $\overline{OE} = \text{VIL}$ .  
12. Address valid prior or coincident with CS transition low.

ORDERING INFORMATION

| Package                           | Device Type                    | Grade     | Level                   |
|-----------------------------------|--------------------------------|-----------|-------------------------|
| HM1                               | 65756                          | K         | - 5 : R                 |
|                                   | 32 k x 8 high speed static RAM |           | Tape & Reel Service     |
| 0 - Chip form                     |                                | H = 25 ns | - 5 : Commercial        |
| 1 - Ceramic 28 pins 300 mils      |                                | K = 35 ns | - 9 : Industrial        |
| 1E - Ceramic 28 pins 600 mils     |                                | M = 45 ns | - 2 : Military          |
| 3 - Plastic 28 pins 300 mils      |                                | N = 55 ns | - 8 : Military with B.I |
| 3E - Plastic 28 pins 600 mils     |                                |           |                         |
| 4P - LCC 28 pins/4J - LCC 32 pins |                                |           | (B.I : Burn-In)         |
| T - SOIC 28 pins 300 mils         |                                |           |                         |
| U - SOJ 28 pins                   |                                |           |                         |



# **HIGH SPEED BICMOS SRAM**

**5**







DATA SHEET

M-65864

8,192 x 8  
STATIC RAM

FEATURES

- BiCMOS FOR OPTIMUM SPEED/POWER
- HIGH SPEED
  - 12 ns
- LOW ACTIVE POWER
  - 600 mW
- LOW STANDBY POWER
  - 200 mW
- TTL-COMPATIBLE INPUTS AND OUTPUTS
- CAPABLE OF WITHSTANDING GREATER THAN 2001V ELECTROSTATIC DISCHARGE

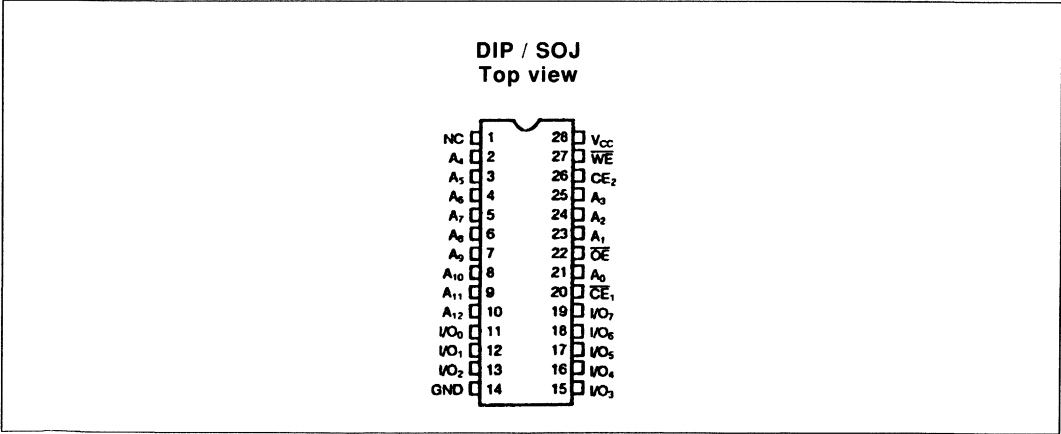
DESCRIPTION

The M-65864 is a high-performance BiCMOS static RAM organized as 8,192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE<sub>1</sub>), an active HIGH chip enable (CE<sub>2</sub>), and active LOW output enable (OE) and three-state drivers. Both devices have a power-down feature (CE<sub>1</sub>) that reduces the power consumption by 67 % when deselected. An active LOW write enable signal (WE) controls the writing/reading operation of the memory. When CE<sub>1</sub> and WE inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the

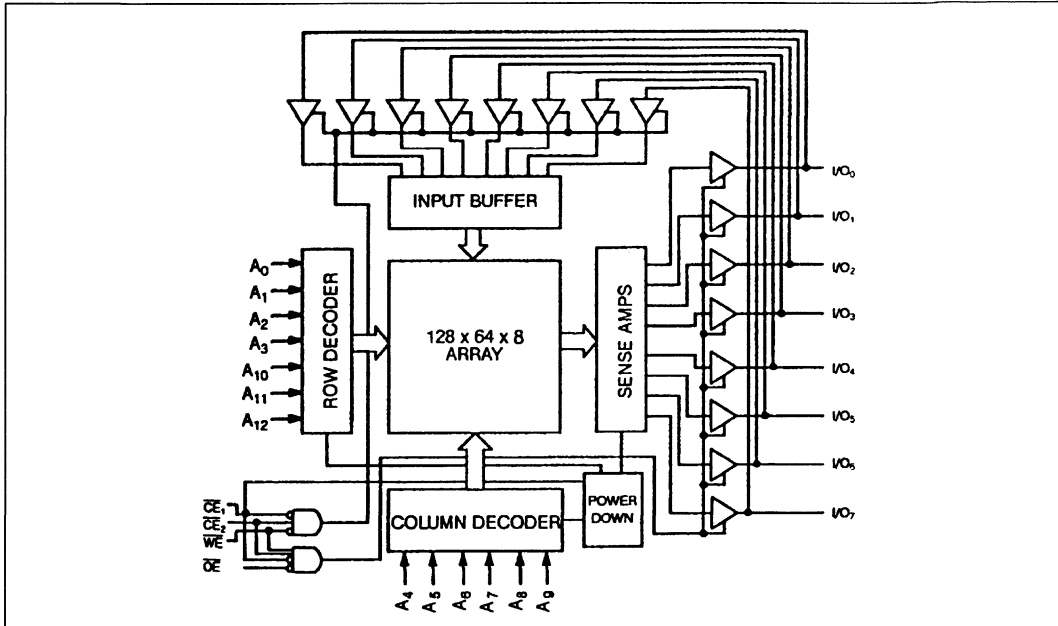
memory location addressed by (A<sub>0</sub> through A<sub>12</sub>). Reading the device is accomplished by selecting the device and enabling the outputs, CE<sub>1</sub> and OE active LOW, CE<sub>2</sub> active HIGH, while WE remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.

PACKAGES



## BLOCK DIAGRAM



## SELECTION GUIDE

|                                |            | M-65864-12 | M-65864-15 |
|--------------------------------|------------|------------|------------|
| Maximum Access Time (ns)       |            | 12         | 15         |
| Maximum Operating Current (mA) | Commercial | 140        | 135        |
|                                | Military   |            | 145        |
| Maximum Standby Current (mA)   | Commercial | 40         | 40         |
|                                | Military   |            | 50         |

5

## MAXIMUM RATING

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested)

Storage Temperature . . . . . - 65°C to + 150°C

Ambient Temperature with

Power Applied . . . . . - 55°C to + 125°C

Supply Voltage to

Ground Potential . . . . . - 0.5V to + 7.0V

DC Voltage Applied to Outputs

in High Z State . . . . . - 0.5 V to + 7.0 V

DC Input Voltage<sup>[1]</sup> . . . . . - 3.0 V to + 7.0 V

Output Current into Outputs (Low) . . . 20 mA

Static Discharge Voltage . . . . . > 2001 V

(per MIL-STD-883, Method 3015)

Latch-up Current . . . . . > 200 mA

## OPERATING RANGE

| RANGE                   | AMBIENT TEMPERATURE | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to + 70°C       | 5 V ± 10 %      |
| Military <sup>[2]</sup> | - 55°C to + 125°C   | 5 V ± 10 %      |

**ELECTRICAL CHARACTERISTICS** over the operating range

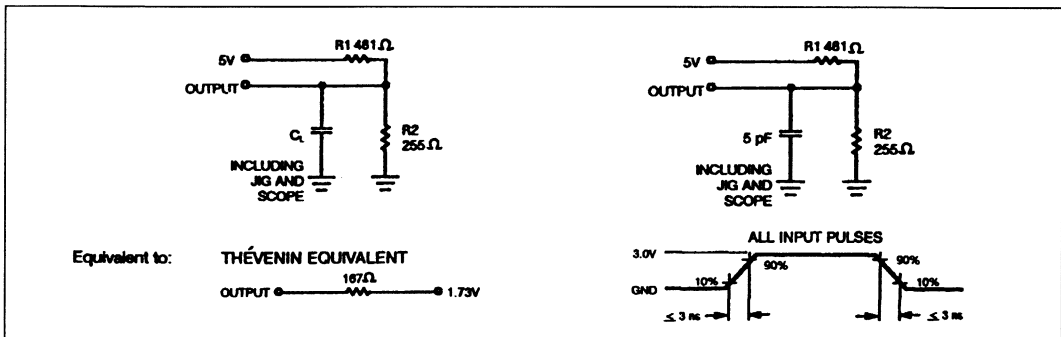
| PARAMETERS | DESCRIPTION                          | TEST CONDITIONS                                                                                 | M-65864-12 |          | M-65864-15 |          | UNITS         |
|------------|--------------------------------------|-------------------------------------------------------------------------------------------------|------------|----------|------------|----------|---------------|
|            |                                      |                                                                                                 | MIN.       | MAX.     | MIN.       | MAX.     |               |
| $V_{OH}$   | Output HIGH Voltage                  | $V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$ , Com'l<br>$I_{OH} = -2.0 \text{ mA}$ , Mil | 2.4        |          | 2.4        |          | V             |
| $V_{OL}$   | Output LOW Voltage                   | $V_{CC} = \text{Min.}$ , $I_{OL} = 8.0 \text{ mA}$                                              |            | 0.4      |            | 0.4      | V             |
| $V_{IH}$   | Input HIGH Level                     |                                                                                                 | 2.2        | $V_{CC}$ | 2.2        | $V_{CC}$ | V             |
| $V_{IL}$   | Input LOW Voltage <sup>[1]</sup>     |                                                                                                 | -0.5       | 0.8      | -0.5       | 0.8      | V             |
| $I_{IX}$   | Input Load Current                   | $GND \leq V_I \leq V_{CC}$                                                                      | -10        | +10      | -10        | +10      | $\mu\text{A}$ |
| $I_{OZ}$   | Output Leakage Current               | $GND \leq V_I \leq V_{CC}$ , Output Disabled                                                    | -10        | +10      | -10        | +10      | $\mu\text{A}$ |
| $I_{CC}$   | $V_{CC}$ Operating Supply Current    | $V_{CC} = \text{Max.}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{\text{max.}}$                       | Com'l      | 140      |            | 135      | mA            |
|            |                                      |                                                                                                 | Mil        |          |            | 145      | mA            |
| $I_{SB}$   | $\overline{CE}_1$ Power-Down Current | $\overline{CE}_1 \geq V_{IH}$                                                                   | Com'l      | 40       |            | 40       | mA            |
|            |                                      |                                                                                                 | Mil        |          |            | 50       | mA            |

**CAPACITANCE** <sup>[3]</sup>

| PARAMETERS | DESCRIPTION        | TEST CONDITIONS                                | MAX. <sup>[4]</sup> | UNITS |
|------------|--------------------|------------------------------------------------|---------------------|-------|
| $C_{IN}$   | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ | 5                   | pF    |
| $C_{OUT}$  | Output Capacitance | $V_{CC} = 5.0 \text{ V}$                       | 7                   | pF    |

- Notes** : 1.  $V_{IL}(\text{min}) = -3.0 \text{ V}$  for pulse width  $< 20 \text{ ns}$ .  
2.  $T_A$  is the "instant on" case temperature.  
3. Tested initially and after any design on process changes that may affect these parameters.  
4. For all packages except Cerdip, which has maximums of  $C_{IN} = 8 \text{ pF}$ ,  $C_{OUT} = 9 \text{ pF}$ .

**AC TEST LOADS AND WAVEFORMS**



**SWITCHING CHARACTERISTICS** Over the Operating Range <sup>[5]</sup>

| PARAMETERS                 | DESCRIPTION                                                                           | M-65864-12 |      | M-65864-15 |      | UNITS |
|----------------------------|---------------------------------------------------------------------------------------|------------|------|------------|------|-------|
|                            |                                                                                       | MIN.       | MAX. | MIN.       | MAX. |       |
| READ CYCLE                 |                                                                                       |            |      |            |      |       |
| t <sub>RC</sub>            | Read Cycle Time                                                                       | 12         |      | 15         |      | ns    |
| t <sub>AA</sub>            | Address to Data Valid                                                                 |            | 12   |            | 15   | ns    |
| t <sub>OHA</sub>           | Data Hold from Address Change                                                         | 3          |      | 3          |      | ns    |
| t <sub>ACE1</sub>          | $\overline{CE}_1$ LOW to Data Valid                                                   |            | 12   |            | 15   | ns    |
| t <sub>AE2</sub>           | $\overline{CE}_2$ HIGH to Data Valid                                                  |            | 12   |            | 15   | ns    |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                                                     |            | 8    |            | 10   | ns    |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z                                                          | 2          |      | 3          |      | ns    |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>                                         |            | 8    |            | 8    | ns    |
| t <sub>LZCE1</sub>         | $\overline{CE}_1$ to Low Z <sup>[7]</sup>                                             | 3          |      | 3          |      | ns    |
| t <sub>LZCE2</sub>         | $\overline{CE}_2$ HIGH to Low Z <sup>[7]</sup>                                        | 3          |      | 3          |      | ns    |
| t <sub>HZCE</sub>          | $\overline{CE}_1$ HIGH to High Z <sup>[5, 6]</sup><br>$\overline{CE}_2$ LOW to High Z |            | 7    |            | 8    | ns    |
| WRITE CYCLE <sup>(8)</sup> |                                                                                       |            |      |            |      |       |
| t <sub>WC</sub>            | Write cycle Time                                                                      | 12         |      | 15         |      | ns    |
| t <sub>SCE1</sub>          | $\overline{CE}_1$ LOW to Write End                                                    | 8          |      | 10         |      | ns    |
| t <sub>SCE2</sub>          | $\overline{CE}_2$ HIGH to Write End                                                   | 8          |      | 10         |      | ns    |
| t <sub>AW</sub>            | Address Set-Up to Write End                                                           | 8          |      | 10         |      | ns    |
| t <sub>HA</sub>            | Address Hold From Write End                                                           | 0          |      | 0          |      | ns    |
| t <sub>SA</sub>            | Address Set-Up to Write Start                                                         | 0          |      | 0          |      | ns    |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                                                           | 8          |      | 10         |      | ns    |
| t <sub>SD</sub>            | Data Set-Up to Write End                                                              | 6.5        |      | 8          |      | ns    |
| t <sub>HD</sub>            | Data Hold from Write End                                                              | 0          |      | 0          |      | ns    |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[5]</sup>                                          |            | 7    |            | 7    | ns    |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z                                                         | 3          |      | 3          |      | ns    |

**Notes :** 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$ , and  $C_L = 20$  pF.

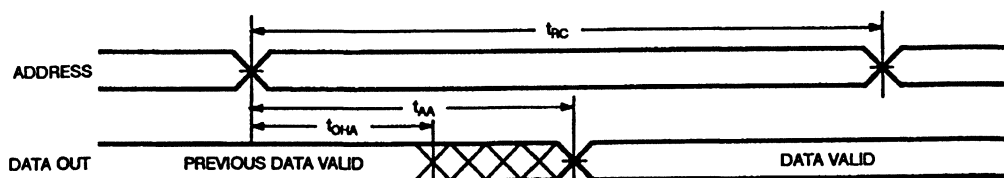
6.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test loads. Transition is measured  $\pm 200$  mV from steady-state voltage.

7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device.

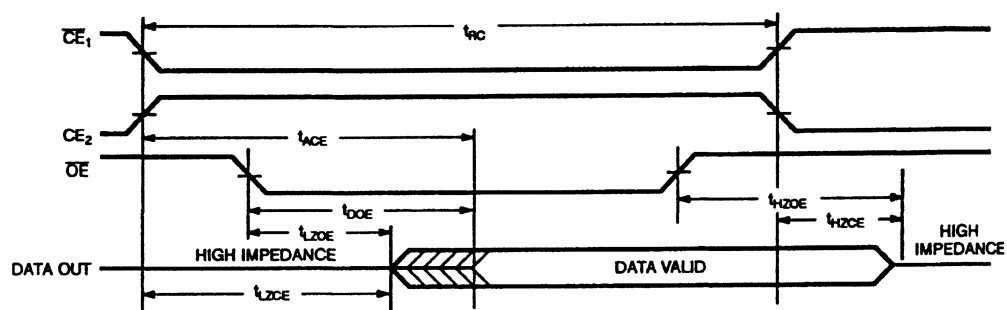
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and  $\overline{WE}$  LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

## SWITCHING WAVEFORMS

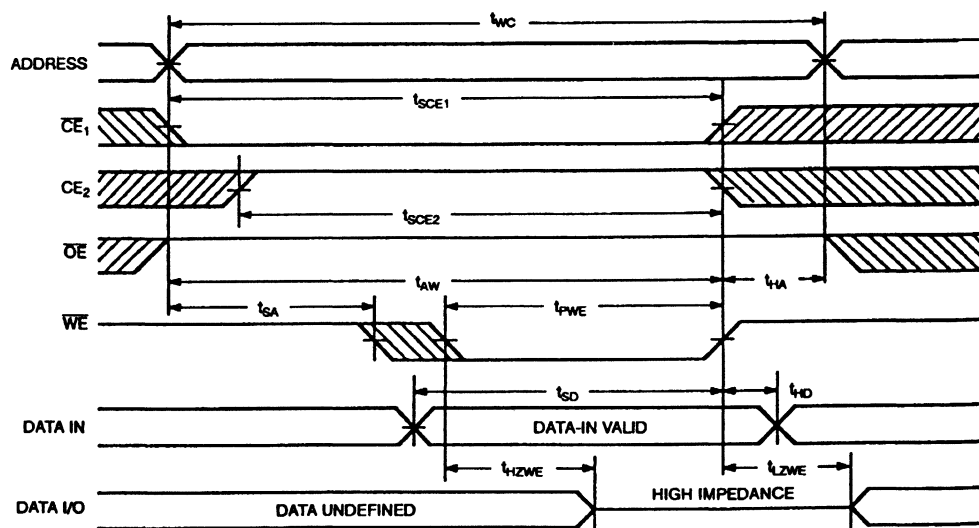
## READ CYCLE N° 1 (9, 10)



## READ CYCLE N° 2 (9, 11)



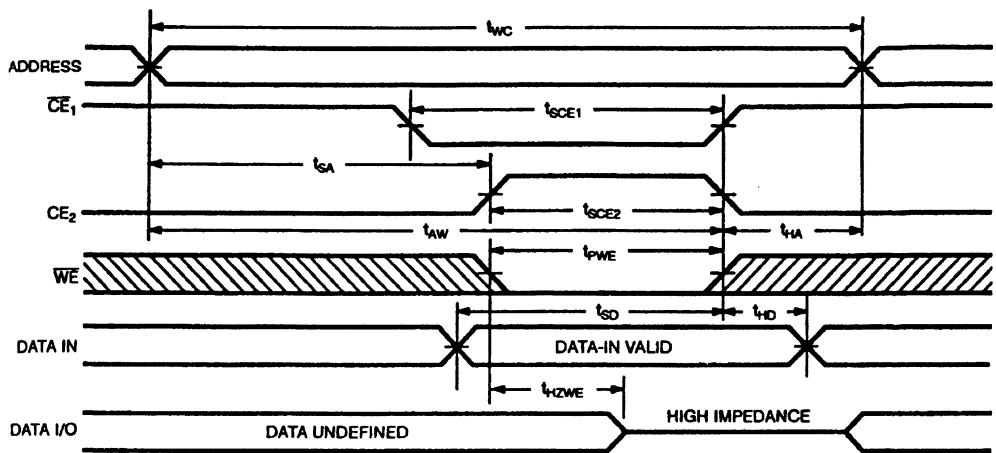
## WRITE CYCLE N° 1 (WE Controlled) (7, 12)



- Notes :
- 9. Device is continuously selected.  $\overline{OE}$ ,  $CE_1 = V_{IL}$ .  $CE_2 = V_{IH}$ .
  - 10. Address valid prior to or coincident with  $CE$  transition LOW.
  - 11.  $WE$  is HIGH for read cycle.
  - 12. Data I/O is HIGH impedance if  $\overline{OE} = V_{IH}$ .
  - 13. If  $CE$  goes HIGH simultaneously with  $WE$  HIGH, the output remains in a high-impedance state.

SWITCHING WAVEFORMS (continued)

WRITE CYCLE N° 2 ( $\overline{CE}$  controlled) (7, 11, 13)



- Notes :
- 9.  $\overline{WE}$  is HIGH for read cycle.
  - 10. Device is continuously selected,  $\overline{CE} = V_{IL}$ . (65889  $\overline{OE} = V_{IL}$  also).
  - 11. Address valid prior to or coincident with  $\overline{CE}$  transition low.
  - 12. 65889 only : Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .
  - 13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remain in a high-impedance state.

TRUTH TABLE

| $\overline{CE}_1$ | $\overline{CE}_2$ | $\overline{WE}$ | $\overline{OE}$ | INPUTS/<br>OUTPUTS | MODE                    |
|-------------------|-------------------|-----------------|-----------------|--------------------|-------------------------|
| H                 | X                 | X               | X               | High Z             | Deselect/<br>Power-Down |
| L                 | L                 | X               | X               | High Z             | Deselect                |
| L                 | H                 | H               | L               | Data Out           | Read                    |
| L                 | H                 | L               | X               | Data In            | Write                   |
| L                 | H                 | H               | H               | High Z             | Deselec                 |

ORDERING INFORMATION

|                |     |                 |             |            |
|----------------|-----|-----------------|-------------|------------|
|                | M   | 1               | 65864       | 12         |
|                | MHS |                 | Device Type | Speed      |
| C : Commercial |     | 0 : chip form   |             | 12 : 12 ns |
| M : Military   |     | 1 : ceramic     |             | 15 : 15 ns |
|                |     | 3 : Plastic Dil |             |            |
|                |     | U : SOJ         |             |            |



## DATA SHEET

## M-65888/889

# 16,384 x 4 Static R/W RAM

## FEATURES

- BiCMOS FOR OPTIMUM SPEED/POWER
- HIGH SPEED
  - 10 ns  $t_{AA}$
- LOW ACTIVE POWER
  - 600 mW
- LOW STANDBY POWER
  - 200 mW
- OUTPUT ENABLE ( $\overline{OE}$ ) FEATURE (65889)
- TTL-COMPATIBLE INPUTS AND OUTPUTS
- CAPABLE OF WITHSTANDING GREATER THAN 2001V ELECTROSTATIC DISCHARGE

## DESCRIPTION

The M-65888 and M-65889 are high-performance BiCMOS static RaMs organized as 16,384 x 4 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The 65889 has an active LOW output enable ( $\overline{OE}$ ) feature. Both devices have an automatic power-down feature, reducing the power consumption by 67 % when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the four input/output pins ( $I/O_0$  through

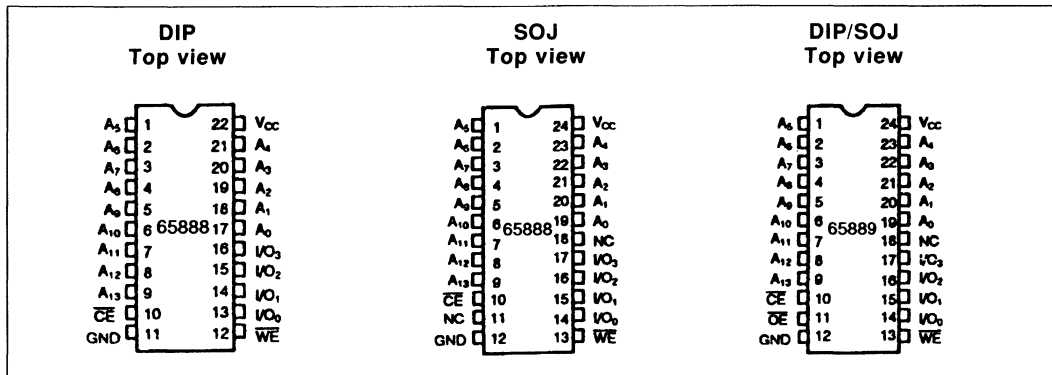
$I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking chip enable (CE) LOW (and OE LOW for M-65889 while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

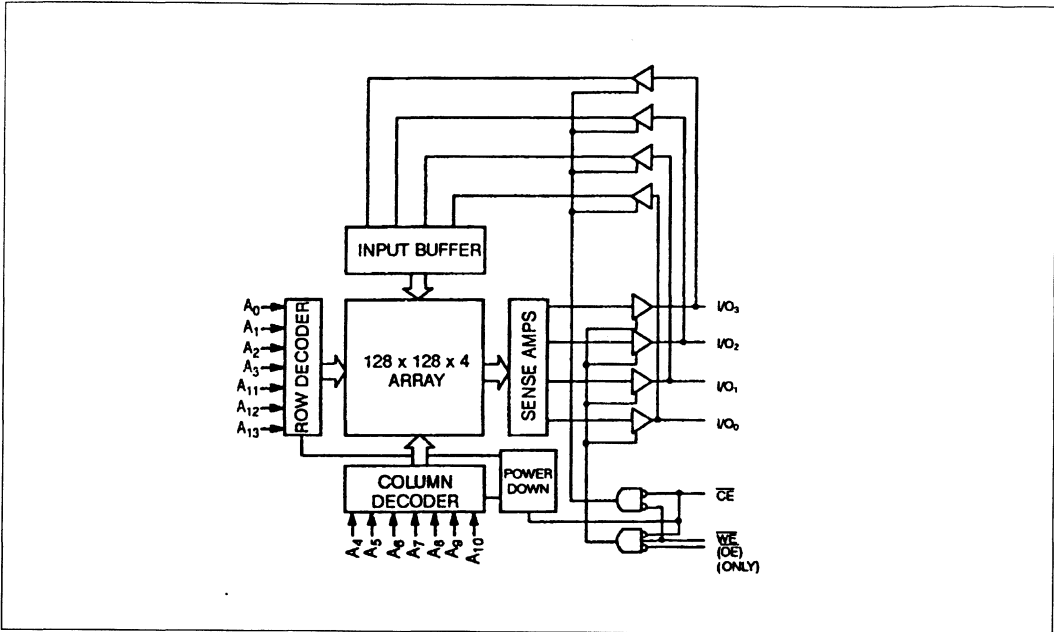
The I/O pins stay in high-impedance state when chip enable (CE) is HIGH, or write enable (WE) is LOW (or output enable ( $\overline{OE}$ ) is HIGH for M-65889.

5

## PACKAGES



BLOCK DIAGRAM



SELECTION GUIDE

|                                |            | M-65888-10<br>M-65889-10 | M-65888-12<br>M-65889-12 | M-65888-15<br>M-65889-15 |
|--------------------------------|------------|--------------------------|--------------------------|--------------------------|
| Maximum Access Time (ns)       |            | 10                       | 12                       | 15                       |
| Maximum Operating Current (mA) | Commercial | 130                      | 120                      |                          |
|                                | Military   |                          |                          | 135                      |
| Maximum Standby Current (mA)   | Commercial | 40                       | 40                       |                          |
|                                | Military   |                          |                          | 50                       |

**MAXIMUM RATINGS**

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested)

Storage Temperature . . . . .  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Ambient Temperature with  
 Power Applied . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Supply Voltage to  
 Ground Potential . . . . .  $-0.5\text{ V}$  to  $+7.0\text{ V}$   
 DC Voltage Applied to Outputs  
 in High Z State . . . . .  $-0.5\text{ V}$  to  $+7.0\text{ V}$

DC Input Voltage<sup>[1]</sup> . . . . .  $-3.0\text{ V}$  to  $+7.0\text{ V}$   
 Output Current into Outputs (Low) . . . . .  $20\text{ mA}$   
 Static Discharge Voltage . . . . .  $> 2001\text{ V}$   
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current . . . . .  $> 200\text{ mA}$

**OPERATING RANGE**

| RANGE                   | AMBIENT TEMPERATURE                             | V <sub>CC</sub>       |
|-------------------------|-------------------------------------------------|-----------------------|
| Commercial              | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    | $5\text{ V} \pm 10\%$ |
| Military <sup>[2]</sup> | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | $5\text{ V} \pm 10\%$ |

**ELECTRICAL CHARACTERISTICS** Over the Operating Range

| PARAMETERS      | DESCRIPTION                                       | TEST<br>CONDITIONS                                                |                               |       | M-65888-10 | M-65888-12      | M-65888-15 | UNITS           |       |                 |      |
|-----------------|---------------------------------------------------|-------------------------------------------------------------------|-------------------------------|-------|------------|-----------------|------------|-----------------|-------|-----------------|------|
|                 |                                                   |                                                                   |                               |       | M-65889-10 | M-65889-12      | M-65889-15 |                 |       |                 |      |
|                 |                                                   |                                                                   |                               |       | MIN.       | MAX.            | MIN.       |                 |       |                 | MAX. |
| V <sub>OH</sub> | Output HIGH<br>Voltage                            | V <sub>CC</sub> = Min.,                                           | I <sub>OH</sub> =<br>– 4.0 mA | Com'l | 2.4        |                 | 2.4        |                 | 2.4   |                 | V    |
|                 |                                                   |                                                                   | I <sub>OH</sub> =<br>– 2.0 mA | Mil   |            |                 |            |                 |       |                 |      |
| V <sub>OL</sub> | Output LOW<br>Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 MA                  |                               |       |            | 0.4             |            | 0.4             |       | 0.4             | V    |
| V <sub>IH</sub> | Input HIGH<br>Voltage                             |                                                                   |                               |       | 2.2        | V <sub>CC</sub> | 2.2        | V <sub>CC</sub> | 2.2   | V <sub>CC</sub> | V    |
| V <sub>IL</sub> | Input LOW<br>Voltage [1]                          |                                                                   |                               |       | – 0.5      | 0.8             | – 0.5      | 0.8             | – 0.5 | 0.8             | V    |
| I <sub>Ix</sub> | Input Load<br>Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                            |                               |       | – 10       | + 10            | – 10       | + 10            | – 10  | + 10            | μA   |
| I <sub>OZ</sub> | Output<br>Leakage<br>Current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled       |                               |       | – 10       | +10             | – 10       | +10             | – 10  | +10             | μA   |
| I <sub>CC</sub> | V <sub>CC</sub><br>Operating<br>Supply<br>Current | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA,<br>f = f max. |                               | Com'l |            | 130             |            | 120             |       |                 | mA   |
|                 |                                                   |                                                                   |                               | Mil   |            |                 |            |                 |       | 135             |      |
| I <sub>SB</sub> | CE<br>Power-Down<br>Current                       | CE ≥ V <sub>IH</sub>                                              |                               | Com'l |            | 40              |            | 40              |       |                 | mA   |
|                 |                                                   |                                                                   |                               | Mil   |            |                 |            |                 |       | 50              |      |

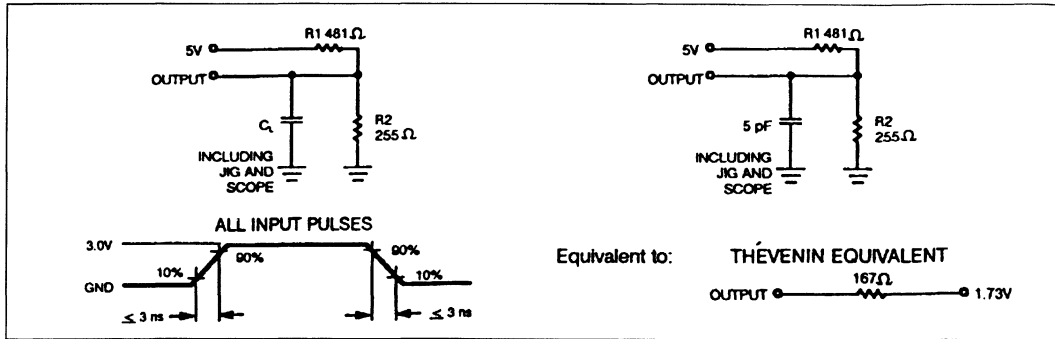
5

**CAPACITANCE** <sup>[3]</sup>

| PARAMETERS       | DESCRIPTION        | TEST CONDITIONS                                                                                  | MAX. <sup>[4]</sup> | UNITS |
|------------------|--------------------|--------------------------------------------------------------------------------------------------|---------------------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = $25^{\circ}\text{C}$ , f = $1\text{ MHz}$ ,<br>V <sub>CC</sub> = $5.0\text{ V}$ | 5                   | pF    |
| C <sub>OUT</sub> | Output Capacitance |                                                                                                  | 7                   | pF    |

- Notes :** 1. V<sub>IL</sub> (min) =  $3.0\text{ V}$  for pulse width  $< 20\text{ ns}$ .  
 2. T<sub>A</sub> is the "instant on" case temperature.  
 3. Tested initially and after any design or process changes that may affect these parameters.  
 4. For all packages except Cerdip, which has maximum of C<sub>IN</sub> =  $8\text{ pF}$ , C<sub>OUT</sub> =  $9\text{ pF}$ .

## AC TEST LOADS AND WAVEFORMS

SWITCHING CHARACTERISTICS Over the Operating Range <sup>[5]</sup>

| PARAMETERS                 | DESCRIPTION                                      | M-65888-10<br>M-65889-10 |      | M-65888-12<br>M-65889-12 |      | M-65888-15<br>M-65889-15 |      | UNITS |
|----------------------------|--------------------------------------------------|--------------------------|------|--------------------------|------|--------------------------|------|-------|
|                            |                                                  | MIN.                     | MAX. | MIN.                     | MAX. | MIN.                     | MAX. |       |
|                            |                                                  | READ CYCLE               |      |                          |      |                          |      |       |
| t <sub>RC</sub>            | Read Cycle Time                                  | 10                       |      | 12                       |      | 15                       |      | ns    |
| t <sub>AA</sub>            | Address to Data Valid                            |                          | 10   |                          | 12   |                          | 15   | ns    |
| t <sub>OHA</sub>           | Output Hold from Address Change                  | 2                        |      | 3                        |      | 3                        |      | ns    |
| t <sub>ACE</sub>           | $\overline{CE}$ LOW to Data Valid                |                          | 10   |                          | 12   |                          | 15   | ns    |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                | 65889                    | 7    |                          | 7    |                          | 10   | ns    |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z                     | 65889                    | 2    | 2                        |      | 3                        |      | ns    |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>    | 65889                    | 7    |                          | 7    |                          | 8    | ns    |
| t <sub>LZCE</sub>          | $\overline{CE}$ LOW to Low Z <sup>[5]</sup>      | 2                        |      | 3                        |      | 3                        |      | ns    |
| t <sub>HZCE</sub>          | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup> |                          | 7    |                          | 7    |                          | 8    | ns    |
| WRITE CYCLE <sup>[8]</sup> |                                                  |                          |      |                          |      |                          |      |       |
| t <sub>WC</sub>            | Write cycle Time                                 | 10                       |      | 12                       |      | 15                       |      | ns    |
| t <sub>SCE</sub>           | $\overline{CE}$ LOW TO write End                 | 8                        |      | 8                        |      | 10                       |      | ns    |
| t <sub>AW</sub>            | Address Set-up to Write End                      | 8                        |      | 8                        |      | 10                       |      | ns    |
| t <sub>HA</sub>            | Address Hold from Write End                      | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>SA</sub>            | Address Set-Up to Write Start                    | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                      | 8                        |      | 8                        |      | 10                       |      | ns    |
| t <sub>SD</sub>            | Data Set-Up to Write End                         | 6                        |      | 6.5                      |      | 8                        |      | ns    |
| t <sub>HD</sub>            | Data Hold from Write End                         | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z                    | 3                        |      | 3                        |      | 3                        |      | ns    |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[6]</sup>     | 0                        | 7    | 0                        | 7    | 0                        | 7    | ns    |

**Notes :** 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$ , and  $C_L = 20$  pF.

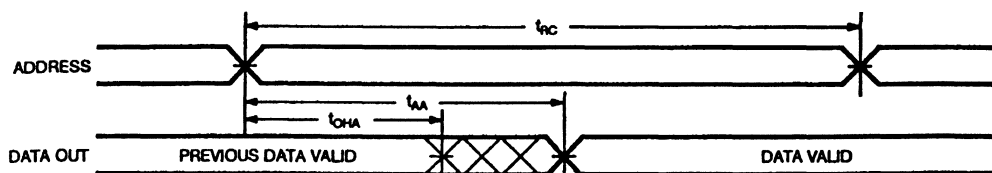
6.  $t_{HZCE}$ ,  $t_{HZWE}$ , and  $t_{HZOE}$  are specified with  $C_L = 5$  pF as in part (b) in AC Test Loads. Transition is measured  $\pm 200$  mV from steady state voltage.

7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device, these parameters are guaranteed and not 100 % tested.

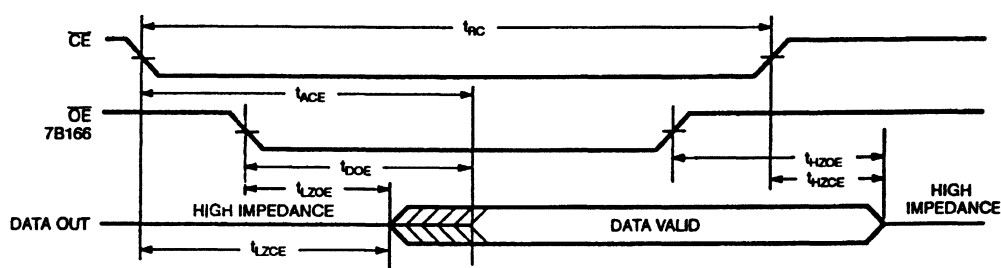
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## SWITCHING WAVEFORMS

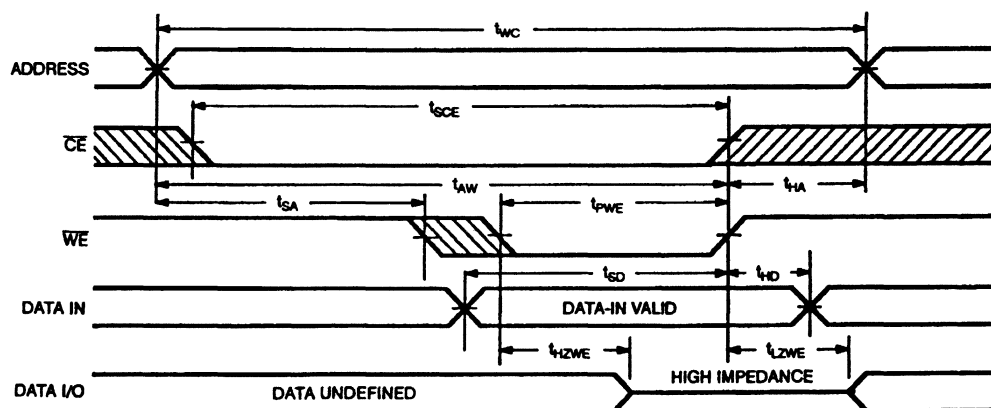
## READ CYCLE N° 1 (9, 10)



## READ CYCLE N° 2 (9, 11)



## WRITE CYCLE N° 1 (WE Controlled) (9, 12)



Notes : 9.  $\overline{WE}$  is HIGH for read cycle.

10. Device is continuously selected,  $\overline{CE} = V_{IL}$ . (65889  $\overline{OE} = V_{IL}$  also).

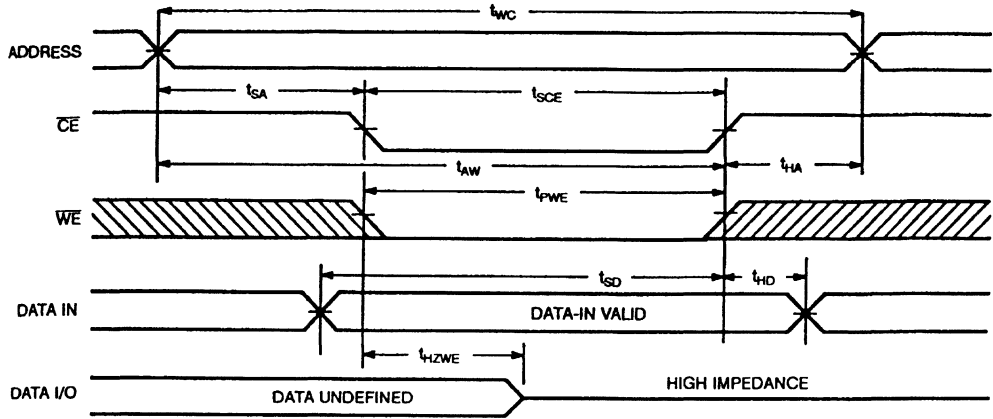
11. Address valid prior to or coincident with  $\overline{CE}$  transition low.

12. 65889 only : Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remain in a high-impedance state.

SWITCHING WAVEFORMS (continued)

WRITE CYCLE N° 2 ( $\overline{CE}$  controlled) (8, 12, 13)



65888 TRUTH TABLE

| CE | WE | INPUTS/OUTPUT | MODE                    |
|----|----|---------------|-------------------------|
| H  | X  | High Z        | Deselect/<br>Power-Down |
| L  | H  | Data Out      | Read                    |
| L  | L  | Data In       | Write                   |

65889 TRUTH TABLE

| CE | WE | OE | INPUTS/OUTPUT | MODE                    |
|----|----|----|---------------|-------------------------|
| H  | X  | X  | High Z        | Deselect/<br>Power-Down |
| L  | H  | L  | Data Out      | Read                    |
| L  | L  | X  | Data In       | Write                   |
| L  | H  | H  | High Z        | Deselect                |

ORDERING INFORMATION

|                                |     |                                                             |             |                                                 |
|--------------------------------|-----|-------------------------------------------------------------|-------------|-------------------------------------------------|
|                                | M   | 1                                                           | 65888       | 10                                              |
|                                |     |                                                             |             |                                                 |
| C : Commercial<br>M : Military | MHS | 0 : chip form<br>1 : ceramic<br>3 : Plastic Dill<br>U : SOJ | Device Type | Speed<br>10 : 10 ns<br>12 : 12 ns<br>15 : 15 ns |

# ECL SRAM









DATA SHEET

M10E422/M100E422

256 x 4 ECL  
STATIC RAM

FEATURES

- 256 X 4 BITS ORGANIZATION
- ULTRA HIGH SPEED/STANDARD POWER
  - $t_{AA} = 3\text{ ns}$ ,  $t_{ABS} = 2\text{ ns}$
  - $I_{EE} = 220\text{ mA}$
- LOW POWER VERSION
  - $t_{AA} = 5\text{ ns}$
  - $I_{EE} = 150\text{ mA}$
- BOTH 10 KH/10 K AND 100 K COMPATIBLE I/O VERSIONS
- ON CHIP VOLTAGE COMPENSATION FOR IMPROVED NOISE MARGIN
- OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION
- INDUSTRY STANDARD PINOUT

6

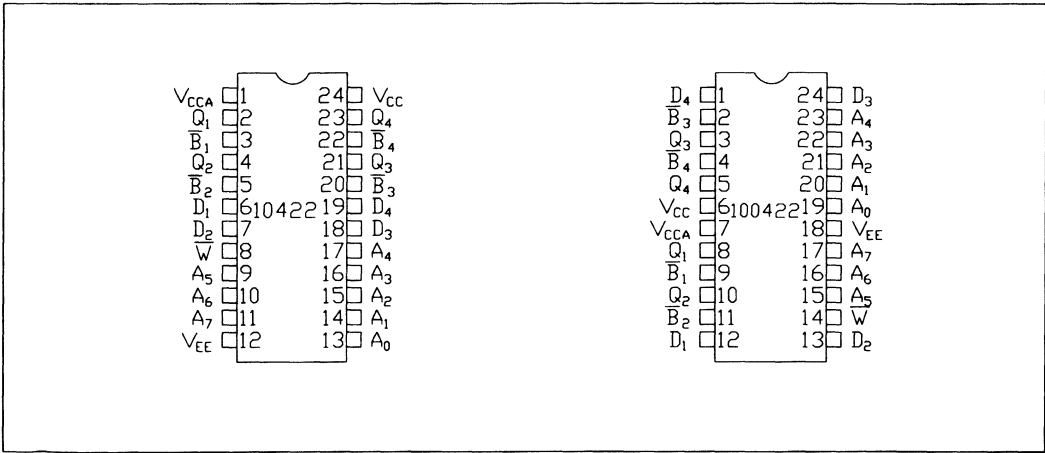
DESCRIPTION

The MHS M10E422 and M100E422 are 256 x 4 ECL RAMs designed for scratch pad, control and Buffer Storage applications. These RAMs are developed by Aspen Semiconductor Corporation. Both parts are fully decoded random access memories organized as 256 words by 4 bits. The M110E422 is 10 KH/10 K compatible. The M100E422 is 100 K compatible.

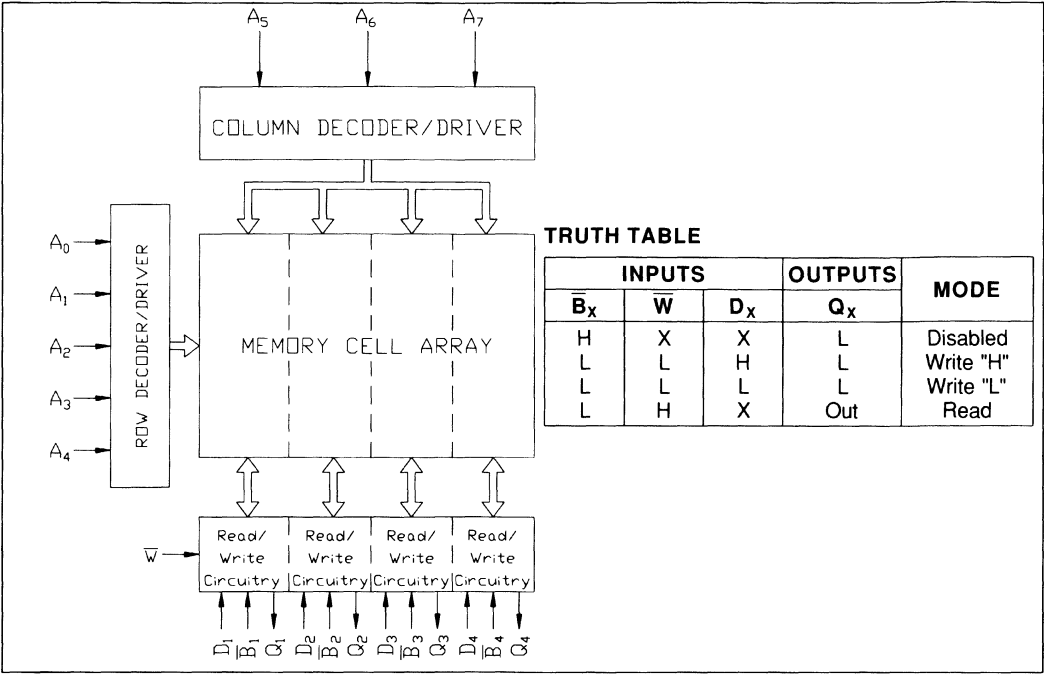
The four independent active LOW block select ( $\overline{B}$ ) inputs control memory selection and allow for memory ex-

pansion and reconfiguration. The read and write operations are controlled by the state of the active LOW write enable (W) input. With W and  $\overline{B}_x$  LOW, the corresponding data at  $D_x$  is written into the addressed location. To read, W is held HIGH, while B is held LOW. Open emitter outputs allow for wired-OR connection to expand or reconfigure the memory.

PIN CONFIGURATIONS



LOGIC BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

| PARAMETERS | DESCRIPTION                                  | TEST CONDITIONS                                                                                                   | TEMPERATURE <sup>(1)</sup>        | MIN.  | MAX.  | UNIT    |
|------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------------------------|-------|-------|---------|
| $V_{OH}$   | Output HIGH Voltage                          | 10E <sup>(2)</sup> $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -5.2\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$                 | -1000 | -840  | mV      |
|            |                                              |                                                                                                                   | $T_A = +25^\circ C$               | -960  | -810  | mV      |
|            |                                              |                                                                                                                   | $T_A = +75^\circ C$               | -900  | -735  | mV      |
|            |                                              | 100K $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -4.5\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to $85^\circ C$ | -1025 | -880  | mV      |
| $V_{OL}$   | Output LOW Voltage                           | 10E $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -5.2\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.                | $T_A = 0^\circ C$                 | -1870 | -1665 | mV      |
|            |                                              |                                                                                                                   | $T_A = +25^\circ C$               | -1850 | -1650 | mV      |
|            |                                              |                                                                                                                   | $T_A = +75^\circ C$               | -1830 | -1625 | mV      |
|            |                                              | 100K $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -4.5\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1620 | mV      |
| $V_{IH}$   | Input HIGH Voltage                           | 10E<br>$V_{EE} = -5.2\ V$                                                                                         | $T_A = 0^\circ C$                 | -1170 | -840  | mV      |
|            |                                              |                                                                                                                   | $T_A = +25^\circ C$               | -1130 | -810  | mV      |
|            |                                              |                                                                                                                   | $T_A = +75^\circ C$               | -1070 | -720  | mV      |
|            |                                              | 100K $V_{EE} = -4.5\ V$                                                                                           | $T_A = 0^\circ C$ to $85^\circ C$ | -1165 | -880  | mV      |
| $V_{IL}$   | Input LOW Voltage                            | 10E<br>$V_{EE} = -5.2\ V$                                                                                         | $T_A = 0^\circ C$                 | -1950 | -1480 | mV      |
|            |                                              |                                                                                                                   | $T_A = +25^\circ C$               | -1950 | -1480 | mV      |
|            |                                              |                                                                                                                   | $T_A = +75^\circ C$               | -1950 | -1450 | mV      |
|            |                                              | 100K $V_{EE} = -4.5\ V$                                                                                           | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1475 | mV      |
| $I_{IH}$   | Input HIGH Current                           | $V_{IN} = V_{IH}$ Max.                                                                                            |                                   |       | 220   | $\mu A$ |
| $I_{iL}$   | Input LOW Current                            | $V_{IN} = V_{iL}$ Min.                                                                                            | $\bar{B}$ inputs                  | 0.5   | 170   | $\mu A$ |
|            |                                              |                                                                                                                   | All other inputs                  | -50   |       | $\mu A$ |
| $I_{EE}$   | Supply Current (All inputs and outputs open) | Commercial "L" (Low Power)                                                                                        |                                   |       | -150  | mA      |
|            |                                              | Commercial Standard                                                                                               |                                   |       | -220  | mA      |

Notes : 1. Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.  
2. 10E specifications support both 10 K and 10 KH compatibility.

CAPACITANCE <sup>(3)</sup>

| PARAMETERS | DESCRIPTION        | MIN. | TYP. | MAX. | UNIT |
|------------|--------------------|------|------|------|------|
| $C_{IN}$   | Input Capacitance  |      | 4    | 10   | pF   |
| $C_{OUT}$  | Output Capacitance |      | 6    | 12   | pF   |

Notes : 3. Tested initially and after any design or process changes that may affect these parameters.

# AC TEST LOADS AND WAVEFORMS (5, 6, 7, 8, 9, 10)

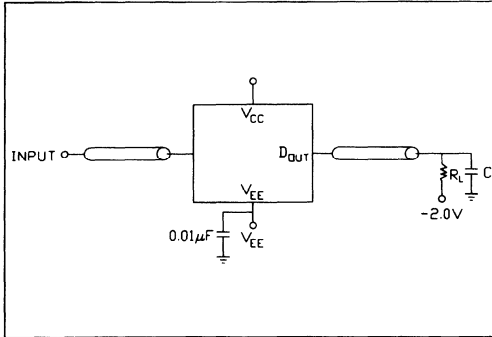


Figure 1.

- Notes :**
5.  $V_{IL} = V_{IL} \text{ Min.}$ ,  $V_{IH} = V_{IH} \text{ Max.}$  on 10E version.
  6.  $V_{IL} = -1.7 \text{ V}$ ,  $V_{IH} = -0.9 \text{ V}$  on 100 K version.
  7.  $R_L = 50 \Omega$ ,  $C < 5 \text{ pF}$  (3 ns grade) or  $< 30 \text{ pF}$  (5, 7 ns grade) (includes fixture and stray capacitance).

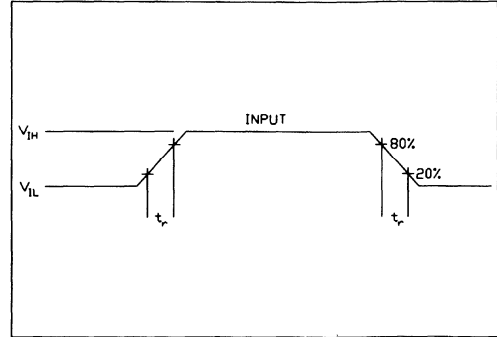


Figure 2.

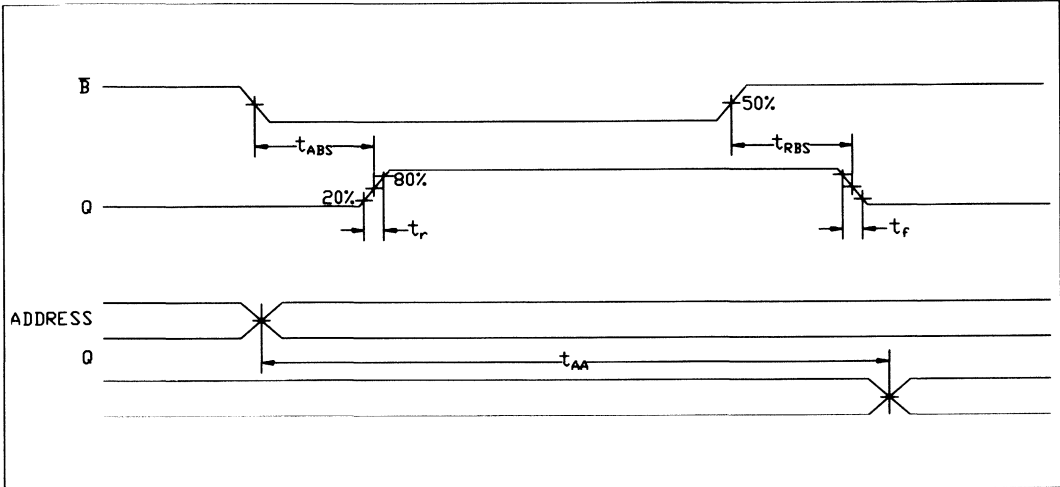
- Notes :**
8. All coaxial cables should be 50  $\Omega$  with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
  9.  $t_r = t_f = 0.7 \text{ ns}$ .
  10. All timing measurements are made from the 50 % point of all waveforms.

## 6

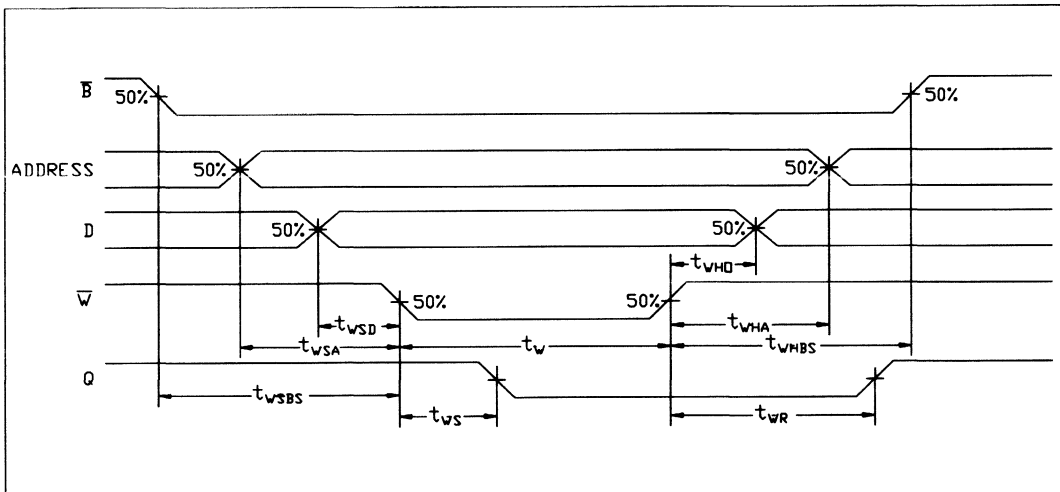
### SWITCHING CHARACTERISTICS Over Operating Range

| PARAMETERS | DESCRIPTION                  | 10E422-3<br>100E422-3 |      | 10E422-5<br>100E422-5 |      | 10E422-7<br>100E422-7 |      | UNIT |
|------------|------------------------------|-----------------------|------|-----------------------|------|-----------------------|------|------|
|            |                              | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |      |
| $t_{ABS}$  | Block Select to Output Delay |                       | 2.0  |                       | 3.0  |                       | 4.0  | ns   |
| $t_{RBS}$  | Block Select Recovery        |                       | 2.0  |                       | 3.0  |                       | 4.0  | ns   |
| $t_{AA}$   | Address Access Time          |                       | 3.0  |                       | 5.0  |                       | 7.0  | ns   |
| $t_W$      | Write Pulse Width            | 3.0                   |      | 3.0                   |      | 5.0                   |      | ns   |
| $t_{WSD}$  | Data Setup to Write          | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WHD}$  | Data Hold to Write           | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WSA}$  | Address Setup/Write          | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WHA}$  | Address Hold/Write           | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WSBS}$ | Block Select Setup/Write     | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WHBS}$ | Block Select Hold/Write      | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns   |
| $t_{WS}$   | Write Disable                |                       | 2.0  |                       | 3.0  |                       | 4.0  | ns   |
| $t_{WR}$   | Write Recovery               |                       | 3.5  |                       | 6.0  |                       | 8.0  | ns   |
| $t_r$      | Output Rise Time             | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns   |
| $t_f$      | Output Fall Time             | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns   |

SWITCHING WAVEFORMS

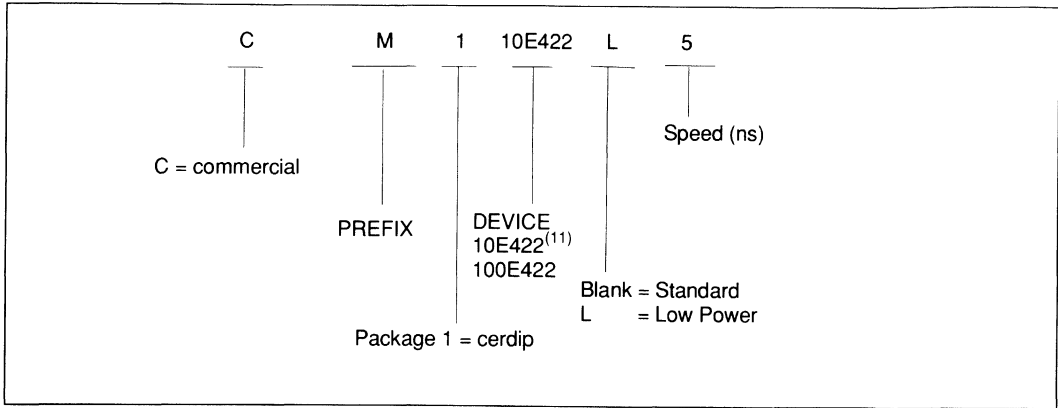


Read Mode



Write Mode

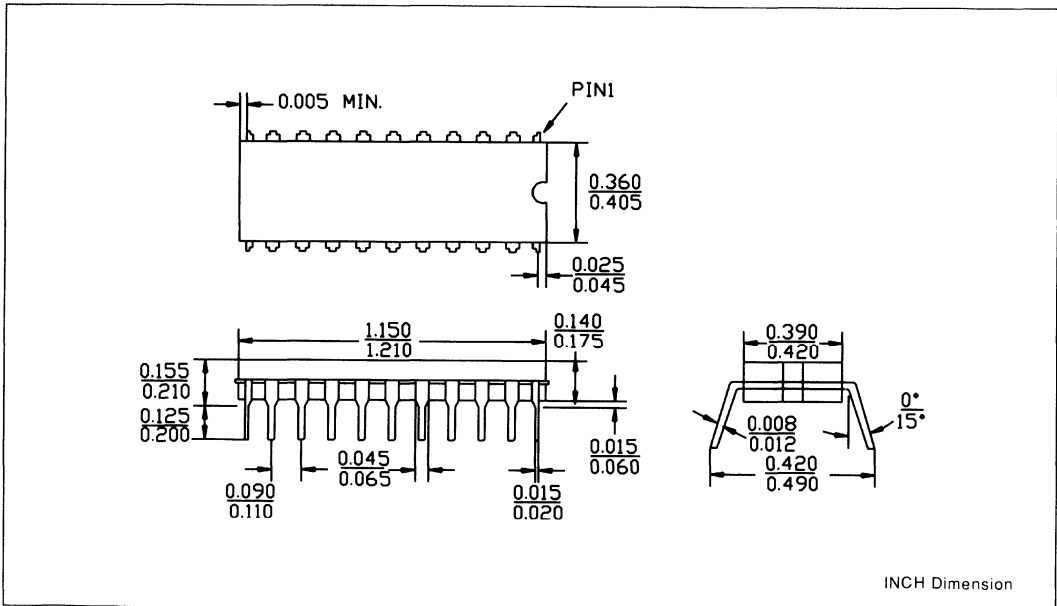
## ORDERING INFORMATION



Note : 11. 10E specifications support both 10 K and 10 KH compatibility.

## PACKAGE DIAGRAMS

### 24 LEAD (400 MIL) CERDIP





DATA SHEET

M10E474/M100E474

1024 x 4 ECL  
STATIC RAM

FEATURES

- 1024 x 4 BITS ORGANIZATION
- ULTRA HIGH SPEED/STANDARD POWER
  - $t_{AA} = 3\text{ ns}$ ,  $t_{ACS} = 2\text{ ns}$
  - $I_{EE} = 275\text{ mA}$
- LOW POWER VERSION
  - $t_{AA} = 5\text{ ns}$
  - $I_{EE} = 190\text{ mA}$
- BOTH 10 KH/10 K AND 100 K COMPATIBLE I/O VERSIONS
- ON CHIP VOLTAGE COMPENSATION FOR IMPROVED NOISE MARGIN
- OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION
- INDUSTRY STANDARD PINOUT

6

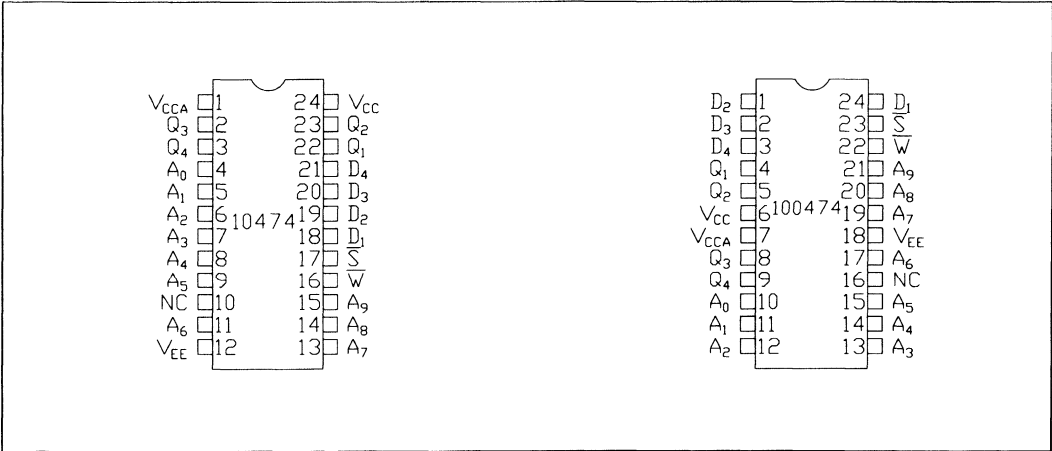
DESCRIPTION

The MHS M10E474 and M100E474 are 1 K x 4 ECL RAMs designed for scratch pad, control and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation. Both parts are fully decoded random access memories organized as 1024 words by 4 bits. The M10E474 is 10 KH/10 K compatible. The M100E474 is 100 K compatible.

The active LOW chip select ( $\bar{S}$ ) input controls memory selection and allows for memory expansion. The read

and write operations are controlled by the state of the active LOW write enable ( $\bar{W}$ ) input. With  $\bar{W}$  and  $\bar{S}$  LOW, the data at  $\bar{D}(1-4)$  is written into the addressed location. To read  $\bar{W}$  is held HIGH, while  $\bar{S}$  is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

PIN CONFIGURATIONS



**6-10**



|                           |            | <b>10E474-3</b><br><b>100E474-3</b> | <b>10E474-5</b><br><b>100E474-5</b> | <b>10E474-7</b><br><b>100E474-7</b> |
|---------------------------|------------|-------------------------------------|-------------------------------------|-------------------------------------|
| Maximum Access Time (ns)  |            | 3                                   | 5                                   | 7                                   |
| I <sub>EE</sub> Max. (mA) | Commercial | – 275                               | – 275                               |                                     |
|                           | "L"        |                                     | – 190                               | – 190                               |

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Ambient Temperature with

Power Applied ..... - 55°C to + 125°C

Supply Voltage  $V_{EE}$  to  $V_{CC}$  ..... - 7.0 to + 0.5 V

Input Voltage ..... VEE to + 0.5 V

Output Current..... - 50 mA

**OPERATING RANGE** referenced to  $V_{CC}$

| RANGE                      | I/O          | AMBIENT TEMPERATURE | V <sub>EE</sub>    |
|----------------------------|--------------|---------------------|--------------------|
| Commercial (Standard, "L") | 10KH/<br>10K | 0°C to 75°C         | - 5.2 V<br>± 5 %   |
| Commercial (Standard, "L") | 100K         | 0°C to 85°C         | - 4.5 V<br>± 0.3 V |



## ELECTRICAL CHARACTERISTICS

| PARAMETERS | DESCRIPTION                                     | TEST CONDITIONS                                                                                                   | TEMPERATURE <sup>(1)</sup>        | MIN.  | MAX.  | UNIT    |
|------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------------------------|-------|-------|---------|
| $V_{OH}$   | Output HIGH Voltage                             | 10E <sup>(2)</sup> $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -5.2\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$                 | -1000 | -840  | mV      |
|            |                                                 |                                                                                                                   | $T_A = +25^\circ C$               | -960  | -810  | mV      |
|            |                                                 |                                                                                                                   | $T_A = +75^\circ C$               | -900  | -735  | mV      |
|            |                                                 | 100K $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -4.5\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to $85^\circ C$ | -1025 | -880  | mV      |
| $V_{OL}$   | Output LOW Voltage                              | 10E $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -5.2\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.                | $T_A = 0^\circ C$                 | -1870 | -1665 | mV      |
|            |                                                 |                                                                                                                   | $T_A = +25^\circ C$               | -1850 | -1650 | mV      |
|            |                                                 |                                                                                                                   | $T_A = +75^\circ C$               | -1830 | -1625 | mV      |
|            |                                                 | 100K $R_L = 50\ \Omega$ to $-2\ V$<br>$V_{EE} = -4.5\ V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1620 | mV      |
| $V_{IH}$   | Input HIGH Voltage                              | 10E<br>$V_{EE} = -5.2\ V$                                                                                         | $T_A = 0^\circ C$                 | -1170 | -840  | mV      |
|            |                                                 |                                                                                                                   | $T_A = +25^\circ C$               | -1130 | -810  | mV      |
|            |                                                 |                                                                                                                   | $T_A = +75^\circ C$               | -1070 | -720  | mV      |
|            |                                                 | 100K $V_{EE} = -4.5\ V$                                                                                           | $T_A = 0^\circ C$ to $85^\circ C$ | -1165 | -880  | mV      |
| $V_{IL}$   | Input LOW Voltage                               | 10E<br>$V_{EE} = -5.2\ V$                                                                                         | $T_A = 0^\circ C$                 | -1950 | -1480 | mV      |
|            |                                                 |                                                                                                                   | $T_A = +25^\circ C$               | -1950 | -1475 | mV      |
|            |                                                 |                                                                                                                   | $T_A = +75^\circ C$               | -1950 | -1450 | mV      |
|            |                                                 | 100K $V_{EE} = -4.5\ V$                                                                                           | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1475 | mV      |
| $I_{IH}$   | Input HIGH Current                              | $V_{IN} = V_{IH}$ Max.                                                                                            |                                   |       | 220   | $\mu A$ |
| $I_{iL}$   | Input LOW Current                               | $V_{IN} = V_{iL}$ Min.                                                                                            | $\bar{S}$ inputs                  | 0.5   | 170   | $\mu A$ |
|            |                                                 |                                                                                                                   | All other inputs                  | -50   |       | $\mu A$ |
| $I_{EE}$   | Supply Current<br>(All inputs and outputs open) | Commercial "L" (Low Power)                                                                                        |                                   | -190  |       | mA      |
|            |                                                 | Commercial Standard                                                                                               |                                   | -275  |       | mA      |

Notes : 1. Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.  
2. 10E specifications support both 10 K and 10 KH compatibility.

CAPACITANCE <sup>(3)</sup>

| PARAMETERS | DESCRIPTION            | MIN. | TYP. | MAX. | UNIT |
|------------|------------------------|------|------|------|------|
| $C_{IN}$   | Input Pin Capacitance  |      | 4    | 10   | pF   |
| $C_{OUT}$  | Output Pin Capacitance |      | 6    | 12   | pF   |

Notes : 3. Tested initially and after any design or process changes that may affect these parameters.

AC TEST LOADS AND WAVEFORMS (5, 6, 7, 8, 9, 10)

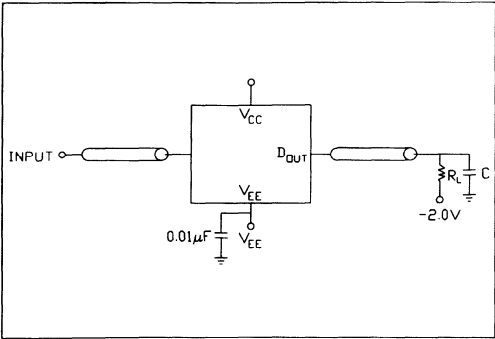


Figure 1.

Notes : 5.  $V_{IL} = V_{IL} \text{ Min.}$ ,  $V_{IH} = V_{IH} \text{ Max.}$  on 10E version.  
6.  $V_{IL} = -1.7 \text{ V}$ ,  $V_{IH} = -0.9 \text{ V}$  on 100 K version.  
7.  $R_L = 50 \Omega$ ,  $C < 5 \text{ pF}$  (3 ns grade) or  $< 30 \text{ pF}$  (5, 7 ns grade) (includes fixture and stray capacitance).

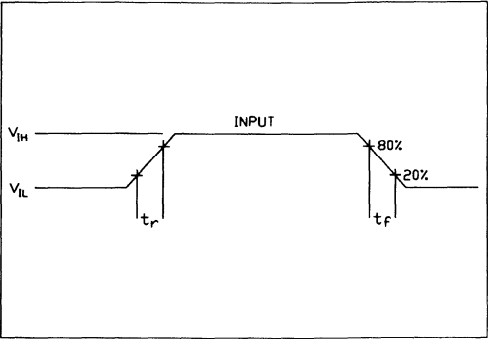


Figure 2.

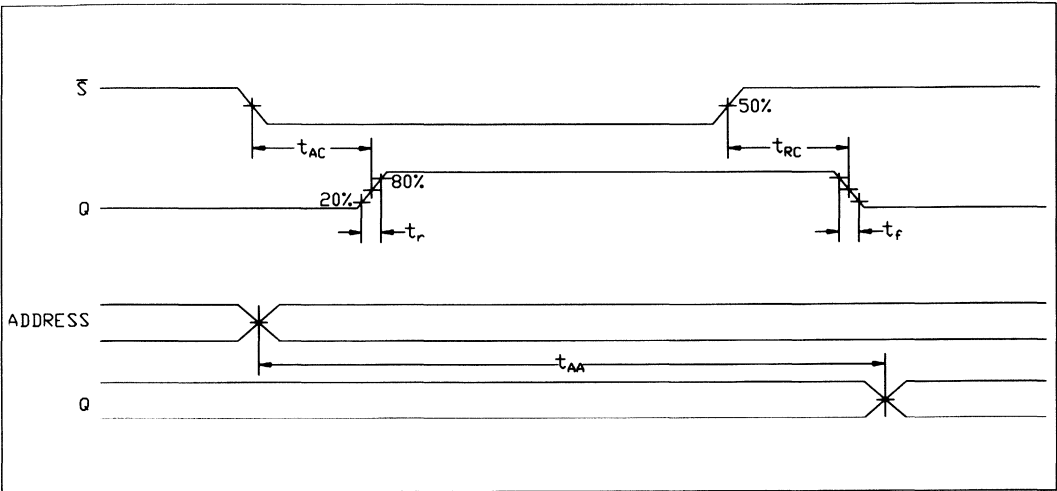
Notes : 8. All coaxial cables should be  $50 \Omega$  with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.  
9.  $t_r = t_f = 0.7 \text{ ns}$ .  
10. All timing measurements are made from the 50 % point of all

6

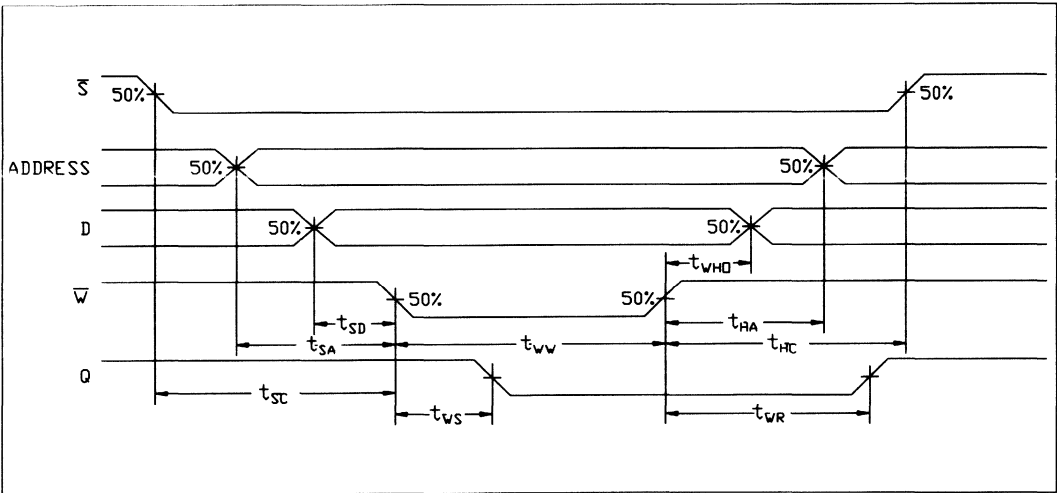
SWITCHING CHARACTERISTICS Over Operating Range

| PARAMETERS | DESCRIPTION             | 10E474-3<br>100E474-3 |      | 10E474-5<br>100E474-5 |      | 10E474-7<br>100E474-7 |      | UNIT |
|------------|-------------------------|-----------------------|------|-----------------------|------|-----------------------|------|------|
|            |                         | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |      |
| $t_{AC}$   | Input to Output Delay   |                       | 2.0  | 0.5                   | 3.0  | 0.5                   | 5.0  | ns   |
| $t_{RC}$   | Chip Select Recovery    |                       | 2.0  | 0.5                   | 3.0  | 0.5                   | 5.0  | ns   |
| $t_{AA}$   | Address Access Time     |                       | 3.0  | 1.2                   | 5.0  | 1.2                   | 7.0  | ns   |
| $t_W$      | Write Pulse Width       | 3.0                   |      | 5.0                   |      | 5.0                   |      | ns   |
| $t_{SD}$   | Data Setup to Write     | 0.5                   |      | 0.0                   |      | 0.0                   |      | ns   |
| $t_{HD}$   | Data Hold to Write      | 0.5                   |      | 0.0                   |      | 1.0                   |      | ns   |
| $t_{SA}$   | Address Setup/Write     | 0.5                   |      | 0.0                   |      | 1.0                   |      | ns   |
| $t_{HA}$   | Address Hold/Write      | 0.5                   |      | 0.0                   |      | 1.0                   |      | ns   |
| $t_{SC}$   | Chip Select Setup/Write | 0.5                   |      | 0.0                   |      | 0.0                   |      | ns   |
| $t_{HC}$   | Chip Select Hold/Write  | 0.5                   |      | 0.0                   |      | 1.0                   |      | ns   |
| $t_{WS}$   | Write Disable           |                       | 2.0  | 0.3                   | 3.0  | 0.3                   | 6.5  | ns   |
| $t_{WR}$   | Write Recovery          |                       | 3.5  | 0.5                   | 5.0  | 0.5                   | 7.0  | ns   |
| $t_r$      | Output Rise Time        | 0.35                  | 1.5  | 0.35                  | 2.5  | 1.0                   | 2.5  | ns   |
| $t_f$      | Output Fall Time        | 0.35                  | 1.5  | 0.35                  | 2.5  | 1.0                   | 2.5  | ns   |

SWITCHING WAVEFORMS



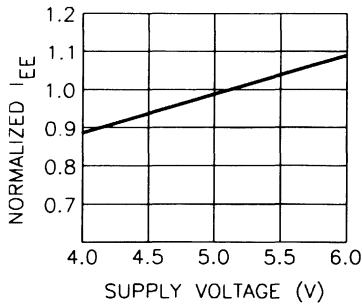
Read Mode



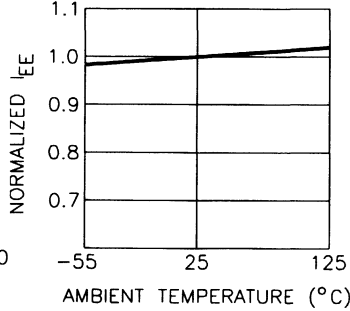
Write Mode

6

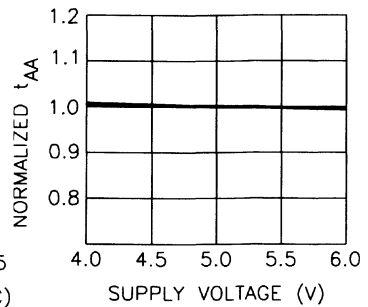
NORMALIZED SUPPLY VOLTAGE  
vs. SUPPLY CURRENT



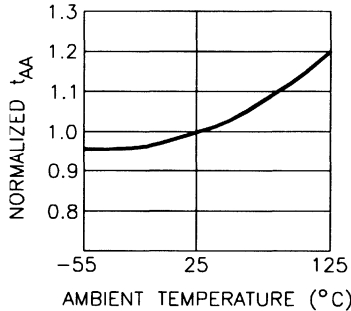
NORMALIZED SUPPLY CURRENT  
vs. AMBIENT TEMPERATURE



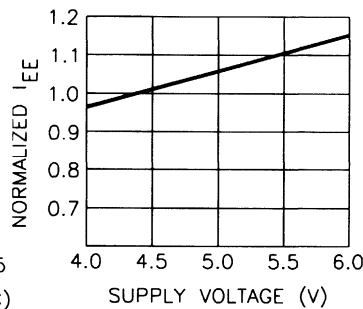
NORMALIZED ACCESS TIME  
vs. SUPPLY VOLTAGE



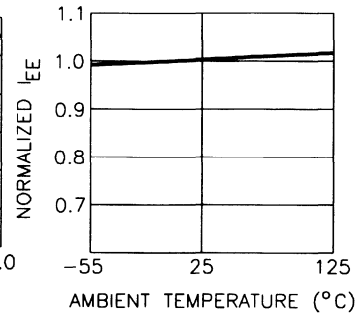
NORMALIZED ACCESS TIME  
vs. AMBIENT TEMPERATURE



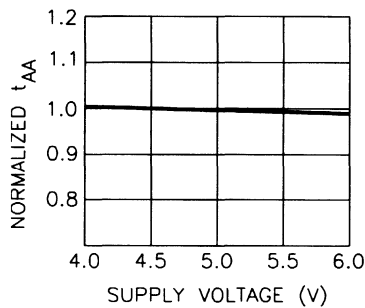
NORMALIZED SUPPLY CURRENT  
vs. SUPPLY VOLTAGE



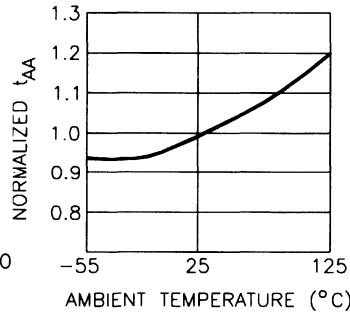
NORMALIZED SUPPLY CURRENT  
vs. AMBIENT TEMPERATURE



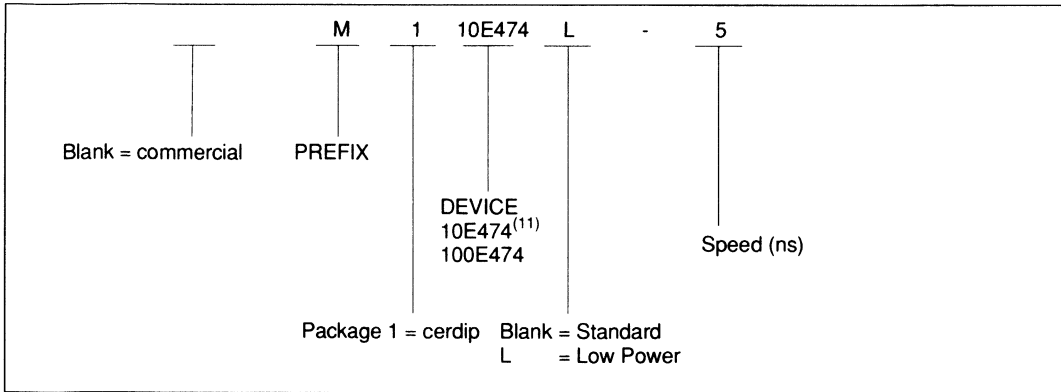
NORMALIZED ACCESS TIME  
vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME  
vs. AMBIENT TEMPERATURE



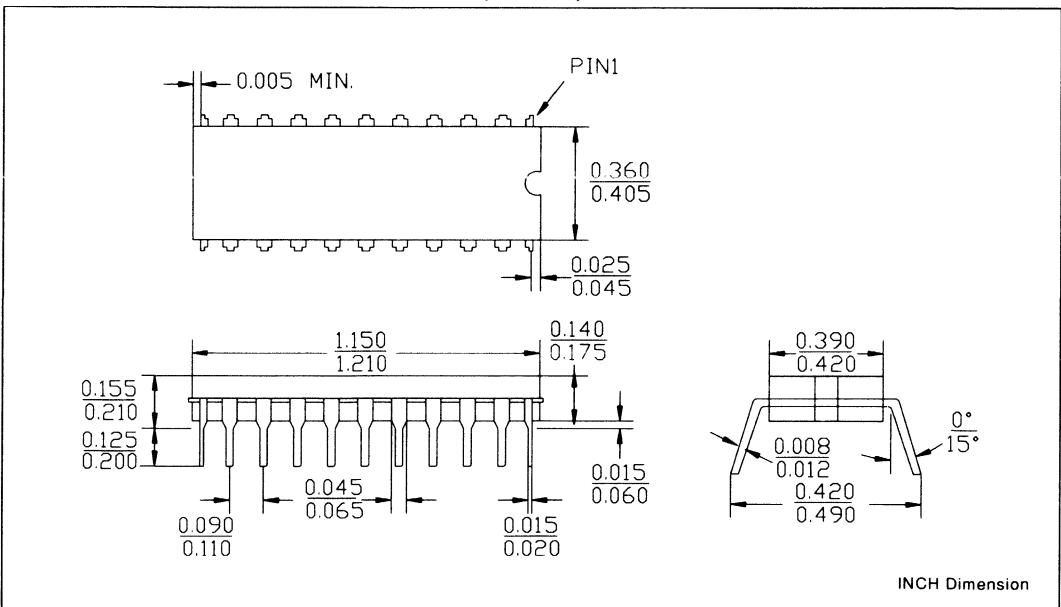
## ORDERING INFORMATION



**Note :** 11. 10E specifications support both 10 K and 10 KH compatibility.

## PACKAGE DIAGRAMS

### 24 LEAD (400 MIL) CERDIP



**6**



# CACHE RAM

7









September 1990

## DATA SHEET

# M 65783/M 65784

## 2 x 4096 x 16 CACHE RAM

### FEATURES

- PIN-PROGRAMMABLE INTO DIRECT-MAPPED OR TWO-WAY SET ASSOCIATIVE FORMAT
- CMOS FOR OPTIMUM SPEED/POWER
- HIGH SPEED
  - 25 ns
- COMMON I/O
- INTERNAL ADDRESS LATCH
- TTL COMPATIBLE INPUTS AND OUTPUTS
- CAPABLE OF WITHSTANDING GREATER THAN 2001 V ELECTROSTATIC DISCHARGE
- COMPATIBLE WITH INTEL 82385 CACHE CONTROLLER

### DESCRIPTION

The M-65783 and M-65784 are high-performance monolithic CMOS static RAMs that contain 128 kbits organized into either, two-way set associative blocks of 4 K x 16 RAM, or one directly mapped 8 K x 16-bit RAM.

They are designed specially for use with the intel 82385 Cache Controller, and their addresses are latched on the falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The M-65783 has all address bits latched by the ALE signal except A<sub>12</sub>, which is unlatched. A<sub>12</sub>, which bypasses the latch, has a faster access time. All address bits are latched by the ALE signal in the M-65784. The mode pin controls whether they are configured as direct-mapped 8 K x 16 or two-way set associative 2 x 4 K x 16 RAMs. When mode is HIGH, the circuits are placed in the two-way mode. In the two way mods, the upper address bit, A<sub>12</sub> is a "don't care", and is externally wired to ground. When mode is LOW, the circuits are placed in the direct mode.

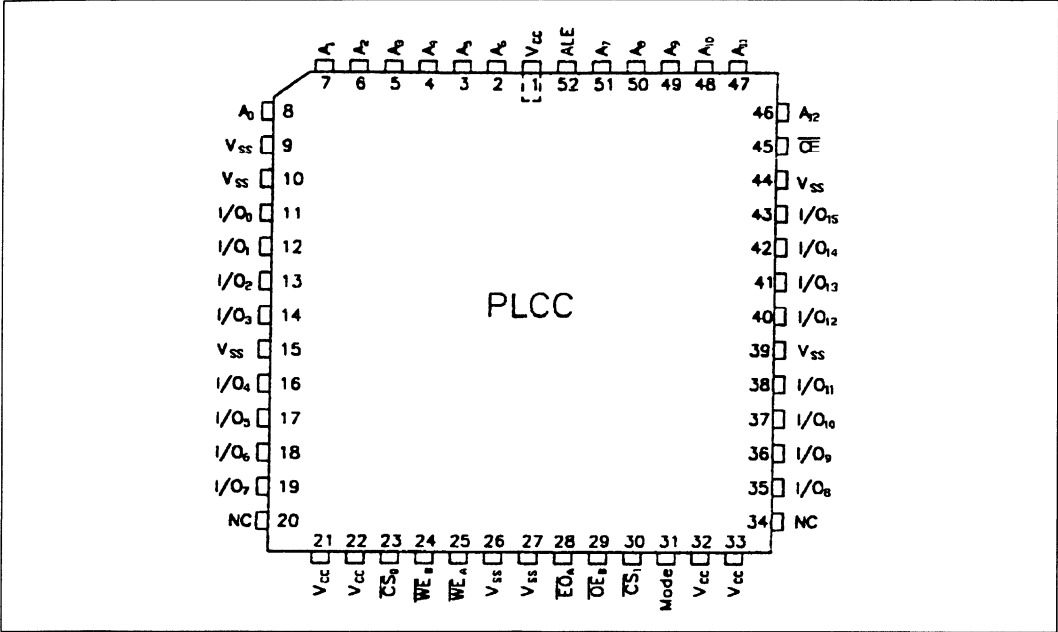
Writing is accomplished in the two-way mode by taking CE LOW and by inserting the respective CS<sub>x</sub> and WE<sub>x</sub> signals LOW. CS<sub>0</sub> enables bits D<sub>0</sub>-D<sub>7</sub> while CS<sub>1</sub> enables bits D<sub>8</sub>-D<sub>15</sub>. WE<sub>A</sub> enables cache bank A, and WE<sub>B</sub> enables cache bank B to receive whatever data resides on the data bus. OE<sub>A</sub> and OE<sub>B</sub> similarly enable cache banks A and B respectively, to drive the data bus.

Writing is accomplished, in the direct mode, by tying WE<sub>A</sub> and WE<sub>B</sub> together externally, and using A<sub>12</sub> to determine which 4 K x 16 memory bank is selected.

Reading is accomplished in the two-way mode by taking CE LOW, inserting the respective OEx and CS<sub>x</sub> signals LOW and the respective WE<sub>x</sub> signal HIGH. The contents of the memory location specified on the address pins will appear on the 16 outputs. Activation of OE<sub>A</sub> and OE<sub>B</sub> simultaneously will cause both banks to be deselected. Reading is accomplished in the direct mode by tying OE<sub>A</sub> and OE<sub>B</sub> together externally. A<sub>12</sub> will determine which 4 K x 16 memory bank is enabled.

7

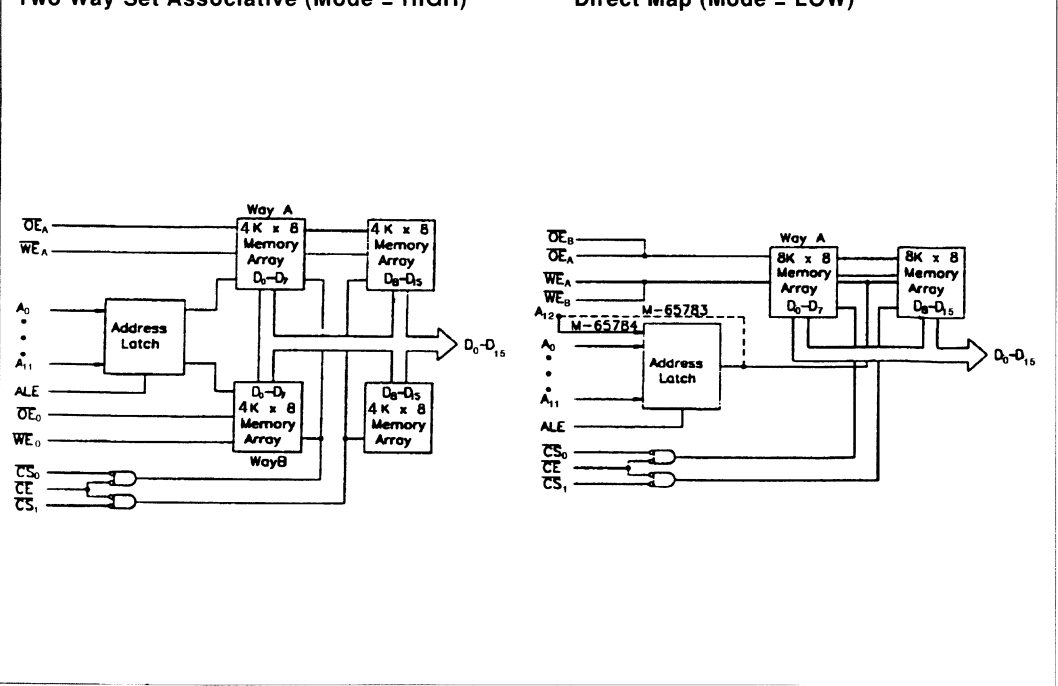
PIN DIAGRAM



LOGIC BLOCK DIAGRAMS

Two Way Set Associative (Mode = HIGH)

Direct Map (Mode = LOW)



## SELECTION GUIDE

|                                        |            | M-65783-25<br>M-65784-25 | M-65783-35<br>M-65784-35 | M-65783-45<br>M-65784-45 |
|----------------------------------------|------------|--------------------------|--------------------------|--------------------------|
| Maximum Address Access Time (ns)       | Commercial | 25                       | 35                       | 45                       |
| Maximum output Enable Access Time (ns) | Commercial | 10                       | 14                       | 16                       |
| Maximum Operating Current (mA)         | Commercial | 220                      | 170                      | 140                      |

## MAXIMUM RATINGS

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature . . . . . - 65 °C to + 150 °C  
 Ambient Temperature with  
 Power Applied . . . . . 0 °C to + 70 °C  
 Supply Voltage to ground Potential . - 0.5 V to + 7.0 V  
 DC Voltage Applied to Outputs  
 in High Z State . . . . . - 0.5 V to + 7.0 V  
 DC Input Voltage . . . . . - 3.0 V to + 7.0 V  
 Output Current into Outputs (Low) . . . . . 20 mA

Static Discharge Voltage . . . . . > 2001 V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current . . . . . > 200 mA

## OPERATING RANGE

| RANGE      | AMBIENT<br>TEMPERATURE | V <sub>CC</sub> |
|------------|------------------------|-----------------|
| Commercial | 0°C to + 70°C          | 5 V ± 10 %      |

## ELECTRICAL CHARACTERISTICS OVER THE OPERATING RANGE

| PARAMETERS      | DESCRIPTION                                       | TEST<br>CONDITIONS                                                                                    | M-65783-25<br>M-65784-25 |                 | M-65783-35<br>M-65784-35 |                 | M-65783-45<br>M-65784-45 |                 | UNITS |
|-----------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------|--------------------------|-----------------|--------------------------|-----------------|--------------------------|-----------------|-------|
|                 |                                                   |                                                                                                       | MIN.                     | MAX.            | MIN.                     | MAX.            | MIN.                     | MAX.            |       |
| V <sub>OH</sub> | Output HIGH<br>Voltage                            | V <sub>CC</sub> = Min.,<br>I <sub>OH</sub> = -1.0 mA                                                  | 2.4                      |                 | 2.4                      |                 | 2.4                      |                 | V     |
| V <sub>OL</sub> | Output LOW<br>Voltage                             | V <sub>CC</sub> = MIN.,<br>I <sub>OL</sub> = 4.0 mA                                                   |                          | 0.4             |                          | 0.4             |                          | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH<br>Voltage                             |                                                                                                       | 2.2                      | V <sub>CC</sub> | 2.2                      | V <sub>CC</sub> | 2.2                      | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW<br>Voltage                              |                                                                                                       | -3.0                     | 0.8             | -3.0                     | 0.8             | -3.0                     | 0.8             | V     |
| I <sub>IX</sub> | Input Load<br>Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                | -10                      | +10             | -10                      | +10             | -10                      | +10             | μ     |
| I <sub>OZ</sub> | Output Leakage<br>Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled                                           | -10                      | +10             | -10                      | +10             | -10                      | +10             | μ     |
| I <sub>OS</sub> | Output Short<br>Circuit<br>Current <sup>(1)</sup> | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND                                                     |                          | -350            |                          | -350            |                          | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating<br>Supply<br>Current    | V <sub>CC</sub> =Max.<br>I <sub>OUT</sub> =0mA<br>Read<br>Cycle <sup>(2)</sup><br>Duty Cycle<br>= 45% |                          | 220             |                          | 170             |                          | 140             | mA    |

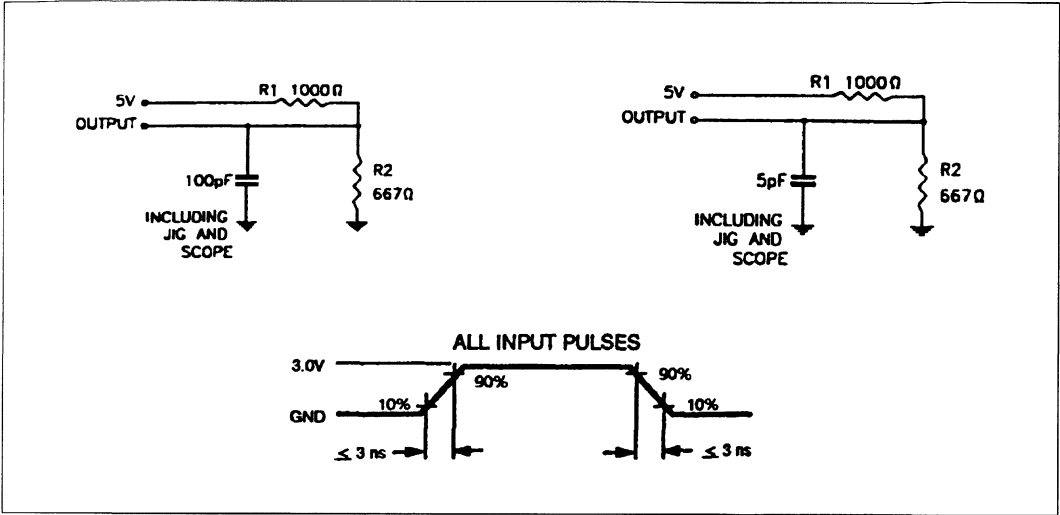
**Notes :** 1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.  
 2. At a given duty cycle, Write Cycle I<sub>CC</sub> is equal to 1.4 times Read Cycle I<sub>CC</sub>.

**7**

CAPACITANCE <sup>(3)</sup>

| PARAMETERS       | DESCRIPTION        | TEST CONDITIONS                                              | MAX. | UNITS |
|------------------|--------------------|--------------------------------------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0 V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |                                                              | 7    | pF    |

AC TEST LOADS AND WAVEFORMS



Note : 3. Tested initially and after any design or process changes that may affect these parameters.

# M 65783/M 65784

## SWITCHING CHARACTERISTICS OVER THE OPERATING RANGE <sup>(4)</sup>

| PARAMETERS                                     | DESCRIPTION                           | M-65783-25 |      | M-65783-35 |      | M-65783-45 |      | UNITS |
|------------------------------------------------|---------------------------------------|------------|------|------------|------|------------|------|-------|
|                                                |                                       | M-65784-25 |      | M-65784-35 |      | M-65784-45 |      |       |
|                                                |                                       | MIN.       | MAX. | MIN.       | MAX. | MIN.       | MAX. |       |
| READ CYCLE <sup>(5)</sup>                      |                                       |            |      |            |      |            |      |       |
| t <sub>RC</sub>                                | Read Cycle Time                       | 25         |      | 35         |      | 45         |      | ns    |
| t <sub>AA</sub>                                | Address to Data Valid                 |            | 25   |            | 35   |            | 45   | ns    |
| t <sub>AA</sub> A <sub>12</sub> <sup>(6)</sup> | Address to Data Valid A <sub>12</sub> |            | 17   |            | 25   |            | 35   | ns    |
| t <sub>CE</sub>                                | Chip Enable to Data Valid             |            | 12   |            | 15   |            | 20   | ns    |
| t <sub>CS</sub>                                | Chip Select to Data Valid             |            | 12   |            | 15   |            | 20   | ns    |
| t <sub>OE</sub>                                | Output Enable to Data Valid           |            | 10   |            | 14   |            | 16   | ns    |
| t <sub>OHA</sub>                               | Output Hold from Address Change       | 3          |      | 3          |      | 3          |      | ns    |
| t <sub>OHL</sub>                               | Output Hold from ALE HIGH             | 3          |      | 3          |      | 3          |      | ns    |
| t <sub>LZCE</sub>                              | Chip Enable to Low Z                  | 3          |      | 3          |      | 3          |      | ns    |
| t <sub>LZOE</sub>                              | Output Enable to Low Z                | 0          |      | 0          |      | 0          |      | ns    |
| t <sub>HZCE</sub>                              | Chip Enable to High Z                 |            | 15   |            | 25   |            | 30   | ns    |
| t <sub>HZOE</sub>                              | Output Enable to High Z               |            | 9    |            | 10   |            | 12   | ns    |
| t <sub>PALE</sub>                              | ALE Pulse Width                       | 8          |      | 10         |      | 12         |      | ns    |
| t <sub>SALE</sub>                              | Address Set-Up to ALE Low             | 4          |      | 6          |      | 8          |      | ns    |
| t <sub>HALE</sub>                              | Address Hold to ALE Low               | 4          |      | 4          |      | 4          |      | ns    |
| WRITE CYCLE <sup>(7)</sup>                     |                                       |            |      |            |      |            |      |       |
| t <sub>WC</sub>                                | Write cycle Time                      | 25         |      | 35         |      | 45         |      | ns    |
| t <sub>AW</sub>                                | Address Set-up to Write End           | 20         |      | 30         |      | 40         |      | ns    |
| t <sub>SCE</sub>                               | Chip Enable to Write End              | 20         |      | 25         |      | 30         |      | ns    |
| t <sub>SCS</sub>                               | Chip Select to Write End              | 20         |      | 25         |      | 30         |      | ns    |
| t <sub>SD</sub>                                | Data Set-Up to Write End              | 10         |      | 10         |      | 10         |      | ns    |
| t <sub>HD</sub>                                | Data Hold from Write End              | 0          |      | 0          |      | 0          |      | ns    |
| t <sub>PWE</sub>                               | Write Enable Pulse Width              | 20         |      | 25         |      | 30         |      | ns    |
| t <sub>SA</sub>                                | Address Set-Up to Write Enable        | 0          |      | 0          |      | 0          |      | ns    |
| t <sub>HA</sub>                                | Address Hold from Write Enable        | 0          |      | 0          |      | 0          |      | ns    |
| t <sub>LZWE</sub>                              | Write Enable HIGH to Low Z            | 3          |      | 3          |      | 3          |      | ns    |
| t <sub>HZWE</sub>                              | $\overline{WE}$ LOW to High Z         |            | 15   |            | 15   |            | 20   | ns    |
| t <sub>PALE</sub>                              | ALE Pulse Width                       | 8          |      | 10         |      | 12         |      | ns    |
| t <sub>SALE</sub>                              | Address Set-Up to ALE Low             | 4          |      | 6          |      | 8          |      | ns    |
| t <sub>HALE</sub>                              | Address Hold to ALE Low               | 4          |      | 4          |      | 4          |      | ns    |

**Notes :** 4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I<sub>OL</sub>, I<sub>OH</sub> and 100 pF load capacitance.

5. Both WE<sub>A</sub> and WE<sub>B</sub> must be HIGH to read cycle.

6. M-65783 only.

7. The internal write time of the memory is defined by the overlap  $\overline{CE}$ ,  $\overline{CS}_x$  and  $\overline{WE}_x$ . All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

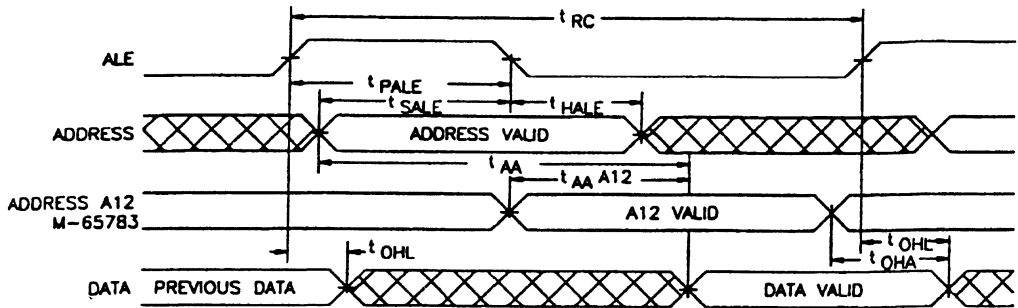
8. Device is continuously selected.  $\overline{CE}$  and  $\overline{CS}$  are LOW.

9. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

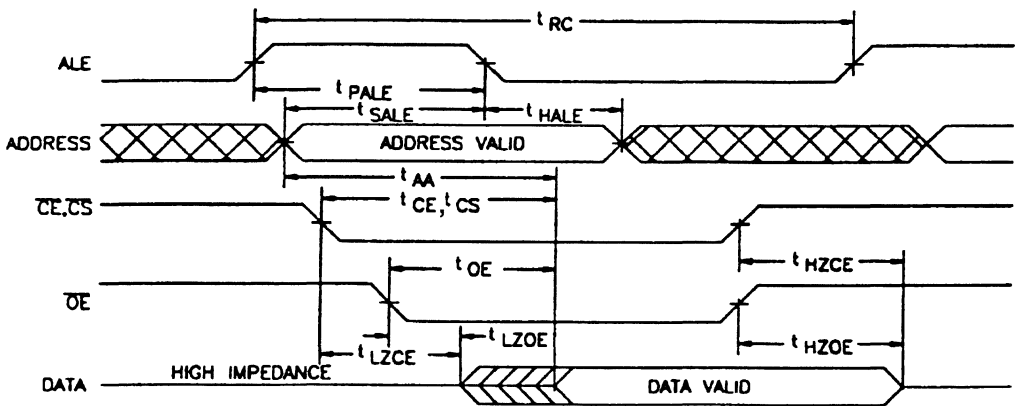
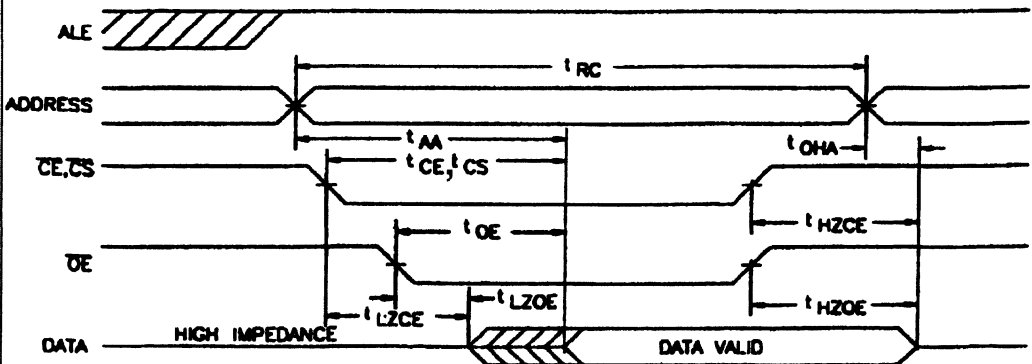
10. WE is HIGH for read cycle.

11. OE is deselected (HIGH).

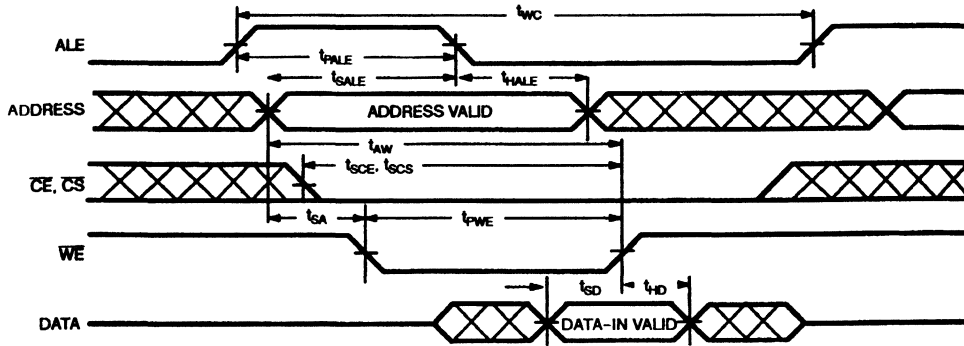
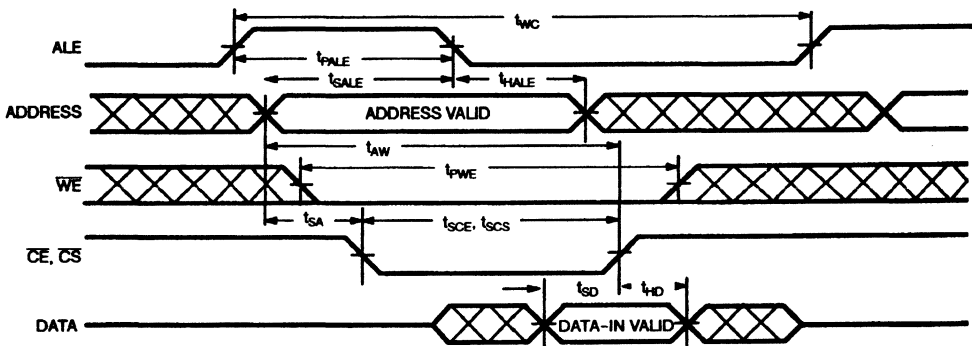
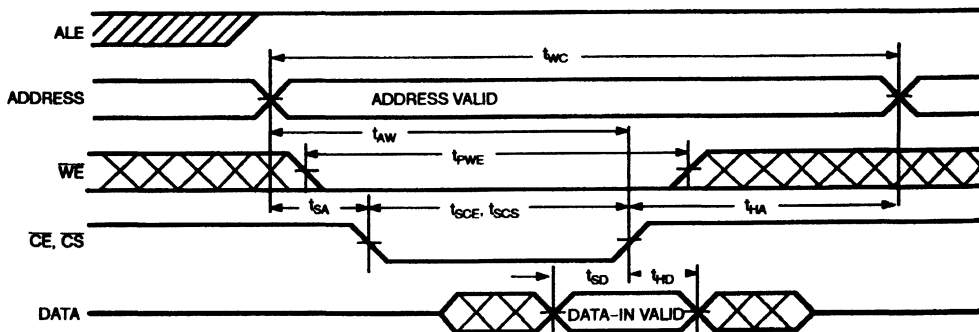
## SWITCHING WAVEFORMS

READ CYCLE No. 1 (ALE = CLOCK) <sup>(8)</sup>

READ CYCLE No. 2 (ALE = CLOCK)

READ CYCLE No 3 (ALE = HIGH) <sup>(9, 10)</sup>

## SWITCHING WAVEFORMS (continued)

READ CYCLE No. 1 (ALE = CLOCK  $\overline{WE}$  Controlled) <sup>(11)</sup>READ CYCLE No. 2 (ALE = CLOCK,  $\overline{CE}/\overline{CS}$  Controlled) <sup>(11)</sup>WRITE CYCLE No 3 (ALE = HIGH,  $\overline{CE}/\overline{CS}$  Controlled) <sup>(11)</sup>

## TRUTH TABLES

## Two-Way Mode (Mode = HIGH)

| CE | CS <sub>0</sub> | CS <sub>1</sub> | OE <sub>A</sub> | OE <sub>B</sub> | WE <sub>A</sub> | WE <sub>B</sub> | OPERATION                                           |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------------------------------------------|
| H  | X               | X               | X               | X               | X               | X               | Outputs High Z, Write Disabled                      |
| L  | H               | H               | X               | X               | X               | X               | Outputs High Z, Write Disabled                      |
| X  | X               | X               | H               | H               | X               | X               | Outputs High Z                                      |
| X  | X               | X               | L               | L               | X               | X               | Outputs High Z                                      |
| L  | L               | H               | L               | H               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub> Way A       |
| L  | L               | H               | H               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub> Way B       |
| L  | H               | L               | L               | H               | H               | H               | Read I/O <sub>8</sub> -I/O <sub>15</sub> Way A      |
| L  | H               | L               | H               | L               | H               | H               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way B     |
| L  | L               | L               | L               | H               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub> Way A      |
| L  | L               | L               | H               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub> Way B      |
| L  | L               | H               | X               | X               | L               | H               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way A      |
| L  | L               | H               | X               | X               | H               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way B      |
| L  | H               | L               | X               | X               | L               | H               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way A     |
| L  | H               | L               | X               | X               | H               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way B     |
| L  | L               | L               | X               | X               | L               | H               | Write I/O <sub>0</sub> -I/O <sub>15</sub> Way A     |
| L  | L               | L               | X               | X               | H               | L               | Write I/O <sub>0</sub> -I/O <sub>15</sub> Way B     |
| L  | L               | H               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way A & B  |
| L  | H               | L               | X               | X               | L               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way A & B |
| L  | L               | L               | X               | X               | L               | L               | Write I/O <sub>0</sub> I/O <sub>15</sub> Way A & B  |

## DIRECT MODE (Mode = LOW)

| CE | CS <sub>0</sub> | CS <sub>1</sub> | OE <sub>A</sub> | OE <sub>B</sub> | WE <sub>A</sub> | WE <sub>B</sub> | OPERATION                                 |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------------------------|
| H  | X               | X               | X               | X               | X               | X               | Outputs High Z, Write Disabled            |
| L  | H               | H               | X               | X               | X               | X               | Outputs High Z, Write Disabled            |
| X  | X               | X               | H               | H               | X               | X               | Outputs High Z                            |
| L  | L               | H               | L               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub>   |
| L  | H               | L               | L               | L               | H               | H               | Read I/O <sub>8</sub> -I/O <sub>15</sub>  |
| L  | L               | L               | L               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub>  |
| L  | L               | H               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub>  |
| L  | H               | L               | X               | X               | L               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> |
| L  | L               | L               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>15</sub> |



ORDERING INFORMATION

| Memory | Package             | Device Type | Speed      |
|--------|---------------------|-------------|------------|
| M      | S –                 | 65783 –     | 25         |
|        | ↓                   | 65784       | 25         |
|        | S = PLCC 52         |             | 25 = 25 ns |
|        |                     |             | 35 = 35 ns |
|        | → Temperature Range |             | 45 = 45 ns |
|        | Blank : Commercial  |             |            |



# VERY LOW POWER CMOS SRAM

8





# DATA SHEET

# HM 65162

## 2 k x 8 VERY LOW POWER CMOS SRAM

### FEATURES

- **ACCESS TIME**  
MILITARY/INDUSTRIAL : 70/85 ns (max)  
COMMERCIAL : 55/70 ns (max)
- **VERY LOW POWER CONSUMPTION**  
ACTIVE : 240 mW (typ)  
STANDBY : 2.0  $\mu$ W (typ)  
DATA RETENTION : 0.8  $\mu$ W (typ)
- **WIDE TEMPERATURE RANGE : - 55 TO + 125°C**
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN  
RESISTORS ARE REQUIRED**

### DESCRIPTION

The HM 65162 is a very low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.

The HM 65162 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1  $\mu$ A) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Easy memory expansion is provided by an active low chip select (CS), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM-65162 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65162 is processed following the test methods of MIL STD 883C.

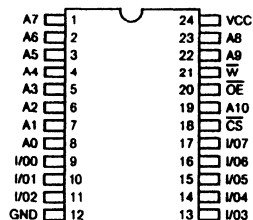
8

### PACKAGES

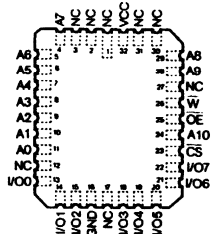
Plastic 600 mils, 24 pins, DIL.  
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

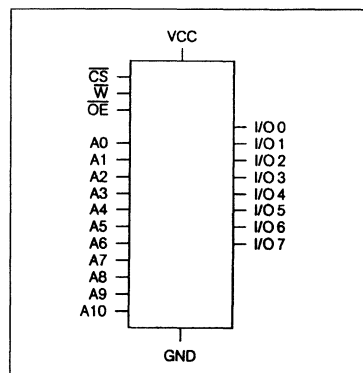
Pinout DIL 24 pins (top view)



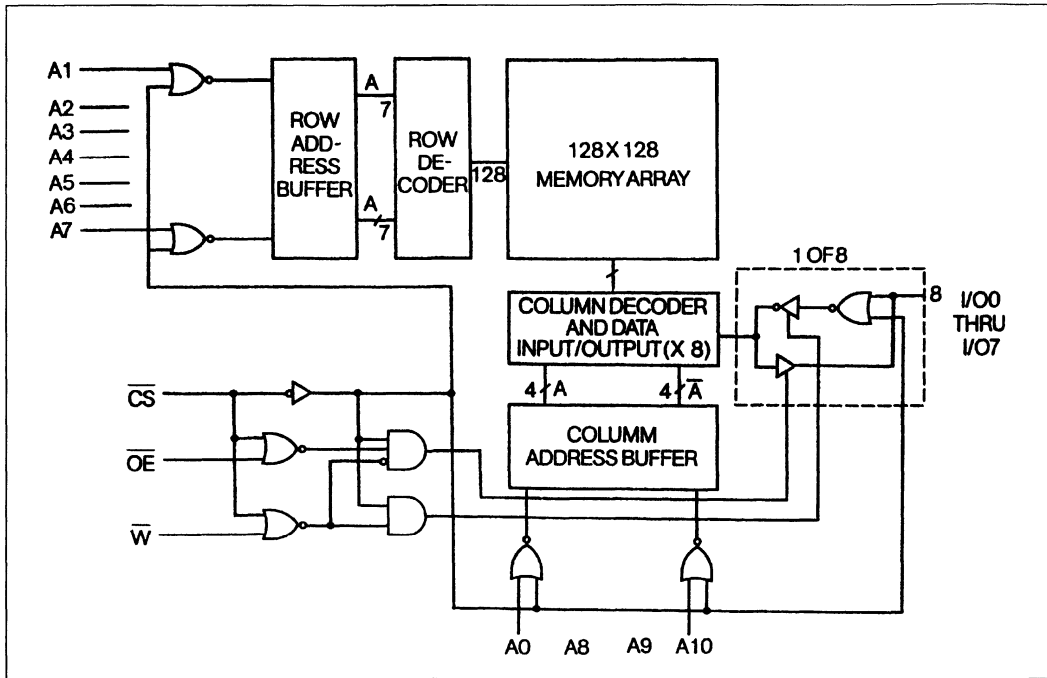
Pinout LCC 32 pins (top view)



### LOGIC SYMBOL



**8-4**



## PIN NAMES

|                          |                                        |
|--------------------------|----------------------------------------|
| A0-A10 : Address inputs  | $\overline{\text{CS}}$ : Chip Select   |
| I/O0-I/O7 : Input/Output | $\overline{\text{OE}}$ : Output Enable |
| Vcc : Power              | $\overline{\text{W}}$ : Write enable   |
| GND : Ground             |                                        |

## TRUTH TABLE

| <b>CS</b> | <b>OE</b> | <b>W</b> | <b>DATA-IN</b> | <b>DATA-OUT</b> | <b>MODE</b> |
|-----------|-----------|----------|----------------|-----------------|-------------|
| H         | X         | X        | Z              | Z               | Deselect    |
| L         | L         | H        | Z              | Valid           | Read        |
| L         | H         | L        | Valid          | Z               | Write       |
| L         | L         | L        | Valid          | Z               | Write       |

L = low, H = high, X = H or L, Z = high impedance.

**ABSOLUTE MAXIMUM RATINGS**Supply voltage to GND potential :  $-0.5\text{ V}$  to  $+7.0\text{ V}$ Input or Output voltage applied :  $(\text{Gnd} - 0.3\text{ V})$  to  $(\text{Vcc} + 0.3\text{ V})$ Storage temperature :  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ **OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                           |
|------------|-------|-----------------------|-------------------------------------------------|
| Military   | (- 2) | $\text{Vcc} \pm 10\%$ | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $\text{Vcc} \pm 10\%$ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $\text{Vcc} \pm 10\%$ | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM                     | UNIT |
|-----------|--------------------|---------|---------|-----------------------------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5                         | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0                         | V    |
| VIL (1)   | Input low voltage  | $-0.3$  | 0.0     | 0.8                         | V    |
| VIH       | Input high voltage | 2.2     | —       | $\text{Vcc} + 0.3\text{ V}$ | V    |

Note : 1. VIL min =  $-0.3\text{ V}$  or  $-1.0\text{ V}$  pulse width 50 ns.**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | —       | —       | 5       | pF   |
| Cout (2)  | Output capacitance | —       | —       | 7       | pF   |

Note : 2. TA =  $25^{\circ}\text{C}$ , f = 1 MHz, Vcc = 5.0 V, these parameters are not 100% tested.

**ELECTRICAL CHARACTERISTICS DC PARAMETER**

| PARAMETER |     | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------|---------|---------|---------|---------|
| IIX       | (3) | Input leakage current  | - 1.0   | -       | 1.0     | $\mu$ A |
| IOZ       | (3) | Output leakage current | - 1.0   | -       | 1.0     | $\mu$ A |
| VOL       | (4) | Output low voltage     | -       | -       | 0.4     | V       |
| VOH       | (4) | Output high voltage    | 2.4     | -       | -       | V       |

Notes : 3.  $Gnd < VIN < Vcc$ ,  $Gnd < Vout < Vcc$  Output disabled.  
 4.  $Vcc$  min,  $IOL = 4.0mA$ ,  $IOH = - 1.0mA$ .

**Consumption for Commercial specification (- 5) :**

| SYMBOL |     | PARAMETER                | 65162<br>B-5 | 65162<br>-5 | 65162<br>C-5 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 2.0          | 2.0         | 2.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 1.0          | 1.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |

**Consumption for Industrial specification (- 9) :**

| SYMBOL |     | PARAMETER                | 65162<br>B-9 | 65162<br>-9 | 65162<br>C-9 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 3.0          | 3.0         | 3.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 5.0          | 5.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |

**Consumption for Military specification (- 2) :**

| SYMBOL |     | PARAMETER                | 65162<br>B-2 | 65162<br>-2 | 65162<br>C-2 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 5.0          | 5.0         | 5.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 50.0         | 50.0        | 500.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 70.0         | 70.0        | 70.0         | mA      | max   |

Notes : 5.  $\overline{CS} \geq VIH$ .  
 6.  $\overline{CS} \geq Vcc - 0.3V$ ,  $I_{out} = 0mA$ .  
 7.  $\overline{CS} \leq VIL$ ,  $I_{out} = 0mA$ ,  $V_{in} = Gnd/Vcc$ .  
 8.  $Vcc$  max,  $I_{out} = 0mA$ ,  $f = 1MHz$  and  $5mA/MHz$ ,  $V_{in} = Gnd/Vcc$ .



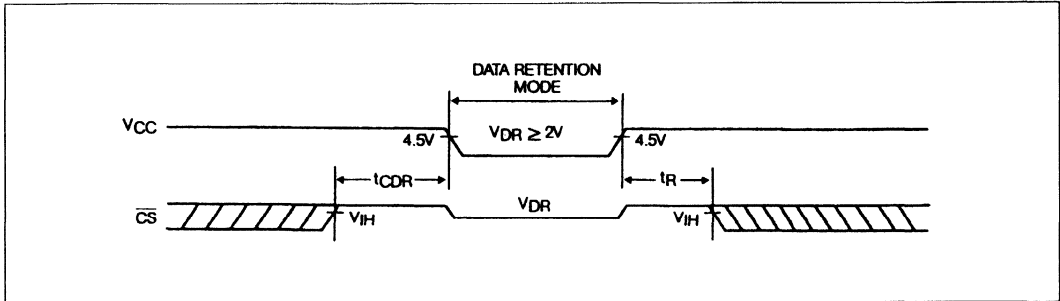
**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the

RAM outputs high impedance, minimizing power dissipation.

3.  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3$  V and 70% of  $V_{CC}$  during the power up and power down transitions.
4. The RAM can begin operation > 55 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

**TIMING****DATA RETENTION CHARACTERISTICS**

| PARAMETER   | DESCRIPTION                                     | MINIMUM    | TYPICAL<br>(9) | MAXIMUM | UNIT |
|-------------|-------------------------------------------------|------------|----------------|---------|------|
| VCCDR       | V <sub>CC</sub> for data retention              | 2.0        | —              | —       | V    |
| TCDR        | Chip deselect to data retention time            | 0.0        | —              | —       | ns   |
| TR          | Operation recovery time                         | TAVAV (10) | —              | —       | ns   |
| ICCDR1 (11) | Data retention current<br>2.0 V : HM-65162(B)-5 | —          | 0.1            | 1.0     | μA   |
|             | HM-65162(B)-9                                   | —          | 0.1            | 2.0     | μA   |
|             | HM-65162(B)-2                                   | —          | 0.1            | 20.0    | μA   |
|             | HM-65162C-5                                     | —          | 0.1            | 30.0    | μA   |
|             | HM-65162C-9                                     | —          | 0.1            | 30.0    | μA   |
|             | HM-65162C-2                                     | —          | 0.1            | 200.0   | μA   |
| ICCDR2 (11) | Data retention current<br>3.0 V : HM-65162(B)-5 | —          | 0.3            | 1.0     | μA   |
|             | HM-65162(B)-9                                   | —          | 0.3            | 3.0     | μA   |
|             | HM-65162(B)-2                                   | —          | 0.3            | 30.0    | μA   |
|             | HM-65162C-5                                     | —          | 0.3            | 50.0    | μA   |
|             | HM-65162C-9                                     | —          | 0.3            | 50.0    | μA   |
|             | HM-65162C-2                                     | —          | 0.3            | 300.0   | μA   |

Notes : 9. TA = 25 °C.

10. TAVAV = Read cycle time.

11. CS = V<sub>CC</sub>, Vin = Gnd/V<sub>CC</sub>, this parameter is only tested to V<sub>CC</sub> = 2 V.

**ELECTRICAL CHARACTERISTICS AC PARAMETERS****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output load : 1 TTL gate + 100 pF

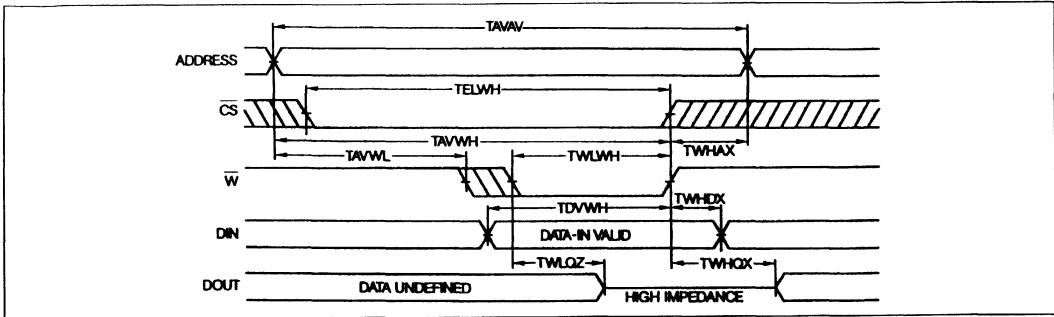
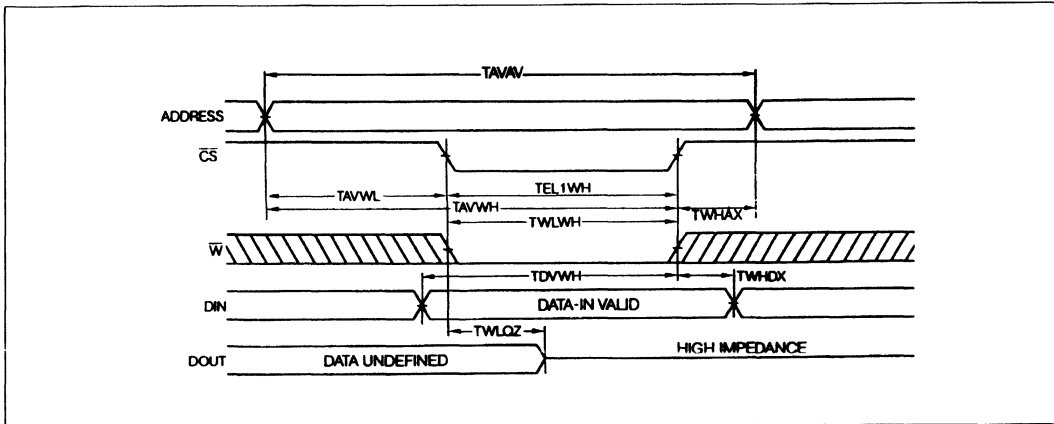
**WRITE CYCLE : Commercial specification**

| SYMBOL     | PARAMETER                        | 65162<br>B-5 | 65162<br>-5 | 65162<br>C-5 | UNIT | VALUE |
|------------|----------------------------------|--------------|-------------|--------------|------|-------|
| TAVAV      | Write cycle time                 | 55           | 70          | 70           | ns   | min   |
| TAVWL      | Address set-up time              | 0            | 0           | 0            | ns   | min   |
| TAVWH      | Address valid to end of write    | 45           | 50          | 50           | ns   | min   |
| TDVWH      | Data set-up time                 | 25           | 30          | 30           | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 40           | 45          | 45           | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 35           | 40          | 40           | ns   | max   |
| TWLWH      | Write pulse width                | 35           | 40          | 40           | ns   | min   |
| TWHAX      | Address hold to end of write     | 10           | 10          | 10           | ns   | min   |
| TWHDX      | Data hold time                   | 10           | 10          | 10           | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0            | 0           | 0            | ns   | min   |

**WRITE CYCLE : Industrial and Military specification**

| SYMBOL     | PARAMETER                        | 65162<br>B-9/2 | 65162<br>-9/2 | 65162<br>C-9/2 | UNIT | VALUE |
|------------|----------------------------------|----------------|---------------|----------------|------|-------|
| TAVAV      | Write cycle time                 | 70             | 85            | 85             | ns   | min   |
| TAVWL      | Address set-up time              | 0              | 0             | 0              | ns   | min   |
| TAVWH      | Address valid to end of write    | 50             | 65            | 65             | ns   | min   |
| TDVWH      | Data set-up time                 | 30             | 30            | 30             | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 45             | 55            | 55             | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 40             | 50            | 50             | ns   | max   |
| TWLWH      | Write pulse width                | 40             | 55            | 55             | ns   | min   |
| TWHAX      | Address hold to end of write     | 10             | 10            | 10             | ns   | min   |
| TWHDX      | Data hold time                   | 10             | 10            | 10             | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0              | 0             | 0              | ns   | min   |

**Note :** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED) (note 13)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED) (note 13)

**Note :** 13. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
Data I/O Pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.

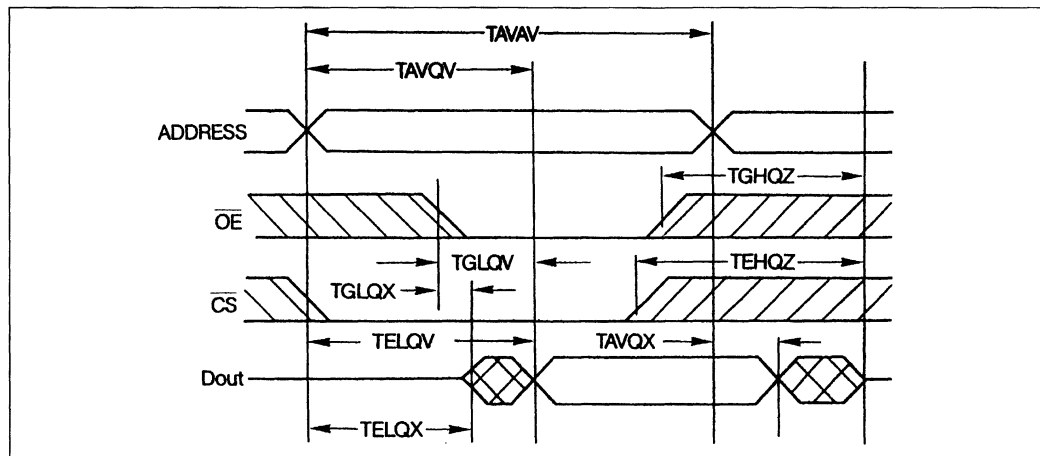
## READ CYCLE : Commercial specification

| SYMBOL | PARAMETER                 | 65162<br>B-5 | 65162<br>-5 | 65162<br>C-5 | UNIT | VALUE |
|--------|---------------------------|--------------|-------------|--------------|------|-------|
| TAVAV  | READ cycle time           | 55           | 70          | 70           | ns   | min   |
| TAVQV  | Address access time       | 55           | 70          | 70           | ns   | max   |
| TAVQX  | Address valid to low Z    | 5            | 5           | 5            | ns   | min   |
| TELQV  | Chip-select access time   | 55           | 70          | 70           | ns   | max   |
| TELQZ  | CS low to low Z           | 5            | 5           | 5            | ns   | min   |
| TEHQZ  | CS high to high Z         | 35           | 50          | 50           | ns   | max   |
| TGLQV  | Output enable access time | 40           | 50          | 50           | ns   | max   |
| TGLQX  | OE low to low Z           | 5            | 5           | 5            | ns   | min   |
| TGHQZ  | OE high to high Z         | 35           | 40          | 40           | ns   | max   |

## READ CYCLE : Industrial and Military specification

| SYMBOL | PARAMETER                 | 65162<br>B-9/2 | 65162<br>-9/2 | 65162<br>C-9/2 | UNIT | VALUE |
|--------|---------------------------|----------------|---------------|----------------|------|-------|
| TAVAV  | READ cycle time           | 70             | 85            | 85             | ns   | min   |
| TAVQV  | Address access time       | 70             | 85            | 85             | ns   | max   |
| TAVQX  | Address valid to low Z    | 5              | 5             | 5              | ns   | min   |
| TELQV  | Chip-select access time   | 70             | 85            | 85             | ns   | max   |
| TELQX  | CS low to low Z           | 5              | 5             | 5              | ns   | min   |
| TEHQZ  | CS high to high Z         | 35             | 50            | 50             | ns   | max   |
| TGLQV  | Output Enable access time | 50             | 65            | 65             | ns   | max   |
| TGLQX  | OE low to low Z           | 5              | 5             | 5              | ns   | min   |
| TGHQZ  | OE high to high Z         | 35             | 40            | 40             | ns   | min   |

## READ CYCLE



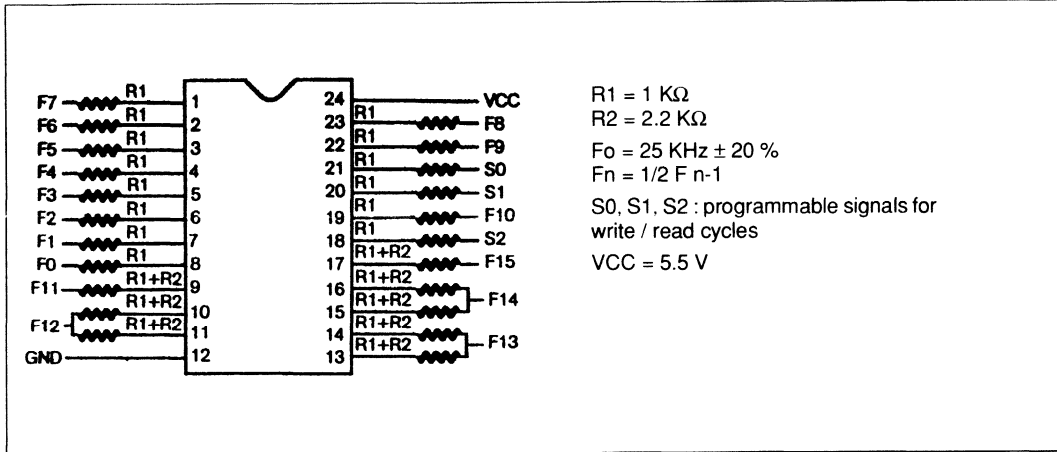
Addresses must remain stable for the duration of the read cycle. To read OE and CS must be < VIL and VIH. The output buffers can be controlled independently by OE while CS is low. To execute consecu-

tive read cycles, CS may be tied low continuously until all desired locations are accessed. When CS is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

ORDERING INFORMATION

| Package                                                                                                | Device Type                       | Grade                                                                            | Level                                                                                                  |
|--------------------------------------------------------------------------------------------------------|-----------------------------------|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| HM1                                                                                                    | 65162                             | B                                                                                | - 5                                                                                                    |
| 0 - Chip form<br>1 - Ceramic 24 pins<br>600 mils<br>3 - Plastic 24 pins<br>600 mils<br>4 - LCC 32 pins | 2 k x 8 very low power static RAM | B = high speed/low current<br>Blank : standard speed/low current<br>C : standard | - 5 : Commercial<br>- 9 : Industrial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

BURN-IN SCHEMATICS





## DATA SHEET

## HM 65262

# 16 k x 1 VERY LOW POWER CMOS SRAM

## FEATURES

- ACCESS TIME  
MILITARY/INDUSTRIAL : 70/85 ns (max)  
COMMERCIAL : 55/70 ns (max)
- VERY LOW POWER CONSUMPTION  
ACTIVE : 110 mW (typ)  
STANDBY : 2.0  $\mu$ W (typ)  
DATA RETENTION : 0.8  $\mu$ W (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN  
RESISTORS ARE REQUIRED

## DESCRIPTION

The HM 65262 is a very low power CMOS static RAM organized as 16384 x 1 bit. It is manufactured using the MHS high performance CMOS technology.

The HM 65262 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1  $\mu$ A) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Easy memory expansion is provided by an active low chip select ( $\overline{CS}$ ), an active low output enable ( $\overline{OE}$ ) and three state drivers.

All inputs and outputs of the HM 65262 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65262 is processed following the test methods of MIL STD 883C.

8

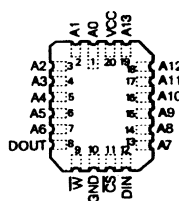
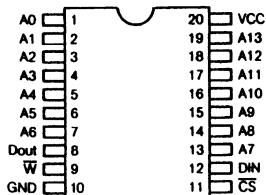
## PACKAGES

Plastic 300 mils, 20 pins, DIL.  
Ceramic 300 mils, 20 pins, DIL.

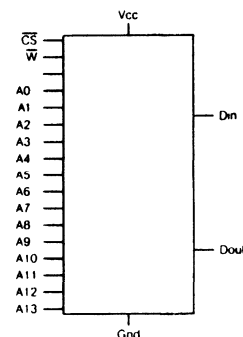
LCC, 20 pins.

Pinout DIL 20 pins (top view)

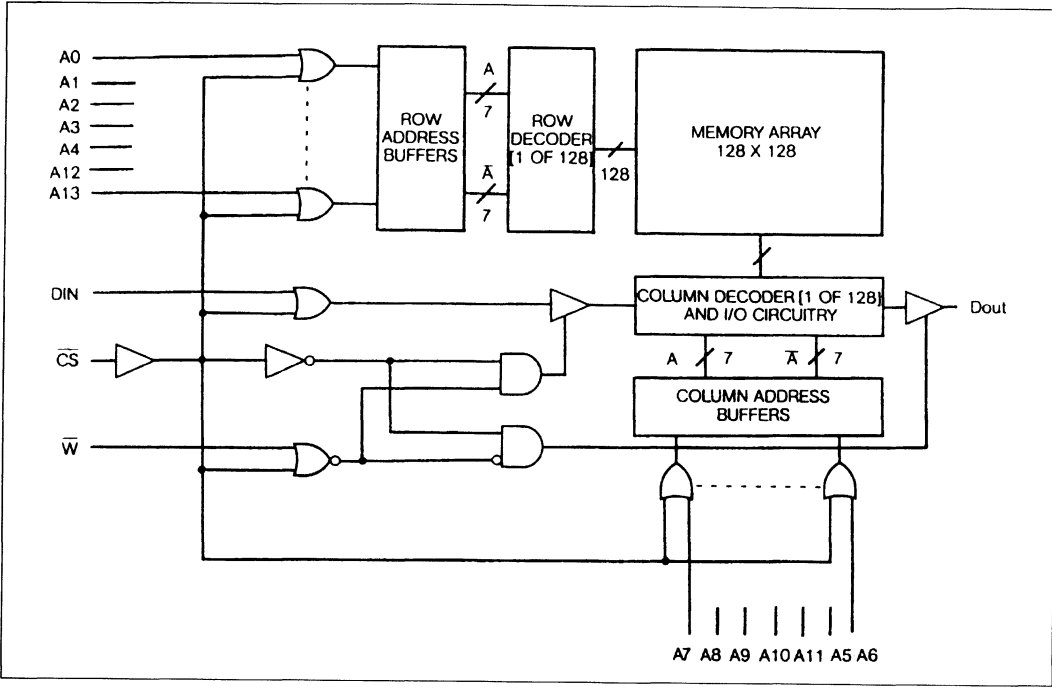
Pinout LCC 20 pins (top view)



## LOGIC SYMBOL



### BLOCK DIAGRAM



## PIN NAMES

|                               |                               |
|-------------------------------|-------------------------------|
| A0-A13 : Address inputs       | $\overline{W}$ : Write enable |
| Din : Input                   | VCC : Power                   |
| Dout : Output                 | GND : Ground                  |
| $\overline{CS}$ : Chip Select |                               |

### TRUTH TABLE

| CS | W | DATA-IN | DATA-OUT | MODE     |
|----|---|---------|----------|----------|
| H  | X | Z       | Z        | Deselect |
| L  | H | Z       | Valid    | Read     |
| L  | L | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance.



**ABSOLUTE MAXIMUM RATINGS**Supply voltage to GND potential :  $-0.3\text{ V}$  to  $+7.0\text{ V}$ Input or Output voltage applied :  $(\text{Gnd} - 0.3\text{ V})$  to  $(\text{Vcc} + 0.3\text{ V})$ Storage temperature :  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ **OPERATING RANGE**

|            |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                           |
|------------|-------|-----------------------|-------------------------------------------------|
| Military   | (- 2) | $\text{Vcc} \pm 10\%$ | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Industrial | (- 9) | $\text{Vcc} \pm 10\%$ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Commercial | (- 5) | $\text{Vcc} \pm 10\%$ | $-0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$   |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM                     | UNIT |
|-----------|--------------------|---------|---------|-----------------------------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5                         | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0                         | V    |
| VIL (1)   | Input low voltage  | $-0.3$  | 0.0     | 0.8                         | V    |
| VIH       | Input high voltage | 2.2     | —       | $\text{Vcc} + 0.3\text{ V}$ | V    |

Note : 1. VIL min =  $-0.3\text{ V}$  or  $-1.0\text{ V}$  pulse width 50 ns.**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | —       | —       | 8       | pF   |
| Cout (2)  | Output capacitance | —       | —       | 8       | pF   |

Note : 2. TA =  $25^{\circ}\text{C}$ , f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER |     | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT    |
|-----------|-----|------------------------|---------|---------|---------|---------|
| IIX       | (3) | Input leakage current  | - 1.0   | -       | 1.0     | $\mu$ A |
| IOZ       | (3) | Output leakage current | - 1.0   | -       | 1.0     | $\mu$ A |
| VOL       | (4) | Output low voltage     | -       | -       | 0.4     | V       |
| VOH       | (4) | Output high voltage    | 2.4     | -       | -       | V       |

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.

4. Vcc min, IOL = 8.0 mA, IOH = - 4.0 mA.

## Consumption for Commercial specification (- 5) :

| SYMBOL |     | PARAMETER                | 65262<br>B-5 | 65262<br>-5 | 65262<br>C-5 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 2.0          | 2.0         | 2.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 1.0          | 1.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |

## Consumption for Industrial specification (- 9) :

| SYMBOL |     | PARAMETER                | 65262<br>B-9 | 65262<br>-9 | 65262<br>C-9 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 3.0          | 3.0         | 3.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 5.0          | 5.0         | 100.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |

## Consumption for Military specification (- 2) :

| SYMBOL |     | PARAMETER                | 65262<br>B-2 | 65262<br>-2 | 65262<br>C-2 | UNIT    | VALUE |
|--------|-----|--------------------------|--------------|-------------|--------------|---------|-------|
| ICCSB  | (5) | Standby supply current   | 5.0          | 5.0         | 5.0          | mA      | max   |
| ICCSB1 | (6) | Standby supply current   | 50.0         | 50.0        | 500.0        | $\mu$ A | max   |
| ICC    | (7) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |
| ICCOP  | (8) | Operating supply current | 50.0         | 50.0        | 50.0         | mA      | max   |

Notes : 5. CS  $\geq$  VIH.

6. CS  $\geq$  Vcc - 0.3V, Iout = 0 mA.

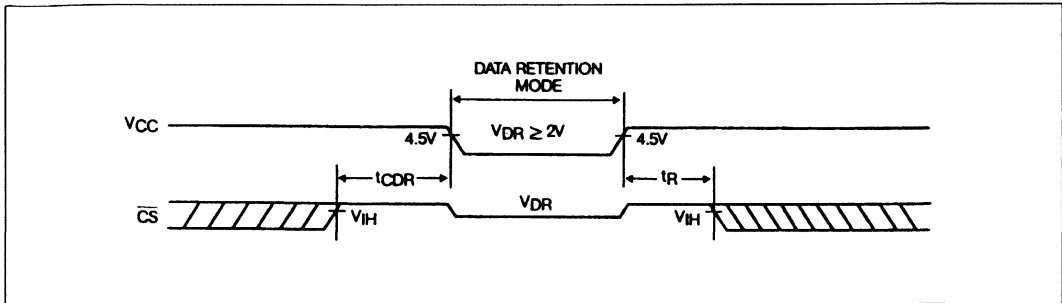
7. CS  $\leq$  VIL, Iout = 0 mA, Vin = Gnd/Vcc.

8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.
2.  $\overline{CS}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions.
3. The RAM can begin operation > 55 ns after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

**TIMING****DATA RETENTION CHARACTERISTICS**

| PARAMETER   | DESCRIPTION                                       | MINIMUM    | TYPICAL<br>( 9 ) | MAXIMUM | UNIT    |
|-------------|---------------------------------------------------|------------|------------------|---------|---------|
| VCCDR       | Vcc for data retention                            | 2.0        | —                | —       | V       |
| TCDR        | Chip deselect to data retention time              | 0.0        | —                | —       | ns      |
| TR          | Operation recovery time                           | TAVAV (10) | —                | —       | ns      |
| ICCDR1 (11) | Data retention current<br>@ 2.0 V : HM-65262(B)-5 | —          | 0.1              | 1.0     | $\mu$ A |
|             | HM-65262(B)-9                                     | —          | 0.1              | 2.0     | $\mu$ A |
|             | HM-65262(B)-2                                     | —          | 0.1              | 20.0    | $\mu$ A |
|             | HM-65262C-5                                       | —          | 0.1              | 30.0    | $\mu$ A |
|             | HM-65262C-9                                       | —          | 0.1              | 30.0    | $\mu$ A |
|             | HM-65262C-2                                       | —          | 0.1              | 200.0   | $\mu$ A |
| ICCDR2 (11) | Data retention current<br>@ 3.0 V : HM-65262(B)-5 | —          | 0.3              | 1.0     | $\mu$ A |
|             | HM-65262(B)-9                                     | —          | 0.3              | 3.0     | $\mu$ A |
|             | HM-65262(B)-2                                     | —          | 0.3              | 30.0    | $\mu$ A |
|             | HM-65262C-5                                       | —          | 0.3              | 50.0    | $\mu$ A |
|             | HM-65262C-9                                       | —          | 0.3              | 50.0    | $\mu$ A |
|             | HM-65262C-2                                       | —          | 0.3              | 300.0   | $\mu$ A |

Notes : 9.  $T_A = 25^\circ\text{C}$ .

10. TAVAV = Read cycle time.

11.  $\overline{CS} = V_{CC}$ ,  $V_{in} = \text{Gnd}/V_{CC}$ , this parameter is only tested to  $V_{CC} = 2$  V.

## ELECTRICAL CHARACTERISTICS AC PARAMETERS

## AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V  
 Input rise : 5 ns

Input timing reference levels : 1.5 V  
 Output load : 1 TTL gate + 100 pF

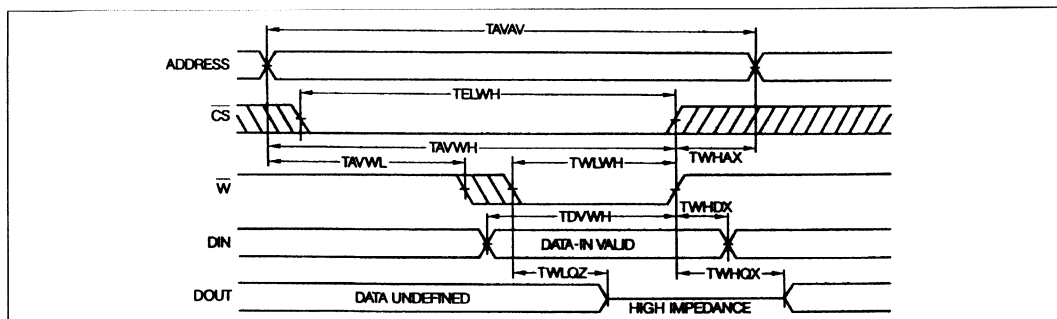
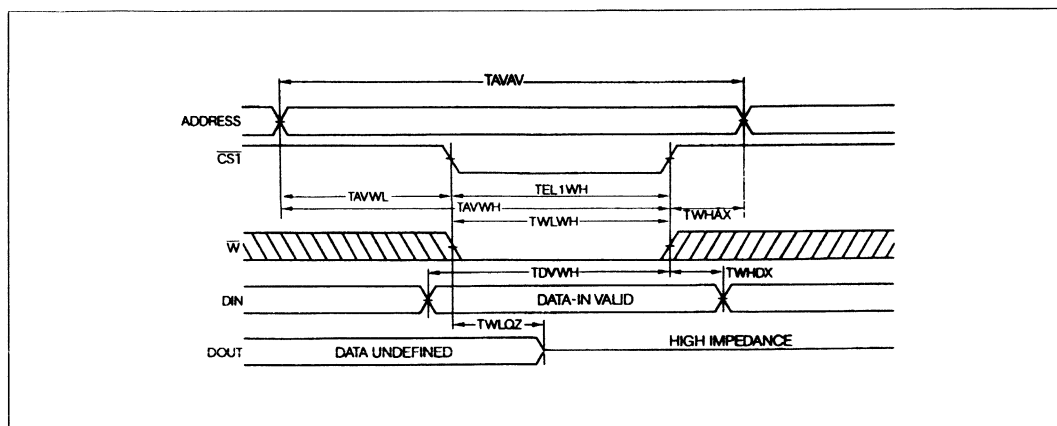
## WRITE CYCLE : Commercial specification

| SYMBOL     | PARAMETER                        | 65262<br>B-5 | 65262<br>-5 | 65262<br>C-5 | UNIT | VALUE |
|------------|----------------------------------|--------------|-------------|--------------|------|-------|
| TAVAV      | Write cycle time                 | 55           | 70          | 70           | ns   | min   |
| TAVWL      | Address set-up time              | 0            | 0           | 0            | ns   | min   |
| TAVWH      | Address valid to end of write    | 50           | 55          | 55           | ns   | min   |
| TDVWH      | Data set-up time                 | 35           | 40          | 40           | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 50           | 55          | 55           | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 35           | 40          | 40           | ns   | max   |
| TWLWH      | Write pulse width                | 50           | 55          | 55           | ns   | min   |
| TWHAX      | Address hold to end of write     | 0            | 0           | 0            | ns   | min   |
| TWHDX      | Data hold time                   | 0            | 0           | 0            | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0            | 0           | 0            | ns   | min   |

## WRITE CYCLE : Industrial and Military specification

| SYMBOL     | PARAMETER                        | 65262<br>B-9/2 | 65262<br>-9/2 | 65262<br>C-9/2 | UNIT | VALUE |
|------------|----------------------------------|----------------|---------------|----------------|------|-------|
| TAVAV      | Write cycle time                 | 70             | 85            | 85             | ns   | min   |
| TAVWL      | Address set-up time              | 0              | 0             | 0              | ns   | min   |
| TAVWH      | Address valid to end of write    | 55             | 65            | 65             | ns   | min   |
| TDVWH      | Data set-up time                 | 40             | 45            | 45             | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 55             | 65            | 65             | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 50             | 50            | 50             | ns   | max   |
| TWLWH      | Write pulse width                | 55             | 65            | 65             | ns   | min   |
| TWHAX      | Address hold to end of write     | 0              | 0             | 0              | ns   | min   |
| TWHDX      | Data hold time                   | 0              | 0             | 0              | ns   | min   |
| TWHQX (12) | Write high to low Z              | 0              | 0             | 0              | ns   | min   |

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ( $\overline{W}$  CONTROLLED) (note 13)WRITE CYCLE 2 ( $\overline{CS}$  CONTROLLED) (note 13)

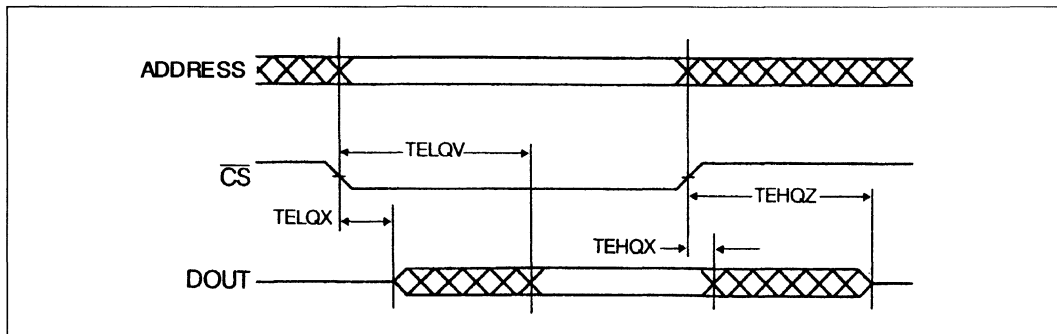
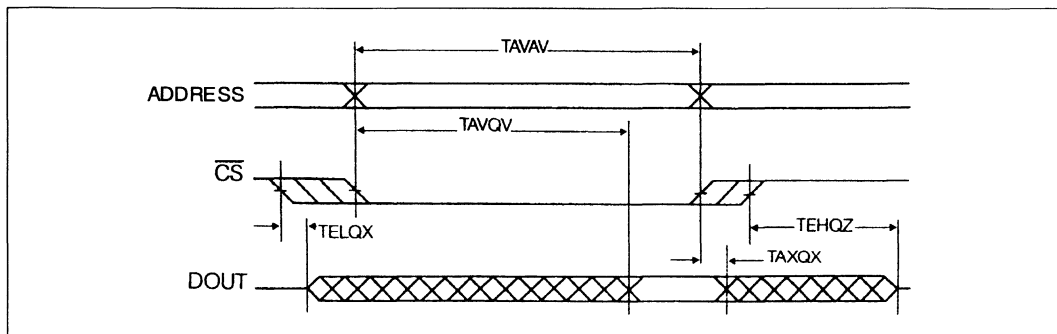
**Note : 13.** The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER                      | 65262<br>B-5 | 65262<br>-5 | 65262<br>C-5 | UNIT | VALUE |
|--------|--------------------------------|--------------|-------------|--------------|------|-------|
| TAVAV  | READ cycle time                | 55           | 70          | 70           | ns   | min   |
| TAVQV  | Address access time            | 55           | 70          | 70           | ns   | max   |
| TAVQX  | Address valid to low Z         | 5            | 5           | 5            | ns   | min   |
| TELQV  | Chip-select access time        | 55           | 70          | 70           | ns   | max   |
| TELQZ  | $\overline{CS}$ low to low Z   | 5            | 5           | 5            | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z | 40           | 40          | 40           | ns   | max   |

**READ CYCLE : Industrial and Military specification**

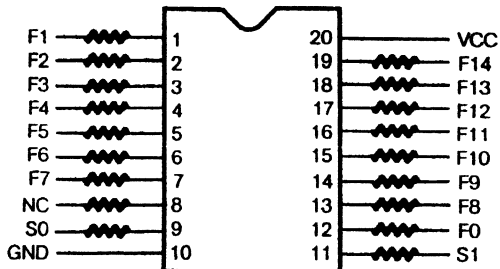
| SYMBOL | PARAMETER                      | 65262<br>B-9/2 | 65262<br>-9/2 | 65262<br>C-9/2 | UNIT | VALUE |
|--------|--------------------------------|----------------|---------------|----------------|------|-------|
| TAVAV  | READ cycle time                | 70             | 85            | 85             | ns   | min   |
| TAVQV  | Address access time            | 70             | 85            | 85             | ns   | max   |
| TAVQX  | Address valid to low Z         | 5              | 5             | 5              | ns   | min   |
| TELQV  | Chip-select access time        | 70             | 85            | 85             | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 5              | 5             | 5              | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z | 40             | 40            | 40             | ns   | max   |

**READ CYCLE nb 1****READ CYCLE nb 2**

### ORDERING INFORMATION

| Package                                                                                                | Device Type                        | Grade                                                                            | Level                                                                                                  |
|--------------------------------------------------------------------------------------------------------|------------------------------------|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| <u>HM1</u>                                                                                             | <u>65262</u>                       | <u>B</u>                                                                         | <u>- 5</u>                                                                                             |
| 0 - Chip form<br>1 - Ceramic 20 pins<br>300 mils<br>3 - Plastic 20 pins<br>300 mils<br>4 - LCC 20 pins | 16 k x 1 very low power static RAM | B = high speed/low current<br>Blank : standard speed/low current<br>C : standard | - 5 : Commercial<br>- 9 : Industrial<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. = Burn-in) |

### BURN-IN SCHEMATICS



$R = 1\text{ K}\Omega$   
 $F_0 = 50\text{ KHz} \pm 20\%$   
 $F_n = 1/2 F_{n-1}$   
 S0, S1 : programmable signals for write / read cycles  
 $VCC = 5.5\text{ V}$   
 NC = Not connected





# GENERAL PURPOSE CMOS SRAM

9





## DATA SHEET

## HM 6116

# 2 k x 8 GENERAL PURPOSE CMOS SRAM

## FEATURES

- ACCESS TIME
  - MILITARY : 120 ns (max)
  - INDUSTRIAL : 120 ns (max)
  - COMMERCIAL : 120 ns (max)
- LOW POWER CONSUMPTION
  - ACTIVE : 240 mW (typ)
  - STANDBY : 25  $\mu$ W (typ)
  - DATA RETENTION : 4  $\mu$ W (typ)
- 600 MILS WIDTH PACKAGE
  - TTL COMPATIBLE INPUTS AND OUTPUTS
  - ASYNCHRONOUS
  - SINGLE 5 VOLT SUPPLY
  - EQUAL CYCLE AND ACCESS TIME
  - NO CLOCK AND STROBES REQUIRED
  - GATED INPUTS
  - WIDE TEMPERATURE RANGE : - 55 TO + 125 °C

## DESCRIPTION

The HM 6116 is a low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology. 120 ns access time for commercial temperature range is available with a maximum power consumption of only 385 mW.

The HM 6116 features fully static operation requiring no external clocks or timing strobes. Thanks to the special input buffer "gated inputs", the circuit stays in stand by

mode when the  $\overline{CS}$  goes to an intermediate level ( $V_{IH}$ ). Easy memory expansion is provided by an active low chip select ( $\overline{CS}$ ), an active low output enable ( $\overline{OE}$ ) and three state drivers.

The HM 6116 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 6116 is processed following the test methods of MIL STD 883C.

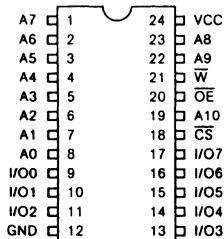
9

## PACKAGES

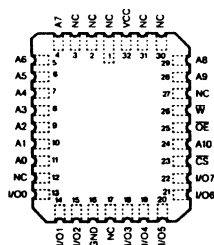
Plastic 600 mils, 24 pins, DIL.  
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

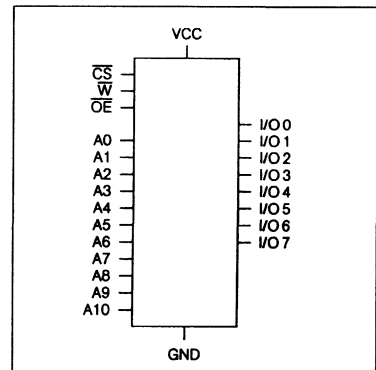
Pinout DIL 24 pins (top view)



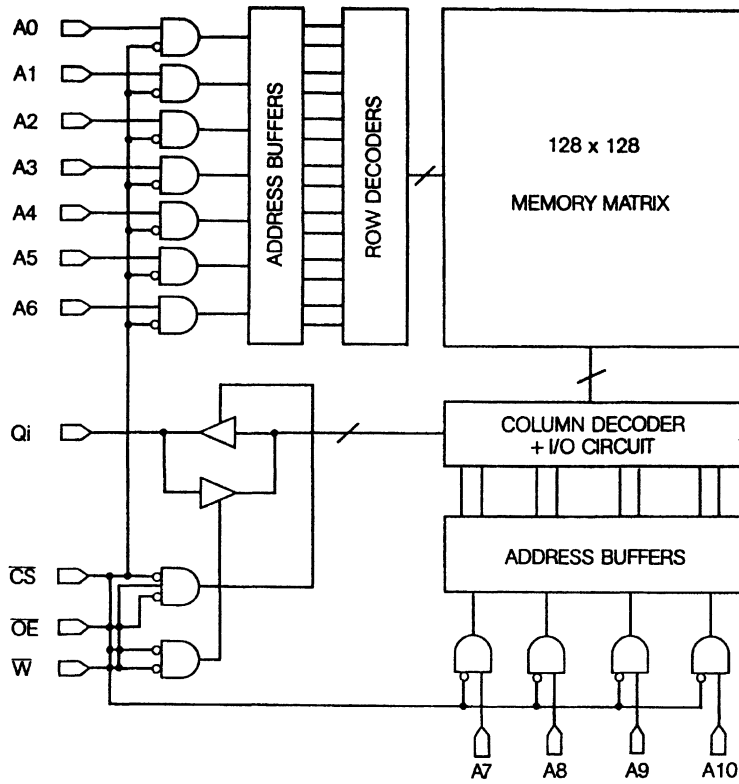
Pinout LCC 32 pins (top view)



## LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN NAMES

|                          |                                 |
|--------------------------|---------------------------------|
| A0-A10 : Address inputs  | $\overline{CS}$ : Chip Select   |
| I/O0-I/O7 : Input/Output | $\overline{OE}$ : Output enable |
| Vcc : Power              | $\overline{W}$ : Write Enable   |
| Gnd : Ground             |                                 |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE     |
|-----------------|-----------------|----------------|---------|----------|----------|
| H               | X               | X              | Z       | Z        | Deselect |
| L               | L               | H              | Z       | Valid    | Read     |
| L               | H               | L              | Valid   | Z        | Write    |
| L               | L               | L              | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = high impedance.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage to GND potential :  $-0.3\text{ V}$  to  $+7.0\text{ V}$

Input or Output voltage applied :  $(\text{Gnd} - 0.3\text{ V})$  to  $(\text{Vcc} + 0.3\text{ V})$

Storage temperature :  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

| OPERATING RANGE |       | OPERATING VOLTAGE     | OPERATING TEMPERATURE                           |
|-----------------|-------|-----------------------|-------------------------------------------------|
| Military        | (- 2) | $\text{Vcc} \pm 10\%$ | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| Industrial      | (- 9) | $\text{Vcc} \pm 10\%$ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Commercial      | (- 5) | $\text{Vcc} \pm 10\%$ | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    |

**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM                    | UNIT |
|-----------|--------------------|---------|---------|----------------------------|------|
| Vcc       | Supply voltage     | 4.5     | 5.0     | 5.5                        | V    |
| Gnd       | Ground             | 0.0     | 0.0     | 0.0                        | V    |
| VIL (1)   | Input low voltage  | $-0.3$  | 0.0     | 0.8                        | V    |
| VIH       | Input high voltage | 2.2     | —       | $\text{Vcc} + 0.3\text{V}$ | V    |

Note : 1. VIL min =  $-0.3\text{ V}$  or  $-1.0\text{ V}$  pulse width 50 ns.

**CAPACITANCE**

| PARAMETER | DESCRIPTION        | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (2)   | Input capacitance  | —       | —       | 8       | pF   |
| Cout (2)  | Output capacitance | —       | —       | 10      | pF   |

Note : 2.  $\text{TA} = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ ,  $\text{Vcc} = 5.0\text{ V}$ , these parameters are not 100 % tested.

## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER | DESCRIPTION            | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|------------------------|---------|---------|---------|------|
| IIX (3)   | Input leakage current  | - 5.0   | -       | 5.0     | μA   |
| IOZ (3)   | Output leakage current | - 5.0   | -       | 5.0     | μA   |
| VOL (4)   | Output low voltage     | -       | -       | 0.4     | V    |
| VOH (4)   | Output high voltage    | 2.4     | -       | -       | V    |

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled specified to ± 10 μA for the HM 6116 2.  
4. Vcc min, IOL = 3.2 mA, IOH = - 1.0 mA.

### Consumption for Commercial specification (- 5) :

| SYMBOL     | PARAMETER                | 6116<br>-5 | 6116<br>L-5 | 6116<br>B-5 | UNIT | VALUE |
|------------|--------------------------|------------|-------------|-------------|------|-------|
| ICCSB (5)  | Standby supply current   | 3.0        | 2.0         | 2.0         | mA   | max   |
| ICCSB1 (6) | Standby supply current   | 2000.0     | 100.0       | 1.0         | μA   | max   |
| ICC (7)    | Operating supply current | 70.0       | 70.0        | 70.0        | mA   | max   |
| ICCOP (8)  | Operating supply current | 70.0       | 70.0        | 70.0        | mA   | max   |

### Consumption for Industrial specification (- 9) :

| SYMBOL     | PARAMETER                | 6116<br>-9 | 6116<br>L-9 | 6116<br>B-9 | UNIT | VALUE |
|------------|--------------------------|------------|-------------|-------------|------|-------|
| ICCSB (5)  | Standby supply current   | 4.5        | 4.0         | 4.0         | mA   | max   |
| ICCSB1 (6) | Standby supply current   | 2000.0     | 500.0       | 5.0         | μA   | max   |
| ICC (7)    | Operating supply current | 80.0       | 80.0        | 80.0        | mA   | max   |
| ICCOP (8)  | Operating supply current | 80.0       | 80.0        | 80.0        | mA   | max   |

### Consumption for Military specification (- 2) :

| SYMBOL     | PARAMETER                | 6116<br>-2 | 6116<br>L-2 | UNIT | VALUE |
|------------|--------------------------|------------|-------------|------|-------|
| ICCSB (5)  | Standby supply current   | 5.0        | 4.5         | mA   | max   |
| ICCSB1 (6) | Standby supply current   | 3000.0     | 1500.0      | μA   | max   |
| ICC (7)    | Operating supply current | 85.0       | 85.0        | mA   | max   |
| ICCOP (8)  | Operating supply current | 85.0       | 85.0        | mA   | max   |

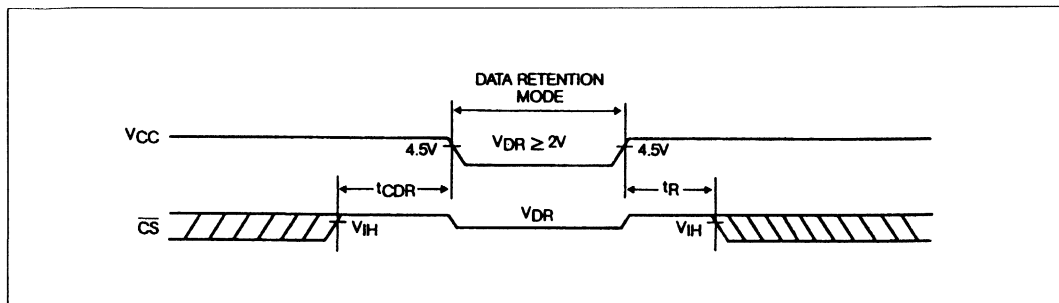
Notes : 5.  $\overline{CS} \leq V_{IH}$ .  
6.  $\overline{CS} \leq V_{cc} - 0.3 V$ , Iout = 0 mA.  
7.  $\overline{CS} \leq V_{IL}$ , Iout = 0 mA, Vin = Gnd/Vcc.  
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

**DATA RETENTION MODE**

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.

2. Output Enable ( $\overline{OE}$ ) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3.  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power up and power down transitions.

**TIMING****DATA RETENTION CHARACTERISTICS**

| PARAMETER   | DESCRIPTION                                  | MINIMUM    | TYPICAL<br>(9) | MAXIMUM | UNIT |
|-------------|----------------------------------------------|------------|----------------|---------|------|
| VCCDR       | V <sub>CC</sub> for data retention           | 2.0        | —              | —       | V    |
| TCDR        | Chip deselect to data retention on time      | 0.0        | —              | —       | ns   |
| TR          | Operation recovery time                      | TAVAV (10) | —              | —       | —    |
| ICCDR1 (11) | Data retention current @ 2.0 V : HM-6116B -5 | —          | 0.1            | 1.0     | μA   |
|             | HM-6116B -9                                  | —          | 0.1            | 5.0     | μA   |
|             | HM-6116L -5                                  | —          | 2.0            | 30.0    | μA   |
|             | HM-6116L -9                                  | —          | 2.0            | 200.0   | μA   |
|             | HM-6116L -2                                  | —          | 2.0            | 600.0   | μA   |
| ICCDR2 (11) | Data retention current @ 3.0 V : HM-6116B -5 | —          | 0.3            | 1.0     | μA   |
|             | HM-6116B -9                                  | —          | 0.3            | 7.0     | μA   |
|             | HM-6116L -5                                  | —          | 3.0            | 45.0    | μA   |
|             | HM-6116L -9                                  | —          | 3.0            | 300.0   | μA   |
|             | HM-6116L -2                                  | —          | 3.0            | 900.0   | μA   |

Notes : 9. TA = 25°C.

10. TAVAV = Read cycle time.

11.  $\overline{CS} = V_{CC}$ ,  $V_{in} = Gnd/V_{CC}$ , this parameter is only tested to  $V_{CC} = 2$  V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

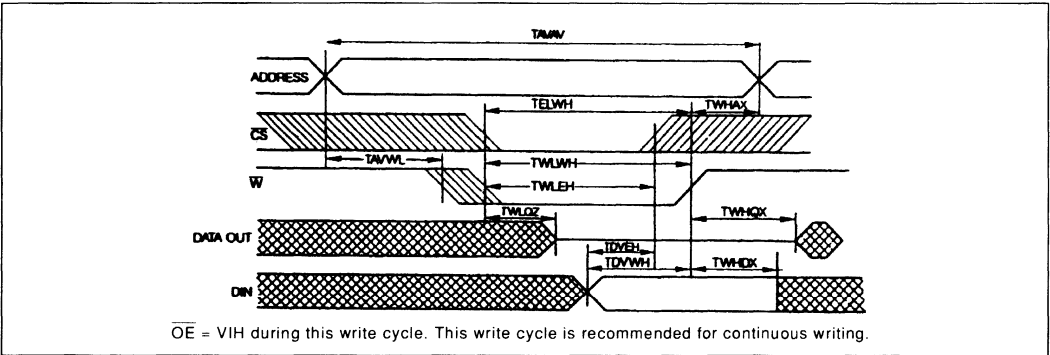
Input pulse levels : Gnd to 3.0 V  
Input rise : 10 ns  
Input timing reference levels : 1.5 V  
Output load : 1 TTL gate + 100 pF

WRITE CYCLE

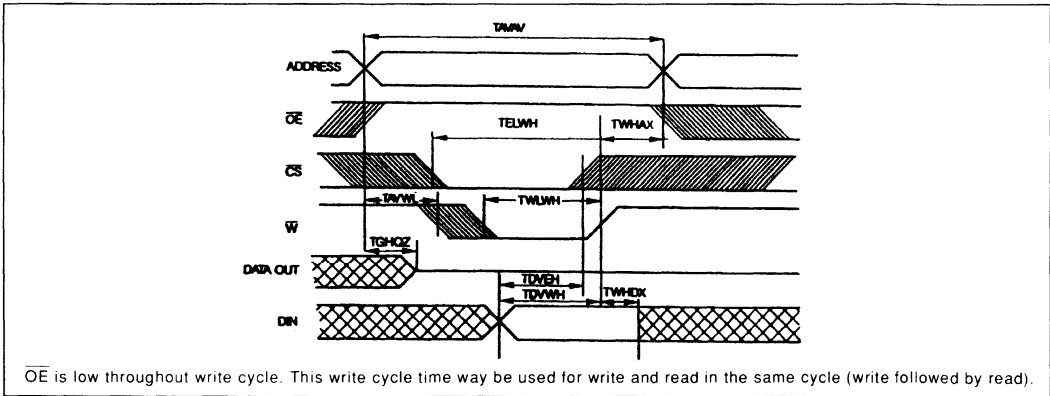
| SYMBOL     | PARAMETER                        | 6116<br>(B)(L) -5/ -9/ -2 | UNIT | VALUE |
|------------|----------------------------------|---------------------------|------|-------|
| TAVAV      | Write cycle time                 | 120                       | ns   | min   |
| TAVWL      | Address set-up time              | 0                         | ns   | min   |
| TAVWH      | Address valid to end of write    | 105                       | ns   | min   |
| TDVWH      | Data set-up time                 | 35                        | ns   | min   |
| TELWH      | $\overline{CS}$ low to write end | 70                        | ns   | min   |
| TWLQZ (12) | Write low to high Z              | 50                        | ns   | max   |
| TWLWH      | Write pulse width                | 70                        | ns   | min   |
| TWHAX      | Address hold to end of write     | 10                        | ns   | min   |
| TWHDX      | Data hold time                   | 10                        | ns   | min   |
| TWHQX (12) | Write high to low Z              | 5                         | ns   | min   |

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1



WRITE CYCLE 2

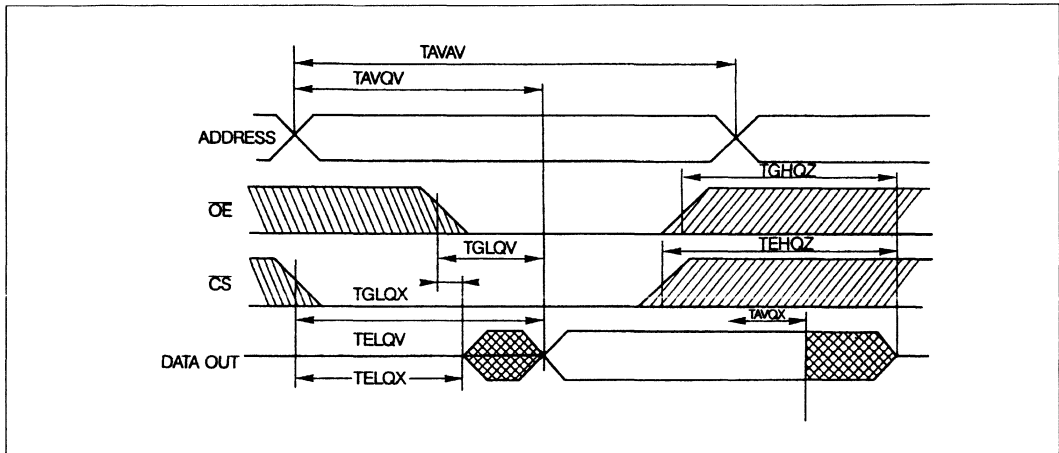




## READ CYCLE

| SYMBOL | PARAMETER                      | 6116<br>(B)(L) -5/ -9/ -2 | UNIT | VALUE |
|--------|--------------------------------|---------------------------|------|-------|
| TAVAV  | Write cycle time               | 120                       | ns   | min   |
| TAVQV  | Address access time            | 120                       | ns   | max   |
| TAVQX  | Address valid to low Z         | 10                        | ns   | min   |
| TELQV  | Chip-select access time        | 120                       | ns   | max   |
| TELQX  | $\overline{CS}$ low to low Z   | 10                        | ns   | min   |
| TEHQZ  | $\overline{CS}$ high to high Z | 40                        | ns   | max   |
| TGLQV  | Output Enable access time      | 80                        | ns   | max   |
| TGLQX  | $\overline{OE}$ low to low Z   | 10                        | ns   | min   |
| TGHQZ  | $\overline{OE}$ high to high Z | 40                        | ns   | max   |

## READ CYCLE

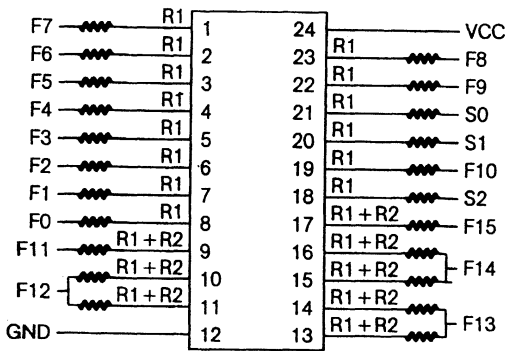


Note : W high for a read cycle.

## ORDERING INFORMATION

| Package                                                                        | Device Type                        |                                                                                       | Level                                                                                                                                                                |
|--------------------------------------------------------------------------------|------------------------------------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>HM1</u>                                                                     | <u>6116</u>                        | <u>L</u>                                                                              | <u>- 5</u>                                                                                                                                                           |
| 0 - Chip form<br>1 - Ceramic 24 pins<br>3 - Plastic 24 pins<br>4 - LCC 32 pins | 2 k x 8 general purpose static RAM | L = Low power<br>Blank = Standard<br>B = very Low Power<br>(only for - 5/- 9 version) | - 5 : Commercial<br>- 5+ : Commercial with B.I.<br>- 9 : Industrial<br>- 9+ : Industrial with B.I.<br>- 2 : Military<br>- 8 : Military with B.I.<br>(B.I. : Burn-in) |

## BURN-IN SCHEMATICS



$R1 = 220 \Omega$  per row or  $1 K\Omega$  per pin

$R2 = 2.2 K\Omega$  per driver

$Fo = 25 KHz \pm 20 \%$

$F_n = 1/2 F_{n-1}$

S0, S1, S2 : programmable signals for write / read cycles

VCC = 5.5 V

# SMART MEMORIES

10





## DATA SHEET

## HMC-6207

# CMOS DUAL-PORT RAM CONTROLLER

### FEATURES

- MANAGES RAM ACCESSES FROM TWO INDEPENDENT PROCESSORS
- RAM SIZE MAY BE 8 OR 16-BITS IRRESPECTIVE OF PROCESSORS
- DIRECT INTERFACING TO 80C86, 80C88 MICRO-PROCESSOR FAMILY
- PROCESSOR WORD SIZES MAY BE MIXED, 8 OR 16-BITS
- CONTROL OF ALL ADDRESS/DATA BUFFERS FOR BOTH PROCESSORS
- GENERATION OF SEPARATE ACKNOWLEDGE SIGNALS
- RAM BYPASS MODE OPTIMISED FOR USE WITH MULTIBUS SYSTEMS
- FABRICATED USING MHS HIGH-SPEED LOW-POWER CMOS TECHNOLOGY

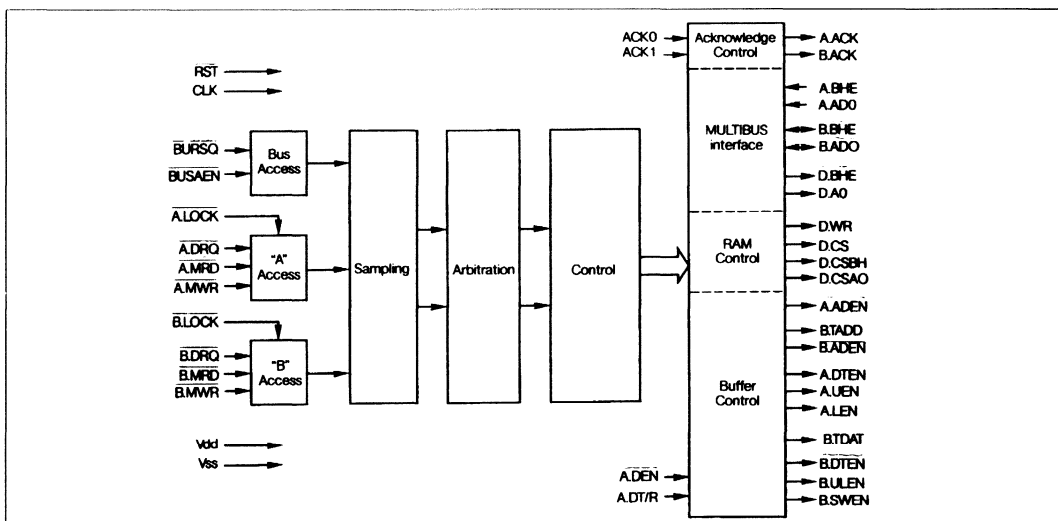
### DESCRIPTION

The Dual-Port RAM Controller from Matra-MHS Semiconductor allows the configuration of a block of memory shared between two independent processors.

The controller manages all accesses to this memory, carrying out both arbitration and priority assignment. Once an access is in progress, the controller generates

all signals for the address and data bus buffers and the RAM selection, according to the access type, either 8 or 16-bits. When the data becomes available the controller sends an acknowledge signal to processor to complete the access.

### FUNCTIONAL DIAGRAM



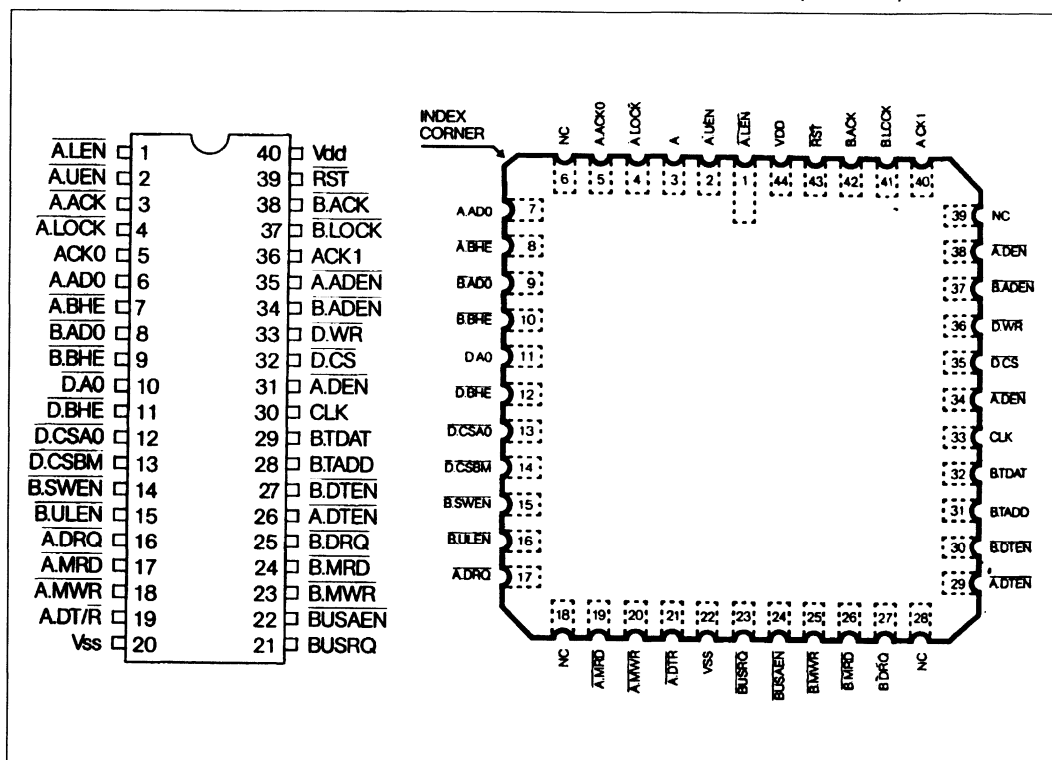
10

### LITERATURE

Data sheets and application notes (ref : AN1029) are available upon request. Contact your sales office or representative.

Pin out (top view)

PLCC (44 leads)



**DATA SHEET****HM 65231****2K x 8 CMOS  
DUAL PORT RAM****FEATURES**

- **HIGH SPEED, FAST ACCESS TIME :**  
COMMERCIAL : 80 ns max  
INDUSTRIAL : 100 ns max  
MILITARY : 120 ns max
- **STANDBY CURRENT : 3 mA**
- **OPERATING SUPPLY CURRENT : 60 mA max**
- **BATTERY BACK UP OPERATION :**  
2V DATA RETENTION
- **ONE SEPARATE ADDRESS/DATA PORT,  
ONE MULTIPLEXED ADDRESS/DATA PORT**
- **3 PROGRAMMABLE ARBITRATION MODES ON CHIP**
- **INT AND BUSY OUTPUTS**
- **FULLY STATIC OPERATION**
- **TTL COMPATIBLE INPUT/OUTPUT**
- **SINGLE 5V +/- 10 % POWER SUPPLY**

**DESCRIPTION**

The HM 65231 is a CMOS 2K x 8 high-speed Dual Port Static RAM. This state of the art technology used to fabricate it, combined with innovative circuit design techniques provides high speed access time together with excellent low power performance.

The HM 65231 provides two ports with controls, address and I/O. Port X is compatible with general purpose buses with separate address and data ; Port Y is directly compatible with a CPU providing multiplexed address and data. It is then possible to interconnect a CPU (type 8088 or 6809) or a microcontroller (type 8051) with a general purpose bus or a local bus without additional logic. Due to input buffers with gated inputs, the CE control pin permits the respective port to go into a standby mode when not selected (CE high).

Three programmable arbitration modes are available to resolve any contention with the maximum of efficiency.

This allows the interconnection of two buses using READY signals or a bus with a READY signal to a bus without wait state capability (8051-). In both cases, the access arbitration is totally software transparent.

The third mode is a general purpose mode based on a software controlled flag.

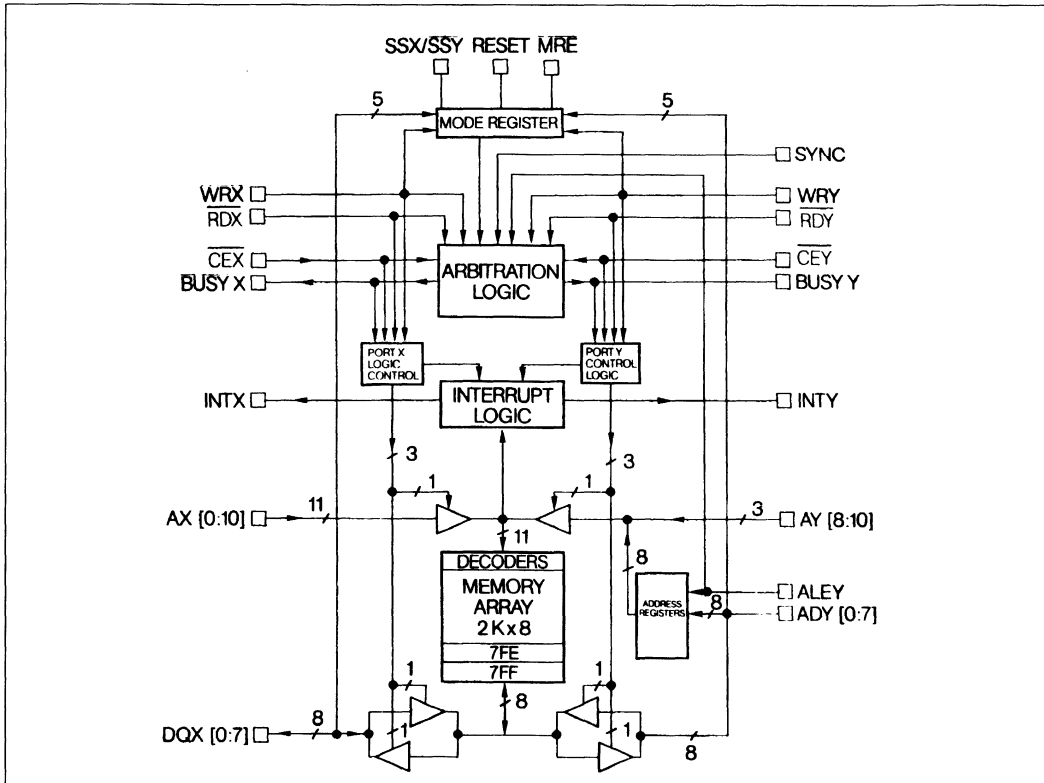
Depending upon the programmed mode, the memory locations 7FE and 7FF are defined as standard memory words or as two 8-bit flag registers. It is then possible to implement up to 16 concurrent communication channels with error free handshaking.

Two internal interrupt request flags are provided. Each flag is set or reset when memory locations 7FE or 7FF are accessed.

**10****LITERATURE**

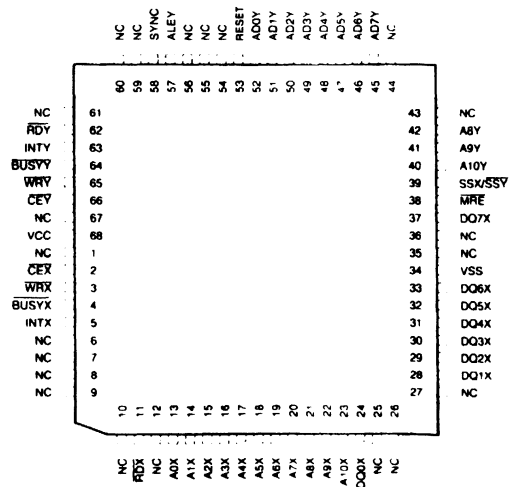
Data sheets, application notes (ref. : AN1033, AN1034) and user's manuals are available upon request. Contact your sales office or representative.

FUNCTIONAL DIAGRAM



Pinout

|       |    |    |         |
|-------|----|----|---------|
| CEX   | 1  | 48 | VCC     |
| WRX   | 2  | 47 | CEY     |
| BUSYX | 3  | 46 | WRY     |
| INTX  | 4  | 45 | BUSY Y  |
| RDX   | 5  | 44 | INTY    |
| A0X   | 6  | 43 | RDY     |
| A1X   | 7  | 42 | SYNC    |
| A2X   | 8  | 41 | ALEY    |
| A3X   | 9  | 40 | NC      |
| A4X   | 10 | 39 | RESET   |
| A5X   | 11 | 38 | AD0Y    |
| A6X   | 12 | 37 | AD1Y    |
| A7X   | 13 | 36 | AD2Y    |
| A8X   | 14 | 35 | AD3Y    |
| A9X   | 15 | 34 | AD4Y    |
| A10X  | 16 | 33 | AD5Y    |
| DQ0X  | 17 | 32 | AD6Y    |
| DQ1X  | 18 | 31 | AD7Y    |
| DQ2X  | 19 | 30 | A8Y     |
| DQ3X  | 20 | 29 | A9Y     |
| DQ4X  | 21 | 28 | A10Y    |
| DQ5X  | 22 | 27 | SSX/SSY |
| DQ6X  | 23 | 26 | MRE     |
| VSS   | 24 | 25 | DQ7X    |





ORDERING INFORMATION

| DEVICE TYPE |         |     | PACKAGE             | TEMPERATURE RANGE                      |
|-------------|---------|-----|---------------------|----------------------------------------|
| HM1         | - 65231 | - 2 | CERAMIC DIL         | - 55 °C to + 125 °C                    |
| HM1         | - 65231 | - 8 | CERAMIC DIL         | - 55 °C to + 125 °C                    |
| HM1         | - 65231 | - 9 | CERAMIC DIL         | - 40 °C to + 85 °C                     |
| HM3         | - 65231 | - 5 | PLASTIC DIL         | 0 °C to + 70 °C                        |
| HM3         | - 65231 | - 9 | PLASTIC DIL         | - 40 °C to + 85 °C                     |
| HMS         | - 65231 | - 5 | PLASTIC LCC 68 PINS | 0 °C to + 70 °C                        |
|             |         |     |                     | TEMPERATURE RANGE (- 2, - 5, - 8, - 9) |
|             |         |     |                     | DEVICE TITLE                           |
|             |         |     |                     | PACKAGE (1, 3, 4, S)                   |



**DATA SHEET****M 67132/M 67142**

# 2 K x 8 CMOS DUAL PORT RAM

**FEATURES**

- **FAST ACCESS TIME :**
  - **MILITARY** : 35 TO 55 ns (max)
  - **COMMERCIAL** : 25 TO 55 ns (max)
- **VERY LOW POWER CONSUMPTION :**
  - **ACTIVE** : 500 mW (typ)
  - **STANDBY** : 10  $\mu$ W (typ)
  - **DATA-RETENTION** : 5  $\mu$ W (typ)
- **EXPANDABLE DATA BUS TO 16 BITS OR MORE USING MASTER/SLAVE DEVICES WHEN USING MORE THAN ONE DEVICE**
- **ON CHIP ARBITRATION LOGIC**
- **BUS $\overline{Y}$  OUTPUT FLAG ON MASTER**
- **BUS $\overline{Y}$  INPUT FLAG ON SLAVE**
- **FULLY ASYNCHRONOUS OPERATION FROM EITHER PORT**
- **BATTERY BACKUP OPERATION : 2 V DATA RETENTION**
- **TTL COMPATIBLE**
- **SINGLE 5 V  $\pm$  10 % POWER SUPPLY**

**DESCRIPTION**

The M 67132/67142 are very low power CMOS dual port static RAM organised as 2048 x 8. They are designed to be used as a stand-alone 8 bit dual port RAM or as a combination MASTER/SLAVE dual port for 16 bit or more width systems. The MATRA-MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need additional discrete logic.

Master and slave devices provide two independant ports with separate control, address and I/O pins that permit independant, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by CS permits the on-

chip circuitry of each port in order to enter a very low stand by power mode.

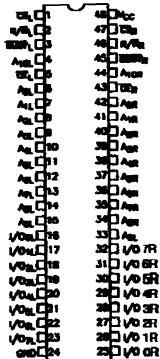
Using an array of eight transistors (8 T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67132/42 combine an extremely low standby supply current (typ = 1.0  $\mu$ A) with a fast access time at 25 ns over the full commercial temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5  $\mu$ W.

The M 67132/42 are processed following the test methods of MIL STD 883C level B.

**10**

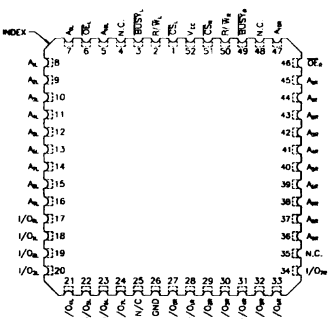
PACKAGES

DIP (top view)



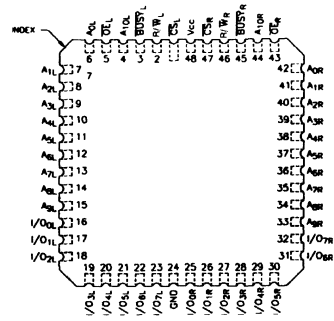
Plastic and Ceramic 600 mils,  
48 pins DIL

52-PIN LCC/PLCC (top view)

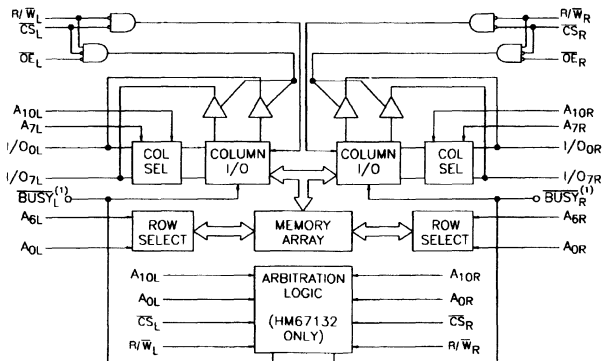


LCC, CQFPJ and PQFP 48 pins  
PLCC and LCC 52 pins

48-PIN LCC/CQFPJ (top view)  
PQFP



BLOCK DIAGRAM



Notes : HM 67132 (MASTER) : BUSY is open drain output and requires pullup resistor.  
HM 67142 (SLAVE) : BUSY in input.

PIN NAMES

| LEFT PORT           | RIGHT PORT          | NAMES             |
|---------------------|---------------------|-------------------|
| $\overline{CS}_L$   | $\overline{CS}_R$   | Chip Select       |
| $R/\overline{W}_L$  | $R/\overline{W}_R$  | Write Enable      |
| $\overline{OE}_L$   | $\overline{OE}_R$   | Output Enable     |
| $A_{0L} - 10L$      | $A_{0R} - 10R$      | Address           |
| $I/O_{0L} - 7L$     | $I/O_{0R} - 7R$     | Data Input/Output |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag         |
| $V_{DD}$            |                     | Power             |
| GND                 |                     | Ground            |



## TRUTH TABLE

TABLE I - NON CONTENTION READ/WRITE CONTROL <sup>(4)</sup>

| LEFT OR RIGHT PORT <sup>(1)</sup> |    |    |                     | FUNCTION                                                                    |
|-----------------------------------|----|----|---------------------|-----------------------------------------------------------------------------|
| R/W                               | CS | OE | D0-7                |                                                                             |
| X                                 | H  | X  | Z                   | Port Disabled and in Power Down Mode. ICCSB2 or ICCSB4                      |
| X                                 | H  | X  | Z                   | $\overline{CS_R} = \overline{CS_L} = H$ . Power Down Mode. ICCSB1 or ICCSB3 |
| L                                 | L  | X  | DATA <sub>IN</sub>  | Data on Port Written into memory <sup>(2)</sup>                             |
| H                                 | L  | L  | DATA <sub>OUT</sub> | Data in Memory Output on Port <sup>(3)</sup>                                |
| H                                 | L  | H  | Z                   | High Impedance Outputs                                                      |

- Notes : 1.  $A_{0L} - A_{10L} \neq A_0 - A_{10R}$   
 2. If  $BUSY = L$ , data is not written.  
 3. If  $BUSY = L$ , data may not be valid, see  $t_{WDD}$  and  $t_{MDD}$  timing  
 4. H = HIGH, L = LOW, X = DON'T CARE,  
 Z = HIGH IMPEDANCE

TABLE III - ARBITRATION <sup>(2)</sup>

| LEFT PORT                                                             |                                     | RIGHT PORT        |                                     | FLAGE(1)            |                     | FUNCTION             |
|-----------------------------------------------------------------------|-------------------------------------|-------------------|-------------------------------------|---------------------|---------------------|----------------------|
| $\overline{CS_L}$                                                     | A <sub>0L</sub> -A <sub>10L</sub>   | $\overline{CS_R}$ | A <sub>0L</sub> -A <sub>10R</sub>   | $\overline{BUSY_L}$ | $\overline{BUSY_R}$ |                      |
| H                                                                     | X                                   | H                 | X                                   | H                   | H                   | No Contention        |
| L                                                                     | Any                                 | H                 | X                                   | H                   | H                   | No Contention        |
| H                                                                     | X                                   | L                 | Any                                 | H                   | H                   | No Contention        |
| L                                                                     | $\neq A_{0R}-A_{10R}$               | L                 | $\neq A_{0L}-A_{10L}$               | H                   | H                   | No Contention        |
| ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH     |                                     |                   |                                     |                     |                     |                      |
| L                                                                     | LV5R                                | L                 | LV5R                                | H                   | L                   | L-Port Wins          |
| L                                                                     | RV5L                                | L                 | RV5L                                | L                   | H                   | R-Port Wins          |
| L                                                                     | Same                                | L                 | Same                                | H                   | L                   | Arbitration Resolved |
| L                                                                     | Same                                | L                 | Same                                | L                   | H                   | Arbitration Resolved |
| $\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$ |                                     |                   |                                     |                     |                     |                      |
| LL5R                                                                  | = A <sub>0R</sub> -A <sub>10R</sub> | LL5R              | = A <sub>0L</sub> -A <sub>10L</sub> | H                   | L                   | L-Port Wins          |
| RL5L                                                                  | = A <sub>0R</sub> -A <sub>10R</sub> | RL5L              | = A <sub>0L</sub> -A <sub>10L</sub> | L                   | H                   | R-Port Wins          |
| LW5R                                                                  | = A <sub>0R</sub> -A <sub>10R</sub> | LW5R              | = A <sub>0L</sub> -A <sub>10L</sub> | H                   | L                   | Arbitration Resolved |
| LW5R                                                                  | = A <sub>0R</sub> -A <sub>10R</sub> | LW5R              | = A <sub>0L</sub> -A <sub>10L</sub> | L                   | H                   | Arbitration Resolved |

- Notes : 1.  $\overline{INT}$  Flags Don't Care.  
 2. X = DON'T CARE, L = LOW, H = HIGH  
 LV5R = Left Address Valid  $\geq 5$  ns before right address.  
 RV5L = Right Address Valid  $\geq 5$  ns before left address.  
 Same = Left and Right Addresses match within 5 ns of each other.  
 LL5R = Left  $\overline{CS}$  - LOW  $\geq 5$  ns before Right  $\overline{CS}$   
 RL5L = Right  $\overline{CS}$  - LOW  $\geq 5$  ns before Left  $\overline{CS}$   
 LW5R = Left and Right  $\overline{CS}$  = LOW within 5 ns of each other.

10

SELECTION GUIDE

|               |                           |            | M67132<br>M67142<br>(25 ns) | M67132<br>M67142<br>(35 ns) | M67132<br>M67142<br>(45 ns) | M67132<br>M67142<br>(55 ns) |
|---------------|---------------------------|------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| ICCOP1<br>(1) | Full Operating<br>Current | MIL<br>COM | -<br>120 mA                 | 150 mA<br>120 mA            | 150 mA<br>120 mA            | 150 mA<br>120 mA            |
| ICCSB1<br>(2) | Standby<br>Current        | MIL<br>COM | -<br>5 mA                   | 10 mA<br>5 mA               | 10 mA<br>5 mA               | 10 mA<br>5 mA               |
| ICCSB2<br>(3) | Standby<br>Current        | MIL<br>COM | -<br>85 mA                  | 110 mA<br>85 mA             | 110 mA<br>85 mA             | 110 mA<br>85 mA             |
| ICCSB3<br>(4) | Full Standby<br>Current   | MIL<br>COM | -<br>10 µA                  | 50 µA<br>10 µA              | 50 µA<br>10 µA              | 50 µA<br>10 µA              |
| ICCSB4<br>(5) | Full Standby<br>Current   | MIL<br>COM | -<br>80 mA                  | 100 mA<br>80 mA             | 100 mA<br>80 mA             | 100 mA<br>80 mA             |
| ICCCR<br>(6)  | Data Retention<br>Current | MIL<br>COM | -<br>5 µA                   | 20 µA<br>5 µA               | 20 µA<br>5 µA               | 20 µA<br>5 µA               |

ALL VALUES ARE MAXIMUM OVER THE FULL TEMPERATURE RANGE

- Notes :
- Both ports active - Maximum frequency - Outputs open.
  - Both ports TTL level inputs ( $\overline{CS}$  L and R  $\geq 2.2$  V).
  - One port active ( $f = \max$ ), outputs open - One port Standby TTL level input ( $\overline{CS}$  L or R  $\geq 2.2$  V).
  - Both ports CMOS level inputs ( $\overline{CS}$  L and R  $\geq V_{cc} - 0.2$  V).
  - One port active ( $f = \max$ ), outputs open - One port standby CMOS level input ( $\overline{CS}$  L or R  $\geq V_{cc} - 0.2$  V).
  - Data retention mode :  $V_{cc} = 2$  V, ( $\overline{CS}$  L and R =  $V_{cc}$ ).

ORDERING INFORMATION

| Temperature range                                | Packages                                                                                                                                                                        | Device Type                                                                                              | Access Time (ns)                 |
|--------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------------------|
| C                                                | Mn                                                                                                                                                                              | 671NN                                                                                                    | 25                               |
| C = COMMERCIAL<br>I = INDUSTRIAL<br>M = MILITARY | 1 = Ceramic 48 pins<br>DIL 600 mils<br>3 = Plastic 48 pins<br>DIL 600 mils<br>4 K = LCC 48 pins<br>4 = LCC 52 pins<br>F = PQFP 48 pins<br>Q = CQFPJ 48 pins<br>S = PLCC 68 pins | 67132 = 16 K (2 K x 8) MASTER<br>CMOS DUAL PORT RAM<br>67142 = 16 K (2K x 8) SLAVE CMOS<br>DUAL PORT RAM | 25 ns<br>35 ns<br>45 ns<br>55 ns |

**DATA SHEET****M 67133/M 67143**

## 2 K x 16 CMOS DUAL PORT RAM

**FEATURES**

- **FAST ACCESS TIME :**
  - MILITARY : 35 TO 55 ns (max)
  - COMMERCIAL : 25 TO 55 ns (max)
- **VERY LOW POWER CONSUMPTION :**
  - ACTIVE : 500 mW (typ)
  - STANDBY : 10  $\mu$ W (typ)
  - DATA-RETENTION : 5  $\mu$ W (typ)
- **EXPANDABLE DATA BUS TO 32 BITS OR MORE USING MASTER/SLAVE DEVICES WHEN USING MORE THAN ONE DEVICE**
- **ON CHIP ARBITRATION LOGIC**
- **BUSY OUTPUT FLAG ON MASTER**
- **BUSY INPUT FLAG ON SLAVE**
- **VERSATILE CONTROL FOR WRITE SEPARATE WRITE CONTROL FOR LOWER AND UPPER BYTE OF EACH PORT**
- **FULLY ASYNCHRONOUS OPERATION FROM EITHER PORT**
- **BATTERY BACK-UP OPERATION : 2 V DATA RETENTION**
- **TTL COMPATIBLE**
- **SINGLE 5 V  $\pm$  10 % POWER SUPPLY**

**DESCRIPTION**

The M 67133/67143 are very low power CMOS dual port static RAM organised as 2048 x 16. They are designed to be used as a stand-alone 16 bit dual port RAM or as a combination MASTER/SLAVE dual port for 32 bit or more width systems. The MATRA-MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need additional discrete logic.

Master and slave devices provide two independant ports with separate control, address and I/O pins that permit independant, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by  $\overline{CS}$  permits the on-

chip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8 T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67133/43 combine an extremely low standby supply current (typ = 1.0  $\mu$ A) with a fast access time at 25 ns over the full commercial temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5  $\mu$ W.

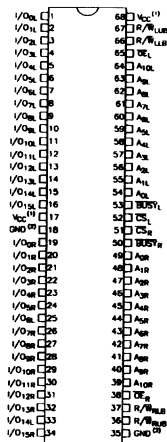
The M 67133/43 are processed following the test methods of MIL STD 883C level B.

**10**

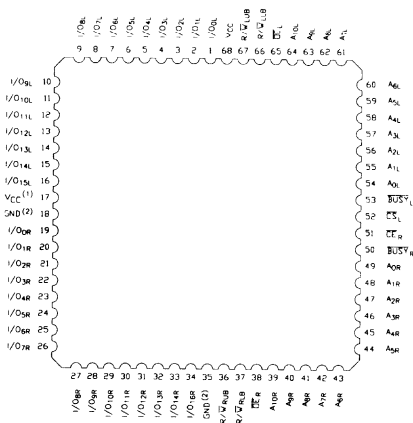
PACKAGES

Ceramic 68 pins, DIL 600 mils  
PLCC, LCC and PGA 68 pins.

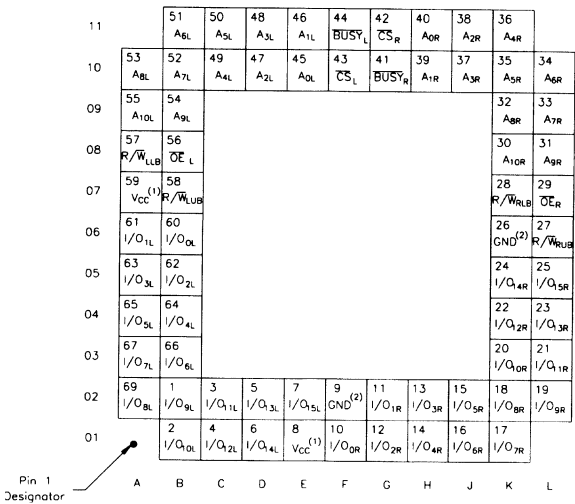
DIP (top view)



LCC/PLCC (top view)

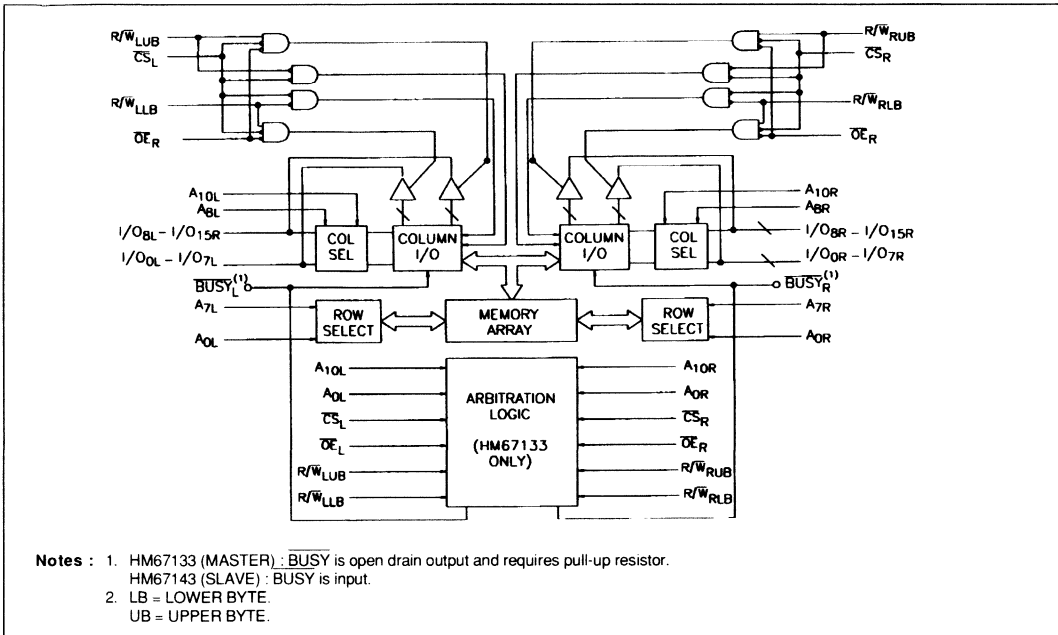


PGA (top view) (Ceramic or Plastic)





### BLOCK DIAGRAM



## PIN NAMES

| LEFT PORT                                                                                   | RIGHT PORT                                                                                  | NAMES         |
|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------|
| $\overline{\text{CS}}_{\text{L}}$                                                           | $\overline{\text{CS}}_{\text{R}}$                                                           | Chip Select   |
| $\text{R}/\overline{\text{W}}_{\text{LUB}},$<br>$\text{R}/\overline{\text{W}}_{\text{LLB}}$ | $\text{R}/\overline{\text{W}}_{\text{RUB}},$<br>$\text{R}/\overline{\text{W}}_{\text{RLB}}$ | Write Enable  |
| $\overline{\text{OE}}_{\text{L}}$                                                           | $\overline{\text{OE}}_{\text{R}}$                                                           | Output Enable |
| $\text{A}_{0\text{L}} - 10\text{L}$                                                         | $\text{A}_{0\text{R}} - 10\text{R}$                                                         | Addresses     |
| $\text{I}/\text{O}_{0\text{L}} - 15\text{L}$                                                | $\text{I}/\text{O}_{0\text{R}} - 15\text{R}$                                                | Input/Output  |
| $\text{BUSY}_{\text{L}}$                                                                    | $\text{BUSY}_{\text{R}}$                                                                    | Busy Flag     |
| $\text{V}_{\text{CC}}$                                                                      |                                                                                             | Power Supply  |
| $\text{GND}$                                                                                |                                                                                             | Ground        |

## TRUTH TABLE

TABLE I - NON CONTENTION READ/WRITE CONTROL <sup>(4)</sup>

| LEFT OR RIGHT PORT |                   |    |    |                     |                     | FUNCTION                                                                                                     |
|--------------------|-------------------|----|----|---------------------|---------------------|--------------------------------------------------------------------------------------------------------------|
| R/W <sub>LB</sub>  | R/W <sub>UB</sub> | CS | OE | I/O <sub>0-7</sub>  | I/O <sub>8-15</sub> |                                                                                                              |
| X                  | X                 | H  | X  | Z                   | Z                   | Port Disabled and in Power Down Mode. ICCSB2 or ICCSB4                                                       |
| X                  | X                 | H  | X  | Z                   | Z                   | $\overline{CS}_R = \overline{CS}_L = H$ . Power Down Mode. ICCSB1 or ICCSB3                                  |
| L                  | L                 | L  | X  | DATA <sub>IN</sub>  | DATA <sub>IN</sub>  | Data on Lower Byte and Upper Byte Written Into Memory <sup>(2)</sup>                                         |
| L                  | H                 | L  | L  | DATA <sub>IN</sub>  | DATA <sub>OUT</sub> | Data on Lower Byte Written into Memory <sup>(2)</sup> , Data in Memory Output on Upper Byte <sup>(3)</sup> . |
| H                  | L                 | L  | L  | DATA <sub>OUT</sub> | DATA <sub>IN</sub>  | Data in Memory Output on Lower Byte <sup>(3)</sup> . Data on Upper Byte Written into Memory <sup>(2)</sup> . |
| L                  | H                 | L  | H  | DATA <sub>IN</sub>  | Z                   | Data on Lower Byte Written into Memory <sup>(2)</sup> .                                                      |
| H                  | L                 | L  | H  | Z                   | DATA <sub>IN</sub>  | Data on Upper Byte Written into Memory <sup>(2)</sup> .                                                      |
| H                  | H                 | L  | L  | DATA <sub>OUT</sub> | DATA <sub>OUT</sub> | Data in Memory Output on Lower Byte and Upper Byte <sup>(3)</sup> .                                          |
| H                  | H                 | L  | H  | Z                   | Z                   | High Impedance Outputs.                                                                                      |

- Notes :**
1.  $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
  2. If  $BUSY = L$ , data is not written.
  3. If  $BUSY = L$ , data may not be valid, see  $t_{WDO}$  and  $t_{DOD}$  timing.
  4. H = High, L = Low, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Byte.

TABLE II - ARBITRATION

| LEFT PORT                                                                                          |                                     | RIGHT PORT        |                                     | FLAGS <sup>(1)</sup> |                     | FUNCTION             |
|----------------------------------------------------------------------------------------------------|-------------------------------------|-------------------|-------------------------------------|----------------------|---------------------|----------------------|
| $\overline{CS}_L$                                                                                  | A <sub>0L</sub> -A <sub>10L</sub>   | $\overline{CS}_R$ | A <sub>0R</sub> -A <sub>10R</sub>   | $\overline{BUSY}_L$  | $\overline{BUSY}_R$ |                      |
| H                                                                                                  | X                                   | H                 | X                                   | H                    | H                   | No Contention        |
| L                                                                                                  | Any                                 | H                 | X                                   | H                    | H                   | No Contention        |
| H                                                                                                  | X                                   | L                 | Any                                 | H                    | H                   | No Contention        |
| L                                                                                                  | $\neq A_{0R}-A_{10R}$               | L                 | $\neq A_{0L}-A_{10L}$               | H                    | H                   | No Contention        |
| <b>ADDRESS ARBITRATION WITH <math>\overline{CE}</math> LOW BEFORE ADDRESS MATCH</b>                |                                     |                   |                                     |                      |                     |                      |
| L                                                                                                  | LV5R                                | L                 | LV5R                                | H                    | L                   | L-Port Wins          |
| L                                                                                                  | RV5L                                | L                 | RV5L                                | L                    | H                   | R-Port Wins          |
| L                                                                                                  | Same                                | L                 | Same                                | H                    | L                   | Arbitration Resolved |
| L                                                                                                  | Same                                | L                 | Same                                | L                    | H                   | Arbitration Resolved |
| <b><math>\overline{CE}</math> ARBITRATION WITH ADDRESS MATCH BEFORE <math>\overline{CE}</math></b> |                                     |                   |                                     |                      |                     |                      |
| LL5R                                                                                               | = A <sub>0R</sub> -A <sub>10R</sub> | LL5R              | = A <sub>0L</sub> -A <sub>10L</sub> | H                    | L                   | L-Port Wins          |
| RL5L                                                                                               | = A <sub>0R</sub> -A <sub>10R</sub> | RL5L              | = A <sub>0L</sub> -A <sub>10L</sub> | L                    | H                   | R-Port Wins          |
| LW5R                                                                                               | = A <sub>0R</sub> -A <sub>10R</sub> | LW5R              | = A <sub>0L</sub> -A <sub>10L</sub> | H                    | L                   | Arbitration Resolved |
| LW5R                                                                                               | = A <sub>0R</sub> -A <sub>10R</sub> | LW5R              | = A <sub>0L</sub> -A <sub>10L</sub> | L                    | H                   | Arbitration Resolved |

- Note :**
1. X = Don't Care, L = Low, H = High.  
LV5R = Left Address Valid  $\geq 5$  ns before right address.  
RV5L = Right address Valid  $\geq 5$  ns before left address.  
Same = Left and Right address match within 5 ns of each other.  
LL5R = Left CS = LOW  $\geq 5$  ns before Right CS.  
RL5L = Right CS = LOW  $\geq 5$  ns before Left CS.  
LW5R = Left and Right CS = LOW within 5 ns of each other.

SELECTION GUIDE

|               |                           |            | M67133<br>M67143<br>(25 ns) | M67133<br>M67143<br>(35 ns) | M67133<br>M67143<br>(45 ns) | M67133<br>M67143<br>(55 ns) |
|---------------|---------------------------|------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| ICCOP1<br>(1) | Full Operating<br>Current | MIL<br>COM | -<br>150 mA                 | 180 mA<br>150 mA            | 180 mA<br>150 mA            | 180 mA<br>150 mA            |
| ICCSB1<br>(2) | Standby<br>Current        | MIL<br>COM | -<br>5 mA                   | 10 mA<br>5 mA               | 10 mA<br>5 mA               | 10 mA<br>5 mA               |
| ICCSB2<br>(3) | Standby<br>Current        | MIL<br>COM | -<br>110 mA                 | 130 mA<br>110 mA            | 130 mA<br>110 mA            | 130 mA<br>110 mA            |
| ICCSB3<br>(4) | Full Standby<br>Current   | MIL<br>COM | -<br>10 µA                  | 50 µA<br>10 µA              | 50 µA<br>10 µA              | 50 µA<br>10 µA              |
| ICCSB4<br>(5) | Full Standby<br>Current   | MIL<br>COM | -<br>100 mA                 | 120 mA<br>100 mA            | 120 mA<br>100 mA            | 120 mA<br>100 mA            |
| ICCDR<br>(6)  | Data Retention<br>Current | MIL<br>COM | -<br>5 µA                   | 20 µA<br>5 µA               | 20 µA<br>5 µA               | 20 µA<br>5 µA               |

ALL VALUES ARE MAXIMUM OVER THE FULL TEMPERATURE RANGE.

- Notes :
- 1. Both ports active - Maximum frequency - Outputs open.
  - 2. Both ports TTL level inputs (CS L and R  $\geq 2.2$  V).
  - 3. One port active (f = max), outputs open - One port Standby TTL level input ( $\overline{\text{CS}}$  L or R  $\geq 2.2$  V).
  - 4. Both ports CMOS level inputs (CS L and R  $\geq V_{CC} - 0.2$  V).
  - 5. One port active (f = max), outputs open - One port Standby CMOS level input ( $\overline{\text{CS}}$  L or R  $\geq -2.2$  V).
  - 6. Data retention mode :  $V_{CC} = 2$  V; (CS L and R =  $V_{CC}$ ).

ORDERING INFORMATION

| Temperature range | Packages            | Device Type               | Access Time (ns) |
|-------------------|---------------------|---------------------------|------------------|
| C                 | Mn                  | 671NN                     | 25               |
| C = COMMERCIAL    |                     | 67133 = 32K (2 K x 16)    |                  |
| I = INDUSTRIAL    |                     | MASTER CMOS DUAL PORT RAM |                  |
| M = MILITARY      |                     | 67143 = 32K (2 K x 16)    |                  |
|                   |                     | SLAVE CMOS DUAL PORT RAM  |                  |
|                   | 1 = Ceramic 68 pins |                           | 25 ns            |
|                   | DIL 600 mils        |                           | 35 ns            |
|                   | 4 = LCC 68 pins     |                           | 45 ns            |
|                   | G = PGA 68 pins     |                           | 55 ns            |
|                   | S = PLCC 68 pins    |                           |                  |



## DATA SHEET

## M 67005

# 8 K x 8 CMOS DUAL PORT RAM

## FEATURES

- FAST ACCESS TIME :
  - MILITARY : 35 TO 55 ns (max)
  - COMMERCIAL : 25 TO 55 ns (max)
- VERY LOW POWER CONSUMPTION :
  - ACTIVE : 500 mW (typ)
  - STANDBY : 10  $\mu$ W (typ)
  - DATA-RETENTION : 5  $\mu$ W (typ)
- EXPANDABLE DATA BUS TO 16 BITS OR MORE USING MASTER/SLAVE CHIP SELECT WHEN USING MORE THAN ONE DEVICE
- ON CHIP ARBITRATION LOGIC
- VERSATIBLE PIN SELECT FOR MASTER OR SLAVE :
  - $\overline{M/\overline{S}}$  = H FOR  $\overline{BUSY}$  OUTPUT FLAG ON MASTER
  - $\overline{M/\overline{S}}$  = L FOR  $\overline{BUSY}$  INPUT FLAG ON SLAVE
- INT FLAG FOR PORT TO PORT COMMUNICATION
- FULL HARDWARE SUPPORT OF SEMAPHORE SIGNALING BETWEEN PORTS
- FULLY ASYNCHRONOUS OPERATION FROM EITHER PORT
- BATTERY BACKUP OPERATION : 2 V DATA RETENTION
- TTL COMPATIBLE
- SINGLE 5 V  $\pm$  10 % POWER SUPPLY

## DESCRIPTION

The M 67005 is a very low power CMOS dual port static RAM organised as 8192 x 8. The M 67005 is designed to be used as a stand-alone 8 bit dual port RAM or as a combination MASTER/SLAVE dual port for 16 or more width systems. The MATRA MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need an additional discrete logic.

Master and slave devices provide two independant ports with separate control, address and I/O pins that permit independant, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by CS permits the on-

chip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8 T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67005 combines an extremely low standby supply current (typ = 1.0  $\mu$ A) with a fast access time at 25 ns over the full commercial temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5  $\mu$ W.

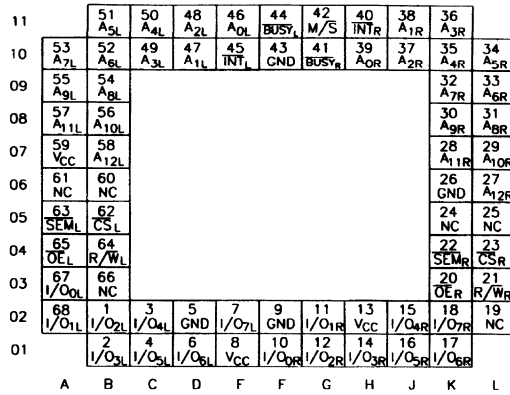
The M 67005 is processed following the test methods of MIL STD 883C level B.

10

## PACKAGES

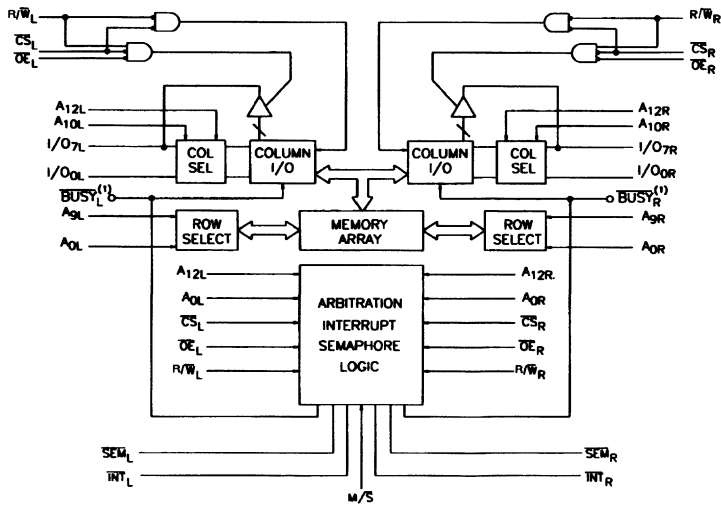
PLCC, LCC and PGA 68 pins.

**68-PIN PGA (top view)**



- Notes :**
1. All  $V_{CC}$  pins have to be connected to power supply.
  2. All GND pins have to be connected to ground supply.

### BLOCK DIAGRAM



- Notes :** 1. (MASTER) : BUSY is output.  
(SLAVE) : BUSY is input.

## PIN NAMES

| LEFT PORT           | RIGHT PORT          | NAMES                  |
|---------------------|---------------------|------------------------|
| $\overline{CS}_L$   | $\overline{CS}_R$   | Chip Select            |
| $R/\overline{W}_L$  | $R/\overline{W}_R$  | Write Enable           |
| $\overline{OE}_L$   | $\overline{OE}_R$   | Output Enable          |
| $A_{0L} - 12L$      | $A_{0R} - 12R$      | Address                |
| $I/O_{0L} - 7L$     | $I/O_{0R} - 7R$     | Data Input/Output      |
| $\overline{SEM}_L$  | $\overline{SEM}_R$  | Semaphore Enable       |
| $\overline{INT}_L$  | $\overline{INT}_R$  | Interrupt Flag         |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag              |
| $M/\overline{S}$    |                     | Master or Slave Select |
| $V_{CC}$            |                     | Power Supply           |
| $GND$               |                     | Ground                 |

## TRUTH TABLE

Table 1 : NON-CONTENTION READ/WRITE CONTROL

| INPUTS <sup>(1)</sup> |                                                                                     |                 |                  | OUTPUTS       | MODE                        |
|-----------------------|-------------------------------------------------------------------------------------|-----------------|------------------|---------------|-----------------------------|
| $\overline{CS}$       | $R/\overline{W}$                                                                    | $\overline{OE}$ | $\overline{SEM}$ | $I/O_1-I/O_7$ |                             |
| H                     | X                                                                                   | X               | H                | Hi-Z          | Deselected Power Down       |
| H                     | H                                                                                   | L               | L                | $DATA_{OUT}$  | Read Data In Sema. Flag     |
| X                     | X                                                                                   | H               | X                | Hi-Z          | Outputs Disabled            |
| H                     |  | X               | L                | $DATA_{IN}$   | Write D IN0 Into Sema. Flag |
| L                     | H                                                                                   | L               | H                | $DATA_{OUT}$  | Read Memory                 |
| L                     | L                                                                                   | X               | H                | $DATA_{IN}$   | Write to Memory             |
| L                     | X                                                                                   | X               | L                | -             | Not Allowed                 |

Note : 1.  $A_{0L} = A_{12L} \neq A_{0R} - A_{12R}$

Table 2 : ARBITRATION OPTIONS

| OPTIONS           | INPUTS          |                  |                  | OUTPUTS           |                  |
|-------------------|-----------------|------------------|------------------|-------------------|------------------|
|                   | $\overline{CS}$ | $M/\overline{S}$ | $\overline{SEM}$ | $\overline{BUSY}$ | $\overline{INT}$ |
| Busy Logic Master | L               | H                | H                | Output Signal     | -                |
| Busy Logic Slave  | L               | L                | H                | Input Signal      | -                |
| Interrupt Logic   | L               | X                | H                | -                 | Output Signal    |
| Semaphore Logic*  | H               | H                | L                | H                 | -                |
|                   | H               | L                | L                | Hi-Z              | -                |

\* Inputs Signals are for Semaphore Flags set and test (Write and Read) operations.

## SELECTION GUIDE

|               |                           |            | M67005<br>(25 ns) | M67005<br>(35 ns)        | M67005<br>(45 ns)        | M67005<br>(55 ns)        |
|---------------|---------------------------|------------|-------------------|--------------------------|--------------------------|--------------------------|
| ICCOP1<br>(1) | Full Operating<br>Current | MIL<br>COM | -<br>200 mA       | 200 mA<br>200 mA         | 200 mA<br>200 mA         | 200 mA<br>200 mA         |
| ICCOP2<br>(2) | Operating<br>Current      | MIL<br>COM | -<br>100 mA       | 100 mA<br>100 mA         | 100 mA<br>100 mA         | 100 mA<br>100 mA         |
| ICCSB<br>(3)  | Standby<br>Current        | MIL<br>COM | -<br>5 mA         | 10 mA<br>5 mA            | 10 mA<br>5 mA            | 10 mA<br>5 mA            |
| ICCSB1<br>(4) | Full Standby<br>Current   | MIL<br>COM | -<br>10 $\mu$ A   | 50 $\mu$ A<br>10 $\mu$ A | 50 $\mu$ A<br>10 $\mu$ A | 50 $\mu$ A<br>10 $\mu$ A |
| ICCDR<br>(4)  | Data Retention<br>Current | MIL<br>COM | -<br>5 $\mu$ A    | 20 $\mu$ A<br>5 $\mu$ A  | 20 $\mu$ A<br>5 $\mu$ A  | 20 $\mu$ A<br>5 $\mu$ A  |

**Notes :** 1. Both ports active - Maximum frequency - Outputs open.  
2. One port active - One port standby - Outputs open.  
3. Both ports TTL level inputs.  
4. Both ports CMOS level inputs.

## ORDERING INFORMATION

| Temperature range                                | Packages                                               | Device Type                                  | Access Time (ns)                 |
|--------------------------------------------------|--------------------------------------------------------|----------------------------------------------|----------------------------------|
| C                                                | Mn                                                     | 67005                                        | 25                               |
| C = COMMERCIAL<br>I = INDUSTRIAL<br>M = MILITARY | S = PLCC 68 pins<br>4 = LCC 68 pins<br>G = PGA 68 pins | 67005 = 64 K (8 K x 8)<br>CMOS DUAL PORT RAM | 25 ns<br>35 ns<br>45 ns<br>55 ns |



## HI-REL DATA SHEET

**M 67024**

## 4 k x 16 CMOS DUAL PORT RAM

### MAIN FEATURES

- FAST ACCESS TIME : 25 TO 55 ns
- WIDE TEMPERATURE RANGE :
  - 55 °C TO + 125 °C
- VERY LOW POWER CONSUMPTION :
  - ACTIVE : 500 mW (typ)
  - STANDBY : 10  $\mu$ W (typ)
  - DATA-RETENTION : 5  $\mu$ W (typ)
- SEPARATE UPPER BYTE AND LOWER BYTE CONTROL FOR MULTIPLEXED BUS COMPATIBILITY
- EXPANDABLE DATA BUS TO 32 BITS OR MORE USING MASTER/SLAVE CHIP SELECT WHEN USING MORE THAN ONE DEVICE
- ON CHIP ARBITRATION LOGIC
- VERSATILE PIN SELECT FOR MASTER OR SLAVE :
  - $\overline{M/\overline{S}}$  = H FOR BUSY OUTPUT FLAG ON MASTER
  - $\overline{M/\overline{S}}$  = L FOR BUSY INPUT FLAG ON SLAVE
- INT FLAG FOR PORT TO PORT COMMUNICATION
- FULL HARDWARE SUPPORT OF SEMAPHORE SIGNALING BETWEEN PORTS
- FULLY ASYNCHRONOUS OPERATION FROM EITHER PORT
- BATTERY BACK-UP OPERATION : 2 V DATA RETENTION
- TTL COMPATIBLE
- SINGLE 5 V  $\pm$  10 % POWER SUPPLY

### DESCRIPTION

The M 67024 is a very low power CMOS dual port static RAM organised as 4096 x 16. The M 67024 is designed to be used as a stand-alone 16 bit dual port RAM or as a combination MASTER/SLAVE dual port for 32 bit or more width systems. The MATRA-MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need additional discrete logic.

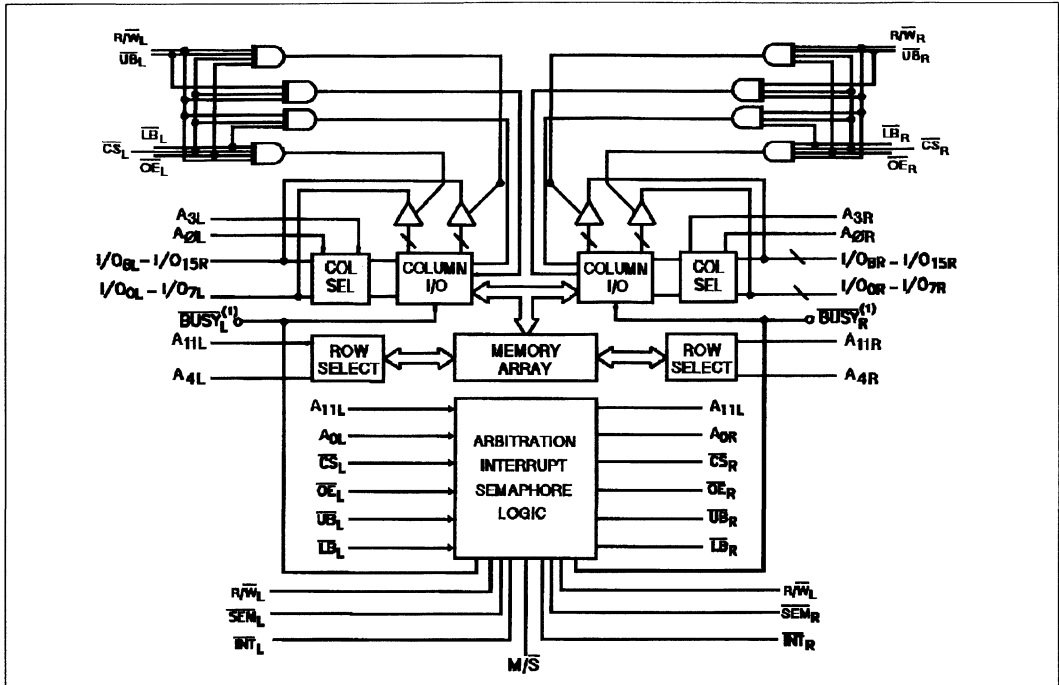
Master and slave devices provide two independant ports with separate control, address and I/O pins that permit independant, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by  $\overline{CS}$  permits the onchip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67024 combines an extremely low standby supply current (typ = 1.0  $\mu$ A) with a fast access time at 25 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5  $\mu$ W.

The M 67024 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

**10**

### BLOCK DIAGRAM

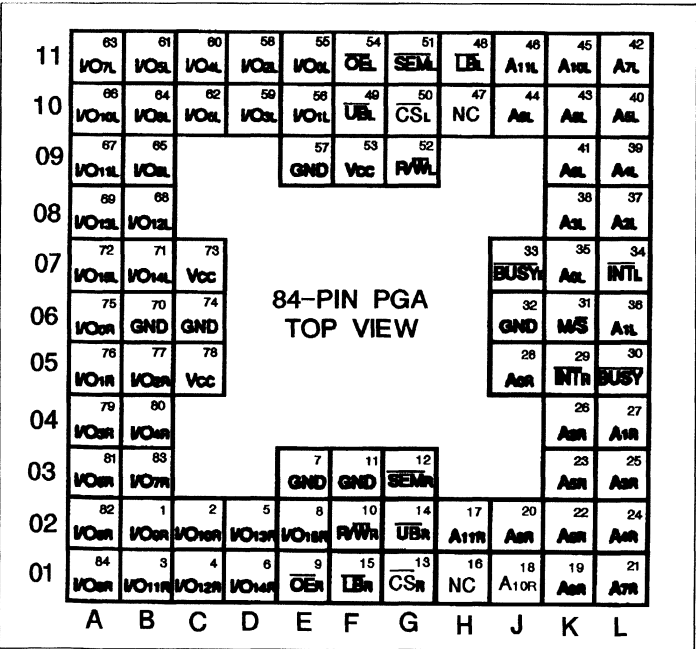
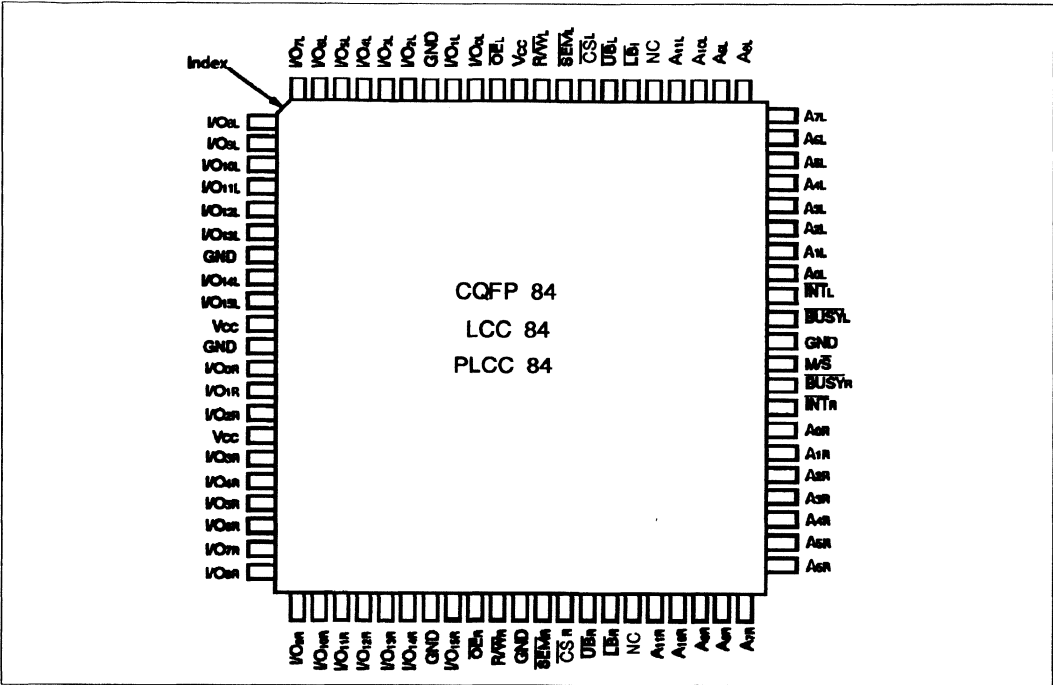


- Notes :**
1. (MASTER) :  $\overline{\text{BUSY}}$  is output. (SLAVE) :  $\overline{\text{BUSY}}$  is input
  2. LB = Lower Byte                      UB = Upper Byte.

## PIN NAMES

| LEFT PORT          | RIGHT PORT         | NAMES                  |
|--------------------|--------------------|------------------------|
| $\overline{CS}_L$  | $\overline{CS}_R$  | Chip select            |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Read/Write Enable      |
| $\overline{OE}_L$  | $\overline{OE}_R$  | Output Enable          |
| $A_{OL-11L}$       | $A_{OR-11R}$       | Address                |
| $I/O_{OL-15L}$     | $I/O_{OR-15R}$     | Data Input/Output      |
| $\overline{SEM}_L$ | $\overline{SEM}_R$ | Semaphore Enable       |
| $\overline{UB}_L$  | $\overline{UB}_R$  | Upper Byte Select      |
| $\overline{LB}_L$  | $\overline{LB}_R$  | Lower Byte Select      |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag         |
| $BUSY_L$           | $BUSY_R$           | Busy Flag              |
| $M/\overline{S}$   |                    | Master or Slave Select |
| $V_{CC}$           |                    | Power                  |
| GND                |                    | Ground                 |

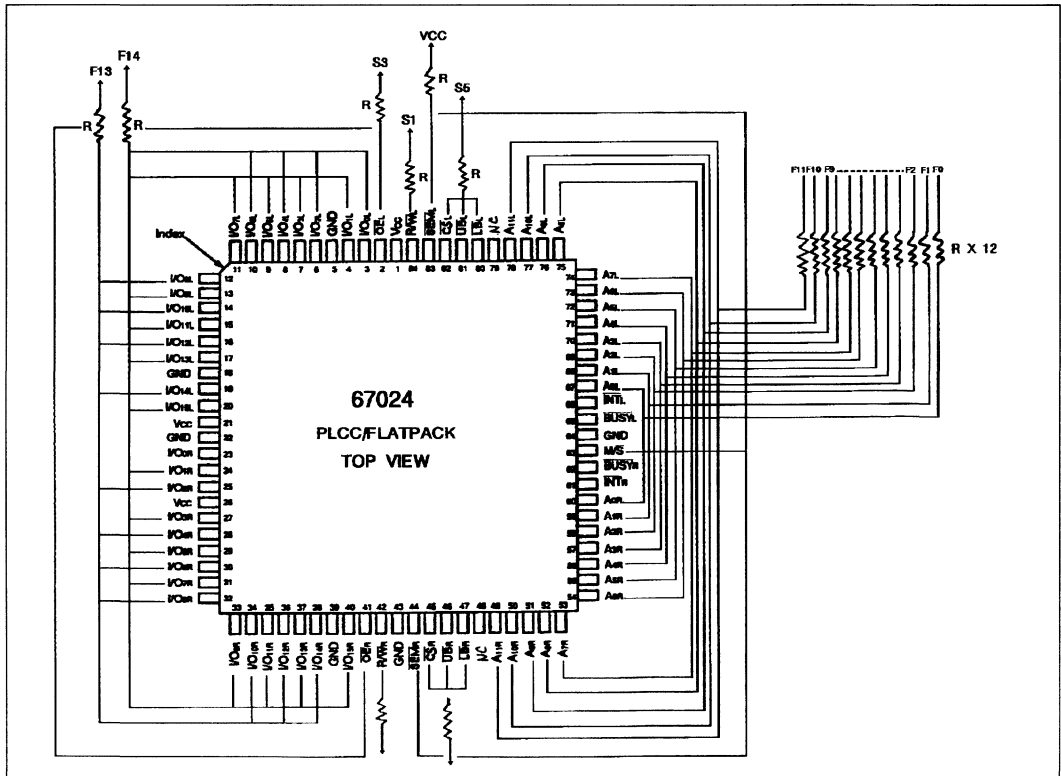
PIN CONFIGURATION



**ORDERING INFORMATION**

| TEMPERATURE RANGE                                                                                                                      | PACKAGE                                                                                        | DEVICE                    | SPEED                            | FLOW                                                                                                                                                                                                                                                                                               |
|----------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|---------------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>IM</b>                                                                                                                              | <b>QR</b>                                                                                      | <b>67024</b>              | <b>35</b>                        | <b>MB</b>                                                                                                                                                                                                                                                                                          |
|                                                                                                                                        | QR = 84 pins J CERQUAD<br>8R = 84 pins PIN GRID ARRAY<br>SR = 84 pins PLCC<br>4R = 84 pins LCC | 4 K x 16<br>DUAL PORT RAM | 25 ns<br>35 ns<br>45 ns<br>55 ns | - 8 = MHS MILITARY PROGRAM<br>MB = MIL-STD 883C CLASS B<br>CB = COMPLIANT CECC 90000<br>LEVEL B<br>SHXXX = SPECIAL CUSTOMER<br>REQUEST<br>FHXXX = FLIGHT MODELS (SPATIAL)<br>EHXXX = ENGINEERING MODELS<br>(SPATIAL)<br>MHXXX = MECHANICAL PARTS<br>(SPATIAL)<br>LHXXX = LIFE TEST PARTS (SPATIAL) |
| C = Commercial 0 °C to + 70 °C<br>I = Industrial - 40 ° to + 85 °C<br>M = Military - 55 ° to + 70 °C<br>S = Spatial - 55 ° to + 125 °C |                                                                                                |                           |                                  |                                                                                                                                                                                                                                                                                                    |

**BURN IN SCHEMATICS**



R = 5 K $\Omega$  +/- 5 % resistor  
VCC = 5,5 V +/- 5%  
S<sub>1</sub> - S<sub>5</sub> = programmable signals.

F<sub>n</sub> = 1/2 F<sub>n-1</sub>  
F<sub>0</sub> = 360 KHz

**DATA SHEET****M 67201****512 x 9  
CMOS PARALLEL FIFO****MAIN FEATURES**

- FIRST IN FIRST OUT DUAL PORT RAM
- FAST ACCESS TIME : 25 TO 55 ns
- WIDE TEMPERATURE RANGE : 55°C TO + 125°C
- VERY LOW POWER CONSUMPTION
  - ACTIVE : 500 mW (typ)
  - STANDBY : 10 W (typ)
  - DATA-RETENTION : 5 W (typ)
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- ASYNCHRONOUS READ/WRITE OPERATIONS
- EMPTY, FULL AND HALF FLAGS IN SINGLE DEVICE MODE
- RETRANSMIT CAPABILITY
- BI-DIRECTIONAL APPLICATIONS
- BATTERY BACK-UP OPERATION 2 V DATA RETENTION
- TTL COMPATIBLE
- SINGLE 5 V  $\pm$  10 % POWER SUPPLY
- HIGH PERFORMANCE SCMOS TECHNOLOGY

**DESCRIPTION**

The M 67201 is a very low power CMOS Parallel FIFO memory organized as 512 x 9. The M 67201 implements a first-in first-out algorithm, featuring asynchronous read/write operations. The FULL and EMPTY flags prevent data overflow and underflow. The Expansion logic allow unlimited expansion in word size and depth with no timing penalties. Twin address pointers automatically generate internal read and write addresses, and no external address information are required for the MATRA-MHS fifo's. Address pointers are automatically incremented with the write pin and read pin. The 9 bits wide data use in data communications applications where a parity bit for error checking is necessary. The Retransmit pin reset the Read pointer to zero without affecting the write pointer. This is very useful for retransmitting data when an error is detected in the system.

Using an array of eight transistors (8 T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67201 combines an extremely low standby supply current (typ = 1.0 A) with a fast access time at 25 ns over the full commercial temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5 W.

The M 67201 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

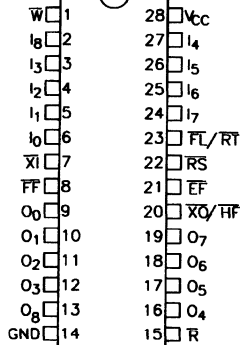
**10**

## PACKAGES

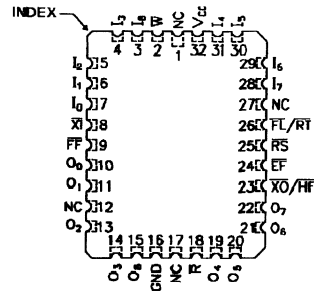
SO plastic 28 pins 300 mils  
 DIL plastic 28 pins 300 mils  
 DIL ceramic 28 pins 300 mils

SO/DIL (top view)

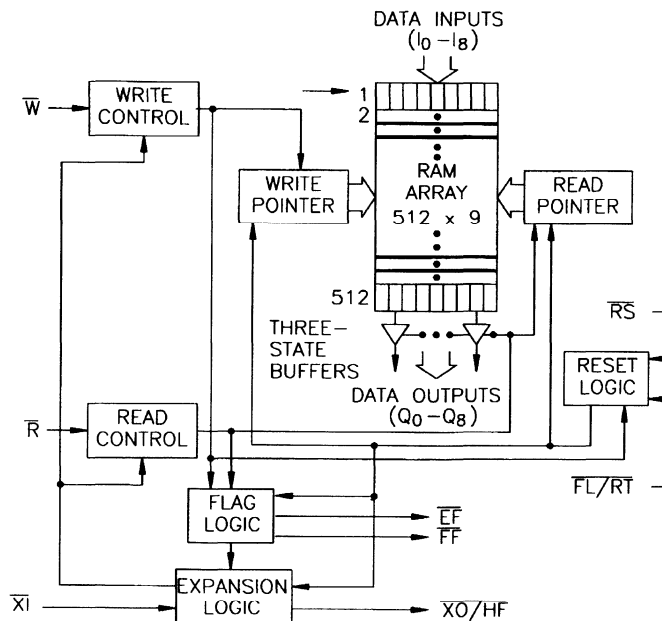
SO/DIL (top view)



LCC (top view)



## BLOCK DIAGRAM



## PIN NAMES

| NAMES              | DESCRIPTION                  |
|--------------------|------------------------------|
| I0-8               | Inputs                       |
| O0-8               | Outputs                      |
| $\overline{W}$     | Write Enable                 |
| $\overline{R}$     | Read Enable                  |
| $\overline{RS}$    | Reset                        |
| $\overline{EF}$    | Empty Flag                   |
| $\overline{FF}$    | Full Flag                    |
| XO/HF              | Expansion Out/Half-Full Flag |
| $\overline{XI}$    | Expansion IN                 |
| $\overline{FL/RT}$ | First Load/Retransmit        |
| VCC                | Power Supply                 |
| GND                | Ground                       |

## ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND) – 0.3 V to 7.0 V

Input or Output voltage applied : (GND – 0.3 V) to (VCC + 0.3 V)

Storage temperature : – 65°C to + 150°C

| OPERATING RANGE | OPERATING VOLTAGE        | OPERATING TEMPERATURE |
|-----------------|--------------------------|-----------------------|
| Military        | $V_{CC} = 5 V \pm 10 \%$ | – 55°C to + 125°C     |
| Industrial      | $V_{CC} = 5 V \pm 10 \%$ | – 40°C to + 85°C      |
| Commercial      | $V_{CC} = 5 V \pm 10 \%$ | 0°C to + 70°C         |

## ELECTRICAL CHARACTERISTICS

## DC PARAMETERS : COMMERCIAL, INDUSTRIAL, AND MILITARY

| PARAMETER | DESCRIPTION              | 67201-25 | 67201-35 |          | 67201-45 |          | 67201-55 |          | UNIT | VALUE | NOTE 8 |
|-----------|--------------------------|----------|----------|----------|----------|----------|----------|----------|------|-------|--------|
|           |                          | COM      | COM      | IND, MIL | COM      | IND, MIL | COM      | IND, MIL |      |       |        |
| ICCSB (1) | Standby supply current   | 20       | 20       | 50       | 20       | 50       | 20       | 50       | μA   | Max   | M      |
| ICCPD (2) | Power down current       | 10       | 10       | 20       | 10       | 20       | 10       | 20       | μA   | Max   | M      |
| ICCOP (3) | Operating supply current | 140      | 120      | 140      | 90       | 120      | 80       | 100      | mA   | Max   | M      |
| ILI (4)   | Input leakage current    | ±2       | ±2       | ±20      | ±1       | ±10      | ±1       | ±10      | μA   | Max   | M      |
| ILO (5)   | Output leakage current   | ±1       | ±1       | ±10      | ±1       | ±10      | ±1       | ±10      | μA   | Max   | M      |
| VIL (6)   | Input low voltage        | 0.8      | 0.8      |          | 0.8      |          | 0.8      |          | V    | Max   | T      |
| VIH (6)   | Input high voltage       | 2.2      | 2.2      |          | 2.2      |          | 2.2      |          | V    | Min   | T      |
| VOL (7)   | Output low voltage       | 0.4      | 0.4      |          | 0.4      |          | 0.4      |          | V    | Max   | M      |
| VOH (7)   | Output high voltage      | 2.4      | 2.4      |          | 2.4      |          | 2.4      |          | V    | Min   | M      |
| CIN       | Input capacitance        | 8        | 8        |          | 8        |          | 8        |          | pF   | Max   | G      |
| COUT      | Output capacitance       | 8        | 8        |          | 8        |          | 8        |          | pF   | Max   | G      |

Note 1 :  $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{CC}$ 

Note 2 : All input = Vcc

Note 3 : Icc measurements are made with outputs open

Note 4 :  $0.4 \leq V_{in} \leq V_{CC}$ Note 5 :  $R = V_{IH} 0.4 \leq V_{OUT} \leq V_{CC}$ Note 6 :  $V_{IH} \text{ max} = V_{CC} + 0.3 V$ ,  $V_{IL} \text{ min} = -0.3 V$  or  $-1 V$  pulse width 50 ns.Note 7 :  $V_{CC} \text{ min}$ ,  $I_{OL} = 8 \text{ mA}$ ,  $I_{OH} = -2 \text{ mA}$ 

Note 8 : Including open/short test or inputs clamp voltage.

G - Guaranteed - Not tested : Parameter measured at design validation and at any design changed.

10

**AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 4, 5, 6, 9, 10, 11)**

|                    |                                 |                   |
|--------------------|---------------------------------|-------------------|
| AC Test Conditions | • VCC                           | 5 V ± 10 %        |
|                    | • Input pulse levels            | Gnd to 3.0 V      |
|                    | • Input rise                    | 5 ns              |
|                    | • Input timing reference levels | 1.5 V             |
|                    | • Output loading IOL / IOH      | + 30 pF           |
|                    | • Operating temperature         | – 55°C to + 125°C |

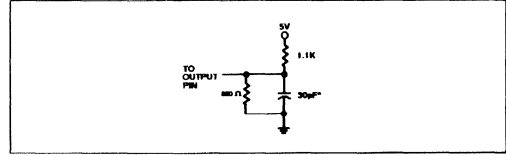
| SYMBOL<br>(1)    | SYMBOL<br>(2) | PARAMETER (3) (7)              | M 67201<br>- 25 |     | M 67201<br>- 35 |     | M 67201<br>- 45 |     | M 67201<br>- 55 |     | UNIT |
|------------------|---------------|--------------------------------|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|------|
|                  |               |                                | MIN             | MAX | MIN             | MAX | MIN             | MAX | MIN             | MAX |      |
| READ CYCLE       |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TALAL            | tRC           | Read cycle time                | 35              | –   | 45              | –   | 55              | –   | 65              | –   | ns   |
| TRLQV            | tA            | Access time                    | –               | 25  | –               | 35  | –               | 45  | –               | 55  | ns   |
| TRHRL            | tRR           | Read recovery time             | 10              | –   | 10              | –   | 10              | –   | 15              | –   | ns   |
| TRLRH            | tRPW          | Read pulse width (4)           | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TRLQX            | tRLZ          | Read low to data low Z (5)     | 5               | –   | 5               | –   | 5               | –   | 10              | –   | ns   |
| TWHQX            | tWLZ          | Write low to data low Z (5, 6) | 5               | –   | 10              | –   | 10              | –   | 15              | –   | ns   |
| TRHQX            | tDV           | Data valid from read high      | 5               | –   | 5               | –   | 5               | –   | 5               | –   | ns   |
| TRHQZ            | tRHZ          | Read high to data high Z (5)   | –               | 18  | –               | 20  | –               | 25  | –               | 30  | ns   |
| WRITE CYCLE      |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TWLWL            | tWC           | Write cycle time               | 35              | –   | 45              | –   | 55              | –   | 65              | –   | ns   |
| TWLWH            | tWPW          | Write pulse width (4)          | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TWHWL            | tWR           | Write recovery time            | 10              | –   | 10              | –   | 10              | –   | 15              | –   | ns   |
| TDWVH            | tDS           | Data set-up time               | 15              | –   | 18              | –   | 20              | –   | 30              | –   | ns   |
| TWHDX            | tDH           | Data hold time                 | 0               | –   | 0               | –   | 0               | –   | 0               | –   | ns   |
| RESET CYCLE      |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRSLWL           | tRSC          | Reset cycle time               | 35              | –   | 45              | –   | 55              | –   | 65              | –   | ns   |
| TRSLASH          | tRS           | Reset pulse width (4)          | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TWHRSH           | tRSS          | Reset set-up time              | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TRSHWL           | tRSR          | Reset recovery time            | 10              | –   | 10              | –   | 10              | –   | 15              | –   | ns   |
| RETRANSMIT CYCLE |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRTLWL           | tRTC          | Retransmit cycle time          | 35              | –   | 45              | –   | 55              | –   | 65              | –   | ns   |
| TRTLRTH          | tRT           | Retransmit pulse width (4)     | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TWHRTH           | tRTS          | Retransmit set-up time (5)     | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TRTHWL           | tRTR          | Retransmit recovery time       | 10              | –   | 10              | –   | 10              | –   | 15              | –   | ns   |
| FLAGS            |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRSLFL           | tEFL          | Reset to EF low                | –               | 35  | –               | 45  | –               | 55  | –               | 65  | ns   |
| TRSLFFH          | tHFH, tFFH    | Reset to HF/FF high            | –               | 35  | –               | 45  | –               | 55  | –               | 65  | ns   |
| TRLEFL           | tREF          | Read low to EF low             | –               | 20  | –               | 30  | –               | 40  | –               | 50  | ns   |
| TRHFFH           | tRFF          | Read high to FF high           | –               | 20  | –               | 30  | –               | 40  | –               | 50  | ns   |
| TEFHRH           | tRPE          | Read width after EF high       | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TWHEFH           | tWEF          | Write high to EF high          | –               | 25  | –               | 30  | –               | 40  | –               | 50  | ns   |
| TWLFFL           | tWFF          | Write low to FF low            | –               | 25  | –               | 30  | –               | 40  | –               | 50  | ns   |
| TWLXOL           | tWHF          | Write low to HF low            | –               | 35  | –               | 45  | –               | 55  | –               | 65  | ns   |
| TRHXOH           | tRHF          | Read high to HF high           | –               | 35  | –               | 45  | –               | 55  | –               | 65  | ns   |
| TFFHWH           | tWPF          | Write width after FF high      | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| EXPANSION        |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TWLXOL           | tXOL          | Read/Write to XO low           | –               | 25  | –               | 35  | –               | 45  | –               | 55  | ns   |
| TWHXOH           | tXOH          | Read/Write to XO high          | –               | 25  | –               | 35  | –               | 45  | –               | 55  | ns   |
| TXILXH           | tXI           | XI pulse width                 | 25              | –   | 35              | –   | 45              | –   | 55              | –   | ns   |
| TXIHXIL          | tXIR          | XI recovery time               | 10              | –   | 10              | –   | 10              | –   | 10              | –   | ns   |
| TXILRL           | tXIS          | XI set-up time                 | 15              | –   | 15              | –   | 15              | –   | 15              | –   | ns   |

- 1 : STD SYMBOL
- 2 : ALT SYMBOL
- 3 : TIMINGS REFERENCED AS IN AC TEST CONDITIONS
- 4 : PULSE WIDTHS LESS THAN MINIMUM VALUE ARE NOT ALLOWED
- 5 : VALUES GUARANTEED BY DESIGN, NOT CURRENTLY TESTED
- 6 : ONLY APPLIES TO READ DATA FLOW-THROUGH MODE
- 7 : ALL PARAMETERS TESTED ONLY



**AC TEST CONDITIONS**

|                               |                |
|-------------------------------|----------------|
| Input pulse levels            | : Gnd to 3.0 V |
| Input rise/Fall times         | : 5 ns         |
| Input timing reference levels | : 1.5 V        |
| Output reference levels       | : 1.5 V        |
| Output load                   | : See figure 1 |

**Figure 1 : Output Load.**

\* Includes jig and scope capacitance

**CAPACITANCE ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )**

| SYMBOL           | PARAMETER *        | CONDITIONS            | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input capacitance  | V <sub>IN</sub> = 0V  | 8    | pF   |
| C <sub>OUT</sub> | Output capacitance | V <sub>OUT</sub> = 0V | 8    | pF   |

**Note 1 :** This parameter is sampled and not 100 % tested**INPUTS****SIGNAL DESCRIPTIONS****DATA IN (I0-I8)**

Data inputs for 9 - bit data

**CONTROLS****RESET ( $\overline{\text{RS}}$ )**

Reset occurs whenever the Reset ( $\overline{\text{RS}}$ ) input is taken to a low state. Reset returns both internal read and write pointers to the first location. A reset is required after power-up before a write operation can be enacted. Both the Read Enable (R) and Write Enable (W) inputs must be in the high state during the period shown in figure 2 (i.e. trss before the rise edge of RS) and should not change until trsr after the rise time of the leading edge of RS. The Half-Full flag (HF) will be reset to high after Reset (RS).

**WRITE ENABLE ( $\overline{\text{W}}$ )**

A write cycle is initiated on the trailing edge of this input if the Full Flag (FF) is not set. Data set-up and hold times must be maintained in the rise time of the leading edge of the Write Enable ( $\overline{\text{W}}$ ). Data is stored sequentially in the Ram array, independently of any current read operation.

Once half the memory is filled, and during the trailing edge of the next write operation, the Half-Full Flag (HF) will be set to low and remain in this state until the difference between the write and read pointers is less than or equal to half the total available memory in the device. The Half-Full Flag (HF) is then reset by the leading edge of the read operation.

To prevent data overflow, the Full Flag ( $\overline{\text{FF}}$ ) will go low, inhibiting further write operations. On completion of a valid read operation, the Full Flag (FF) will go high after tAFF, allowing a valid write to begin. When the FIFO stack is full, the internal write pointer is blocked from W,

so that external changes to W will have no effect on the full FIFO stack.

**READ ENABLE (R)**

A read cycle is initiated on the trailing edge of the Read Enable (R) provided that the Empty Flag (EF) is not set. The data is accessed on a first in/first out basis, not with standing any current write operations. After Read Enable (R) goes high, the Data Outputs (00 - 06) will return to a high impedance state until the next Read operation. When all the data in the FIFO stack has been read, the Empty Flag (EF) will go low, allowing the "final" read cycle, but inhibiting further read operations whilst the data outputs remain in a high impedance state. Once a valid write operation has been completed, the Empty Flag (EF) will go high after tWEF and a valid read may then be initiated. When the FIFO stack is empty, the internal read pointer is blocked from R, so that external changes to R will have no effect on the empty FIFO stack.

**FIRST LOAD/RETRANSMIT ( $\overline{\text{FL}}/\overline{\text{RT}}$ )**

This is a dual-purpose input. In the Depth Expansion Mode, this pin is connected to ground to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by connecting the Expansion in (XI) to earth.

The M 67201 can be made to retransmit data when the Retransmit Enable Control (RT) input is pulsed low. A retransmit operation will set the internal read point to the first location and will not affect the write pointer. Read Enable (R) and Write Enable (W) must be in the high state during retransmit. This feature is useful if fewer than 1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag (HF), in accordance with the relative locations of the read and write pointers.

**10**

### EXPANSION IN ( $\overline{XI}$ )

This input is a dual-purpose pin. Expansion in ( $\overline{XI}$ ) is connected to earth to indicate an operation in the single device mode. Expansion in ( $\overline{XI}$ ) is connected to Expansion Out (XO) of the previous device in the Depth Expansion or Daisy Chain modes.

### OUTPUTS

#### FULL FLAG ( $\overline{FF}$ )

The Full Flag (FF) will go low, inhibiting further write operations when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset (RS), the Full Flag (FF) will go low after 512 writes.

#### EMPTY FLAG ( $\overline{EF}$ )

The Empty Flag ( $\overline{EF}$ ) will go low, inhibiting further read operations when the read pointer is equal to the write pointer, indicating that the device is empty.

#### EXPANSION OUT/HALF-FULL FLAG (XO/HF)

This is a dual-purpose output. In the simple device mode, when Expansion In ( $\overline{XI}$ ) is connected to earth, this output acts as an indication of a half-full memory.

After half the memory is filled and on the next write operation, the Half-Full Flag (HF) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to half of the total memory of the device. The Half-Full Flag (HF) is then reset by the leading of the read operation.

In the Depth Expansion Mode, Expansion in ( $\overline{XI}$ ) is connected to Expansion Out (XO) of the previous device. This output acts as a signal to the next device in the

Daisy Chain by providing a pulse to the next device when the previous device reaches the last memory location.

#### DATA OUTPUT (O0 - O8)

DATA output for 9-bit wide data. This data is in a high impedance condition whenever Read (R) is in a high state.

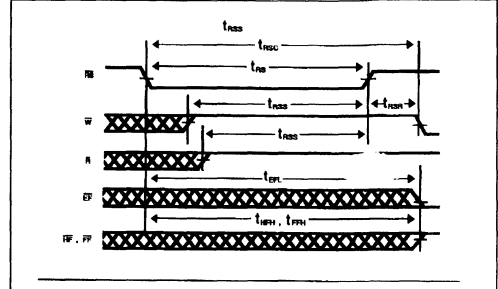


Figure 2 : Reset.

Note 1 :  $\overline{EF}$ ,  $\overline{FF}$  and  $\overline{HF}$  may change status during Reset, but flag will be valid at  $t_{RSC}$ .

Note 2 : W and R =  $V_{IH}$  around the rising edge of RS.

### OPERATING MODES

#### SINGLE DEVICE MODE

A single M 67201 may be used when the application requirements are for 512 words or less. The M 67201 is in a Single Device Configuration when the Expansion In ( $\overline{XI}$ ) control input is grounded (see Figure 12). In this mode the Half-Full Flag (HF), which is an active low output, is shared with Expansion Out (XO).

10

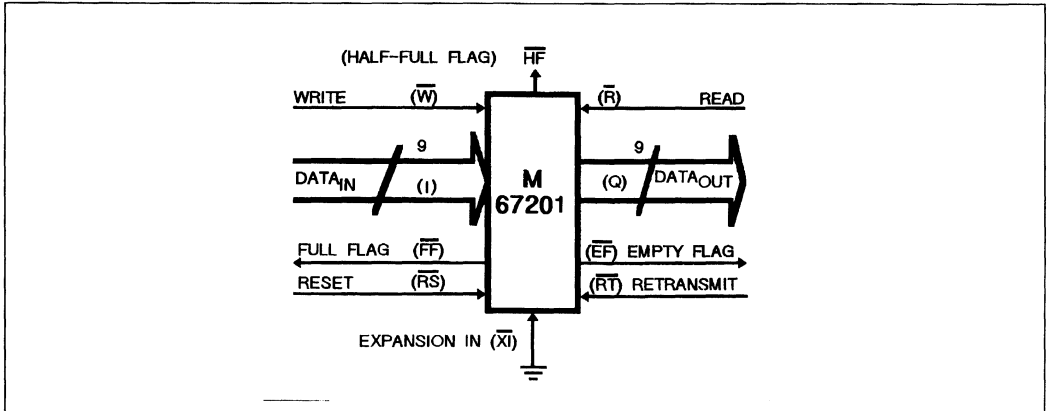
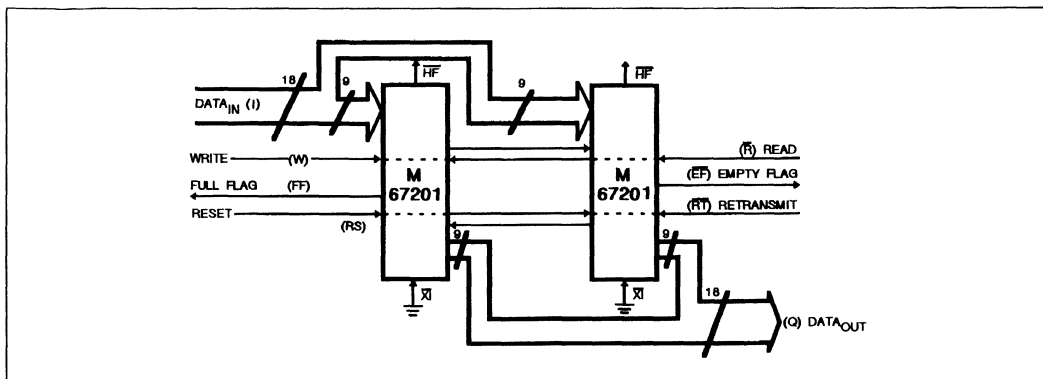


Figure 12 : Block Diagram of Single 512 x 9 FIFO.

### WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags (EF, FF and HF) can be detected from any

one device. Figure 13 demonstrates an 18-bit word width by using two M 67201s. Any word width can be attained by adding additional M 67201s.



**Note 1 :** Flag detection is accomplished by monitoring the FF, EF and the HF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

**Figure 13 :** Block Diagram of 512 x 18 FIFO Memory Used in Width Expansion Mode.

### DEPTH EXPANSION (DAISY CHAIN) MODE

The M 67201 can be easily adapted for applications which require more than 512 words. Figure 14 demonstrates Depth Expansion using three M 67201s. Any depth can be achieved by adding additional M 67201s. The M 67201s operate in the Depth Expansion configuration if the following conditions are met :

1. The first device must be designated by connecting the First Load (FL) control input to earth.
2. All other devices must have FL in the high state.
3. The Expansion Out (XO) pin of each device must be connected to the Expansion In (XI) pin of the next device. See figure 14.
4. External logic is needed to generate a composite Full Flag (FF) and Empty Flag (EF). This requires that all EFs and all FFs be ORed (i.e. all must be set to generated the correct composite FF or EF). See figure 14.
5. The Retransmit (RT) function and Half-Full Flag (HF) are not available in the Depth Expansion Mode.

### COMPOUND EXPANSION MODULE

It is quite simple to apply the two expansion techniques described above together to create large FIFO arrays (see figure 15).

### BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system being capable of Read and Write operations) can be created by coupling M 67201s as shown in figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system (i.e. FF is monitored on the device on which W is in use ; EF

is monitored on the device on which R is in use). Both Depth Expansion and Width Expansion may be used in this mode.

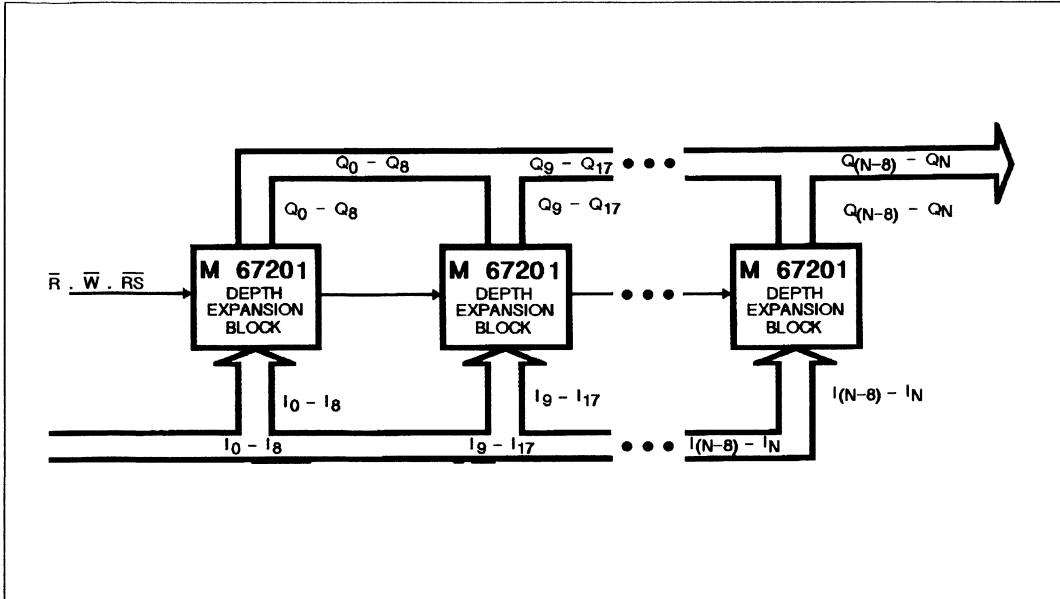
### DATA FLOW - THROUGH MODES

Two types of flow-through modes are permitted : a read flow-through and a write flow-through mode. In the read flow-through mode (figure 17) the FIFO stack allows a single word to be read after one word has been written to an empty FIFO stack. The data is enabled on the bus at  $(t_{WEF} + t_V)$  ns after the leading edge of W, which is known as the first write edge and remains on the bus until the R line is raised from low to high, after which the bus will go into a three-state mode after  $t_{MHS}$  ns. The EF line will show a pulse indicating temporary reset and then will be set. In the interval in which R is low, more words may be written to the FIFO stack (the subsequent writes after the first write edge will reset the Empty Flag) ; however, the same word (written on the first write edge) presented to the output bus as the read pointer will not be incremented if R is low. On toggling R, the remaining words written to the FIFO will appear on the output bus in accordance with the read cycle timings.

In the write flow-through mode (figure 18), the FIFO stack allows a single word of data to be written immediately a single word of data has been read from a full FIFO stack. The R line causes the FF to be reset but the W line, being low, causes it to be set again in anticipation of a new data word. The new word is loaded into the FIFO stack on the leading edge of W. The new word is loaded into the FIFO stack on the leading edge of W. The W line must be toggled when FF is not set in order to write new data into the FIFO stack and to increment the write pointer.

10





#### DEPTH EXPANSION/COMPOUND EXPANSION MODE

Note 1 : For depth expansion block see section on Depth Expansion and Figure 14.

Figure 15 : Compound FIFO Expansion.

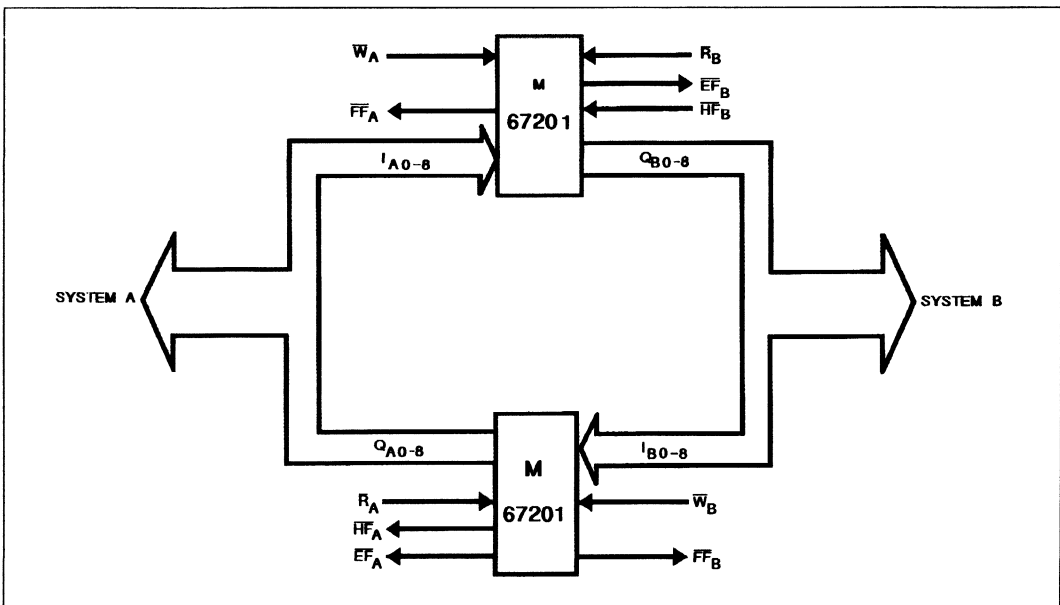


Figure 16 : Bidirectional FIFO Mode.

10

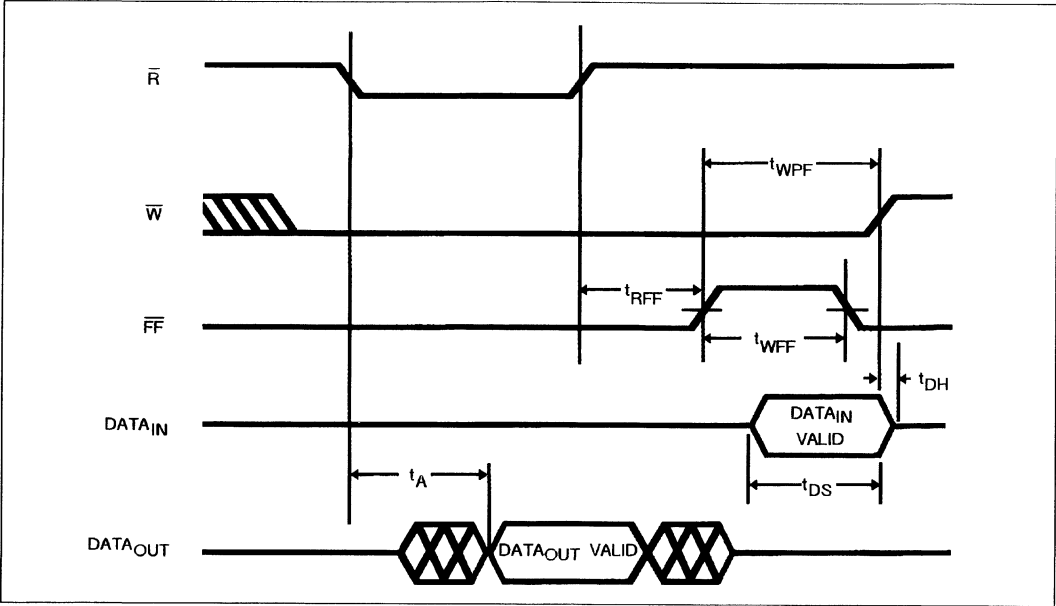


Figure 18 : Write Data Flow-Through Mode.

ORDERING INFORMATION

| Temperature Range                                                                                                                                                                                                                                                                                                                               | Package | Device | Speed | Flow |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------|-------|------|
| IM                                                                                                                                                                                                                                                                                                                                              | 1P      | 67201  | 35    | MB   |
| <div>10</div>                                                                                                                                                                                                                                                                                                                                   |         |        |       |      |
| 1P = 28 pins DIL Ceramic 300 mils<br>3P = 28 pins DIL Plastic 300 mils<br>TI = 28 pins SO L Plastic 300 mils<br>4J = 32 pins rectangular                                                                                                                                                                                                        |         |        |       |      |
| 25 ns   Blank   = No special Flows<br>35 ns   -8   = MHS MILITARY PROGRAM<br>45 ns   MB   = MIL-STD 883C CLASS B<br>55 ns   CB   = COMPLIANT CECC 90000<br>LEVEL<br>SHXXX = SPECIAL CUSTOMER REQUEST<br>FHXXX = FLIGHT MODES (SPATIAL)<br>EHXXX = ENGINEERING MODELS (SPATIAL)<br>MHXXX = MECHANICAL PARTS (SPATIAL)<br>LHXXX = LIFE TEST PARTS |         |        |       |      |
| C = Commercial 0° to 70°C<br>I = Industrial – 40° to + 85°C<br>M = Military – 55° to + 125°C<br>S = Spatial – 55° to + 125°C                                                                                                                                                                                                                    |         |        |       |      |
| 512 K x 9<br>FIRST-IN FIRST-OUT<br>DUAL PORT RAM                                                                                                                                                                                                                                                                                                |         |        |       |      |

**DATA SHEET****M 67202****1 k x 9  
CMOS PARALLEL FIFO****MAIN FEATURES**

- FIRST IN FIRST OUT DUAL PORT RAM
- FAST ACCESS TIME : 25 TO 55 ns
- WIDE TEMPERATURE RANGE : 55°C TO + 125°C
- VERY LOW POWER CONSUMPTION
  - ACTIVE : 500 mW (typ)
  - STANDBY : 10 W (typ)
  - DATA-RETENTION : 5 W (typ)
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- ASYNCHRONOUS READ/WRITE OPERATIONS
- EMPTY, FULL AND HALF FLAGS IN SINGLE DEVICE MODE
- RETRANSMIT CAPABILITY
- BI-DIRECTIONAL APPLICATIONS
- BATTERY BACK-UP OPERATION 2 V DATA RETENTION
- TTL COMPATIBLE
- SINGLE 5 V  $\pm$  10 % POWER SUPPLY
- HIGH PERFORMANCE SCMOS TECHNOLOGY

**DESCRIPTION**

The M 67202 is a very low power CMOS Parallel FIFO memory organized as 1024 x 9. The M 67202 implements a first-in first-out algorithm, featuring asynchronous read/write operations. The FULL and EMPTY flags prevent data overflow and underflow. The Expansion logic allow unlimited expansion in word size and depth with no timing penalties. Twin address pointers automatically generate internal read and write addresses, and no external address information are required for the MATRA-MHS fifo's. Address pointers are automatically incremented with the write pin and read pin. The 9 bits wide data use in data communications applications where a parity bit for error checking is necessary. The Retransmit pin reset the Read pointer to zero without affecting the write pointer. This is very useful for retransmitting data when an error is detected in the system.

Using an array of eight transistors (8 T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M 67202 combines an extremely low standby supply current (typ = 1.0 A) with a fast access time at 25 ns over the full commercial temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5 W.

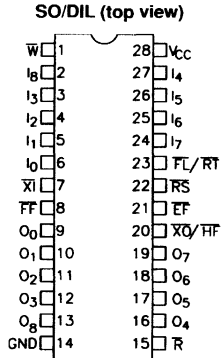
The M 67202 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

**10**

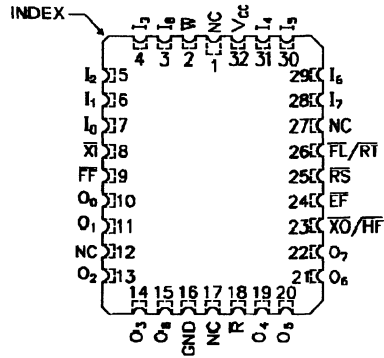
## PACKAGES

SO plastic 28 pins 300 mils  
DIL plastic 28 pins 300 mils  
DIL ceramic 28 pins 300 mils

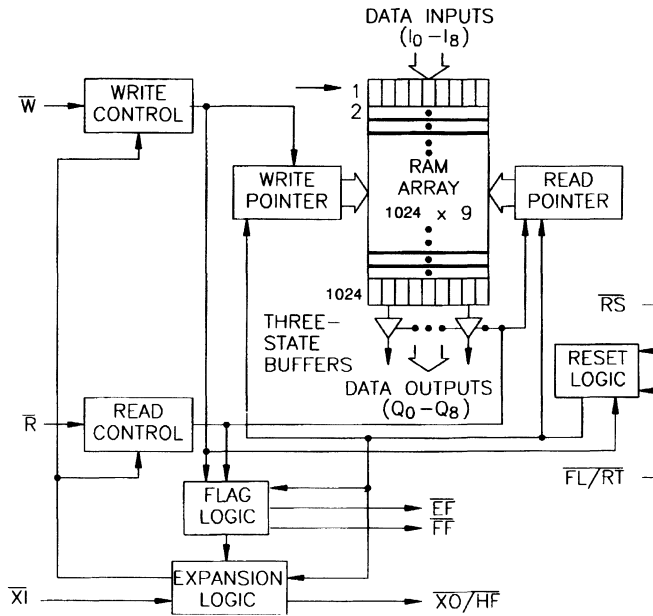
SO/DIL (top view)



LCC (top view)



## BLOCK DIAGRAM





## PIN NAMES

| NAMES | DESCRIPTION                  |
|-------|------------------------------|
| I0-8  | Inputs                       |
| O0-8  | Outputs                      |
| W     | Write Enable                 |
| R     | Read Enable                  |
| RS    | Reset                        |
| EF    | Empty Flag                   |
| FF    | Full Flag                    |
| XO/HF | Expansion Out/Half-Full Flag |
| XI    | Expansion IN                 |
| FL/RT | First Load/Retransmit        |
| VCC   | Power Supply                 |
| GND   | Ground                       |

## ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND) – 0.3 V to 7.0 V  
 Input or Output voltage applied : (GND – 0.3 V) to (VCC + 0.3 V)  
 Storage temperature : – 65°C to + 150°C

| OPERATING RANGE | OPERATING VOLTAGE              | OPERATING TEMPERATURE |
|-----------------|--------------------------------|-----------------------|
| Military        | $V_{CC} = 5\text{ V} \pm 10\%$ | - 55°C to + 125°C     |
| Industrial      | $V_{CC} = 5\text{ V} \pm 10\%$ | - 40°C to + 85°C      |
| Commercial      | $V_{CC} = 5\text{ V} \pm 10\%$ | 0°C to + 70°C         |

## ELECTRICAL CHARACTERISTICS

## DC PARAMETERS : COMMERCIAL, INDUSTRIAL, AND MILITARY

| PARAMETER | DESCRIPTION              | 67202-25 | 67202-35 |          | 67202-45 |          | 67202-55 |          | UNIT | VALUE | NOTE 8 |
|-----------|--------------------------|----------|----------|----------|----------|----------|----------|----------|------|-------|--------|
|           |                          | COM      | COM      | IND, MIL | COM      | IND, MIL | COM      | IND, MIL |      |       |        |
| ICCSB (1) | Standby supply current   | 20       | 20       | 50       | 20       | 50       | 20       | 50       | μA   | Max   | M      |
| ICCPD (2) | Power down current       | 10       | 10       | 20       | 10       | 20       | 10       | 20       | μA   | Max   | M      |
| ICCOP (3) | Operating supply current | 140      | 120      | 140      | 90       | 120      | 80       | 100      | mA   | Max   | M      |
| ILI (4)   | Input leakage current    | ±2       | ±2       | ±20      | ±1       | ±10      | ±1       | ±10      | μA   | Max   | M      |
| ILO (5)   | Output leakage current   | ±1       | ±1       | ±10      | ±1       | ±10      | ±1       | ±10      | μA   | Max   | M      |
| VIL (6)   | Input low voltage        | 0.8      | 0.8      |          | 0.8      |          | 0.8      |          | V    | Max   | T      |
| VIH (6)   | Input high voltage       | 2.2      | 2.2      |          | 2.2      |          | 2.2      |          | V    | Min   | T      |
| VOL (7)   | Output low voltage       | 0.4      | 0.4      |          | 0.4      |          | 0.4      |          | V    | Max   | M      |
| VOH (7)   | Output high voltage      | 2.4      | 2.4      |          | 2.4      |          | 2.4      |          | V    | Min   | M      |
| CIN       | Input capacitance        | 8        | 8        |          | 8        |          | 8        |          | pF   | Max   | G      |
| COU       | Output capacitance       | 8        | 8        |          | 8        |          | 8        |          | pF   | Max   | G      |

Note 1 :  $\bar{R} = \bar{W} = \bar{RS} = \bar{FL/RT} = V_{CC}$

Note 2 : All input =  $V_{CC}$

Note 3 : Icc measurements are made with outputs open

Note 4 :  $0.4 \leq V_{in} \leq V_{CC}$

Note 5 :  $R = V_{IH} 0.4 \leq V_{OUT} \leq V_{CC}$

Note 6 :  $V_{IH} \text{ max} = V_{CC} + 0.3\text{ V}$ ,  $V_{IL} \text{ min} = -0.3\text{ V}$  or  $-1\text{ V}$  pulse width 50 ns.

Note 7 :  $V_{CC} \text{ min}$ ,  $I_{OL} = 8\text{ mA}$ ,  $I_{OH} = -2\text{ mA}$

Note 8 : Including open/short test or inputs clamp voltage.

G - Guaranteed - Not tested : Parameter measured at design validation and at any design changed.

10

**AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 4, 5, 6, 9, 10, 11)**

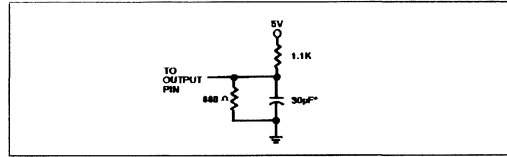
|                    |                                                                                                                                                                                                                                                                                        |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AC Test Conditions | <ul style="list-style-type: none"> <li>• VCC 5 V ± 10 %</li> <li>• Input pulse levels Gnd to 3.0 V</li> <li>• Input rise 5 ns</li> <li>• Input timing reference levels 1.5 V</li> <li>• Output loading IOL / IOH + 30 pF</li> <li>• Operating temperature - 55°C to + 125°C</li> </ul> |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

| SYMBOL<br>(1)    | SYMBOL<br>(2) | PARAMETER (3) (7)              | M 67202<br>- 25 |     | M 67202<br>- 35 |     | M 67202<br>- 45 |     | M 67202<br>- 55 |     | UNIT |
|------------------|---------------|--------------------------------|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|------|
|                  |               |                                | MIN             | MAX | MIN             | MAX | MIN             | MAX | MIN             | MAX |      |
| READ CYCLE       |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TALAL            | tRC           | Read cycle time                | 35              | —   | 45              | —   | 55              | —   | 65              | —   | ns   |
| TRLQV            | tA            | Access time                    | —               | 25  | —               | 35  | —               | 45  | —               | 55  | ns   |
| TRHRL            | tRR           | Read recovery time             | 10              | —   | 10              | —   | 10              | —   | 15              | —   | ns   |
| TRLRH            | tRPW          | Read pulse width (4)           | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TRLQX            | tRLZ          | Read low to data low Z (5)     | 5               | —   | 5               | —   | 5               | —   | 10              | —   | ns   |
| TWHQX            | tWLZ          | Write low to data low Z (5, 6) | 5               | —   | 10              | —   | 10              | —   | 15              | —   | ns   |
| TRHQX            | tDV           | Data valid from read high      | 5               | —   | 5               | —   | 5               | —   | 5               | —   | ns   |
| TRHQZ            | tRHZ          | Read high to data high Z (5)   | —               | 18  | —               | 20  | —               | 25  | —               | 30  | ns   |
| WRITE CYCLE      |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TWLWL            | tWC           | Write cycle time               | 35              | —   | 45              | —   | 55              | —   | 65              | —   | ns   |
| TWLWH            | tWPW          | Write pulse width (4)          | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TWHWL            | tWR           | Write recovery time            | 10              | —   | 10              | —   | 10              | —   | 15              | —   | ns   |
| TDWVH            | tDS           | Data set-up time               | 15              | —   | 18              | —   | 20              | —   | 30              | —   | ns   |
| TWHDH            | tDH           | Data hold time                 | 0               | —   | 0               | —   | 0               | —   | 0               | —   | ns   |
| RESET CYCLE      |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRSLWL           | tRSC          | Reset cycle time               | 35              | —   | 45              | —   | 55              | —   | 65              | —   | ns   |
| TRSLASH          | tRS           | Reset pulse width (4)          | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TWHRSH           | tRSS          | Reset set-up time              | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TRSHWL           | tRSR          | Reset recovery time            | 10              | —   | 10              | —   | 10              | —   | 15              | —   | ns   |
| RETRANSMIT CYCLE |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRTLWL           | tRTC          | Retransmit cycle time          | 35              | —   | 45              | —   | 55              | —   | 65              | —   | ns   |
| TRTLRTH          | tRT           | Retransmit pulse width (4)     | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TWHRTH           | tRTS          | Retransmit set-up time (5)     | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TRTHWL           | tRTR          | Retransmit recovery time       | 10              | —   | 10              | —   | 10              | —   | 15              | —   | ns   |
| FLAGS            |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TRSLFL           | tEFL          | Reset to EF low                | —               | 35  | —               | 45  | —               | 55  | —               | 65  | ns   |
| TRSLFFH          | tHFH, tFFH    | Reset to HF/FF high            | —               | 35  | —               | 45  | —               | 55  | —               | 65  | ns   |
| TRLEFL           | tREF          | Read low to EF low             | —               | 20  | —               | 30  | —               | 40  | —               | 50  | ns   |
| TRHFFH           | tRFF          | Read high to FF high           | —               | 20  | —               | 30  | —               | 40  | —               | 50  | ns   |
| TEFHRH           | tRPE          | Read width after EF high       | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TWHEFH           | tWEF          | Write high to EF high          | —               | 25  | —               | 30  | —               | 40  | —               | 50  | ns   |
| TWLFFL           | tWFF          | Write low to FF low            | —               | 25  | —               | 30  | —               | 40  | —               | 50  | ns   |
| TWLXOL           | tWHF          | Write low to HF low            | —               | 35  | —               | 45  | —               | 55  | —               | 65  | ns   |
| TRHXOH           | tRHF          | Read high to HF high           | —               | 35  | —               | 45  | —               | 55  | —               | 65  | ns   |
| TFHFHH           | tWPF          | Write width after FF high      | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| EXPANSION        |               |                                |                 |     |                 |     |                 |     |                 |     |      |
| TWLXOL           | tXOL          | Read/Write to XO low           | —               | 25  | —               | 35  | —               | 45  | —               | 55  | ns   |
| TWHXOH           | tXOH          | Read/Write to XO high          | —               | 25  | —               | 35  | —               | 45  | —               | 55  | ns   |
| TXILXH           | tXI           | XI pulse width                 | 25              | —   | 35              | —   | 45              | —   | 55              | —   | ns   |
| TXIHXL           | tXIR          | XI recovery time               | 10              | —   | 10              | —   | 10              | —   | 10              | —   | ns   |
| TXILRL           | tXIS          | XI set-up time                 | 15              | —   | 15              | —   | 15              | —   | 15              | —   | ns   |

- 1 : STD SYMBOL  
2 : ALT SYMBOL  
3 : TIMINGS REFERENCED AS IN AC TEST CONDITIONS  
4 : PULSE WIDTHS LESS THAN MINIMUM VALUE ARE NOT ALLOWED  
5 : VALUES GUARANTEED BY DESIGN, NOT CURRENTLY TESTED  
6 : ONLY APPLIES TO READ DATA FLOW-THROUGH MODE  
7 : ALL PARAMETERS TESTED ONLY

**AC TEST CONDITIONS**

|                               |                |
|-------------------------------|----------------|
| Input pulse levels            | : Gnd to 3.0 V |
| Input rise/Fall times         | : 5 ns         |
| Input timing reference levels | : 1.5 V        |
| Output reference levels       | : 1.5 V        |
| Output load                   | : See figure 1 |

**Figure 1 : Output Load.**

\* Includes jig and scope capacitance

**CAPACITANCE ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )**

| SYMBOL    | PARAMETER *        | CONDITIONS     | MAX. | UNIT |
|-----------|--------------------|----------------|------|------|
| $C_{IN}$  | Input capacitance  | $V_{IN} = 0V$  | 8    | pF   |
| $C_{OUT}$ | Output capacitance | $V_{OUT} = 0V$ | 8    | pF   |

**Note 1 :** This parameter is sampled and not 100 % tested**INPUTS****SIGNAL DESCRIPTIONS****DATA IN (I0-I8)**

Data inputs for 9 - bit data

**CONTROLS****RESET ( $\overline{RS}$ )**

Reset occurs whenever the Reset ( $\overline{RS}$ ) input is taken to a low state. Reset returns both internal read and write pointers to the first location. A reset is required after power-up before a write operation can be enacted. Both the Read Enable ( $\overline{R}$ ) and Write Enable ( $\overline{W}$ ) inputs must be in the high state during the period shown in figure 2 (i.e.  $t_{RS}$  before the rise edge of  $\overline{RS}$ ) and should not change until  $t_{RS}$  after the rise time of the leading edge of  $\overline{RS}$ . The Half-Full flag (HF) will be reset to high after Reset ( $\overline{RS}$ ).

**WRITE ENABLE ( $\overline{W}$ )**

A write cycle is initiated on the trailing edge of this input if the Full Flag (FF) is not set. Data set-up and hold times must be maintained in the rise time of the leading edge of the Write Enable ( $\overline{W}$ ). Data is stored sequentially in the Ram array, independently of any current read operation.

Once half the memory is filled, and during the trailing edge of the next write operation, the Half-Full Flag (HF) will be set to low and remain in this state until the difference between the write and read pointers is less than or equal to half the total available memory in the device. The Half-Full Flag (HF) is then reset by the leading edge of the read operation.

To prevent data overflow, the Full Flag ( $\overline{FF}$ ) will go low, inhibiting further write operations. On completion of a valid read operation, the Full Flag ( $\overline{FF}$ ) will go high after  $t_{AFF}$ , allowing a valid write to begin. When the FIFO stack is full, the internal write pointer is blocked from  $\overline{W}$ ,

so that external changes to  $\overline{W}$  will have no effect on the full FIFO stack.

**READ ENABLE ( $\overline{R}$ )**

A read cycle is initiated on the trailing edge of the Read Enable ( $\overline{R}$ ) provided that the Empty Flag (EF) is not set. The data is accessed on a first in/first out basis, not with standing any current write operations. After Read Enable ( $\overline{R}$ ) goes high, the Data Outputs (O0 - O6) will return to a high impedance state until the next Read operation. When all the data in the FIFO stack has been read, the Empty Flag (EF) will go low, allowing the "final" read cycle, but inhibiting further read operations whilst the data outputs remain in a high impedance state. Once a valid write operation has been completed, the Empty Flag ( $\overline{EF}$ ) will go high after  $t_{WEF}$  and a valid read may then be initiated. When the FIFO stack is empty, the internal read pointer is blocked from  $\overline{R}$ , so that external changes to  $\overline{R}$  will have no effect on the empty FIFO stack.

**FIRST LOAD/RETRANSMIT ( $\overline{FL/RT}$ )**

This is a dual-purpose input. In the Depth Expansion Mode, this pin is connected to ground to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by connecting the Expansion in (XI) to earth.

The M 67202 can be made to retransmit data when the Retransmit Enable Control (RT) input is pulsed low. A retransmit operation will set the internal read point to the first location and will not affect the write pointer. Read Enable ( $\overline{R}$ ) and Write Enable ( $\overline{W}$ ) must be in the high state during retransmit. This feature is useful if fewer than 1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag (HF), in accordance with the relative locations of the read and write pointers.

**10**

### EXPANSION IN ( $\overline{XI}$ )

This input is a dual-purpose pin. Expansion in ( $\overline{XI}$ ) is connected to earth to indicate an operation in the single device mode. Expansion in ( $XI$ ) is connected to Expansion Out ( $XO$ ) of the previous device in the Depth Expansion or Daisy Chain modes.

### OUTPUTS

#### FULL FLAG ( $\overline{FF}$ )

The Full Flag ( $\overline{FF}$ ) will go low, inhibiting further write operations when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ( $RS$ ), the Full Flag ( $\overline{FF}$ ) will go low after 1024 writes.

#### EMPTY FLAG ( $\overline{EF}$ )

The Empty Flag ( $\overline{EF}$ ) will go low, inhibiting further read operations when the read pointer is equal to the write pointer, indicating that the device is empty.

#### EXPANSION OUT/HALF-FULL FLAG ( $XO/HF$ )

This is a dual-purpose output. In the simple device mode, when Expansion In ( $XI$ ) is connected to earth, this output acts as an indication of a half-full memory.

After half the memory is filled and on the next write operation, the Half-Full Flag ( $HF$ ) will be set to low and will remain set until the difference between the write and read pointers is less than or equal to half of the total memory of the device. The Half-Full Flag ( $HF$ ) is then reset by the leading of the read operation.

In the Depth Expansion Mode, Expansion in ( $\overline{XI}$ ) is connected to Expansion Out ( $XO$ ) of the previous device. This output acts as a signal to the next device in the

Daisy Chain by providing a pulse to the next device when the previous device reaches the last memory location.

#### DATA OUTPUT ( $O0 - O8$ )

DATA output for 9-bit wide data. This data is in a high impedance condition whenever Read ( $R$ ) is in a high state.

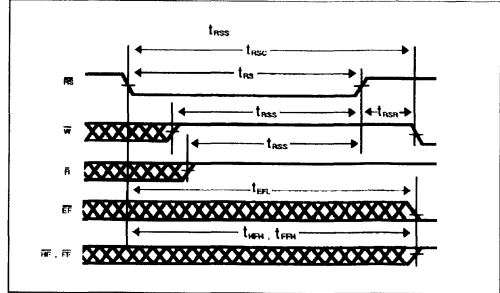


Figure 2 : Reset.

**Note 1 :**  $\overline{EF}$ ,  $\overline{FF}$  and  $\overline{HF}$  may change status during Reset, but flag will be valid at  $t_{RSC}$ .

**Note 2 :**  $W$  and  $R = V_{IH}$  around the rising edge of  $RS$ .

### OPERATING MODES

#### SINGLE DEVICE MODE

A single M 67202 may be used when the application requirements are for 1024 words or less. The M 67202 is in a Single Device Configuration when the Expansion In ( $XI$ ) control input is grounded (see Figure 12). In this mode the Half-Full Flag ( $HF$ ), which is an active low output, is shared with Expansion Out ( $XO$ ).

10

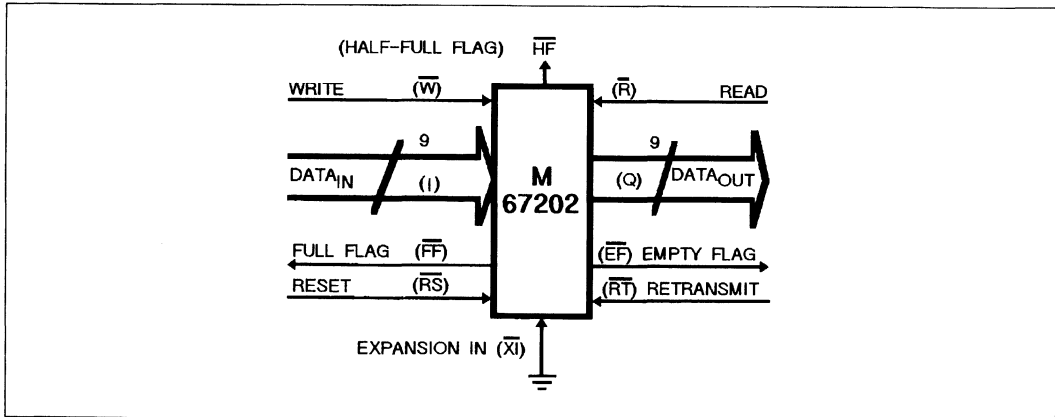
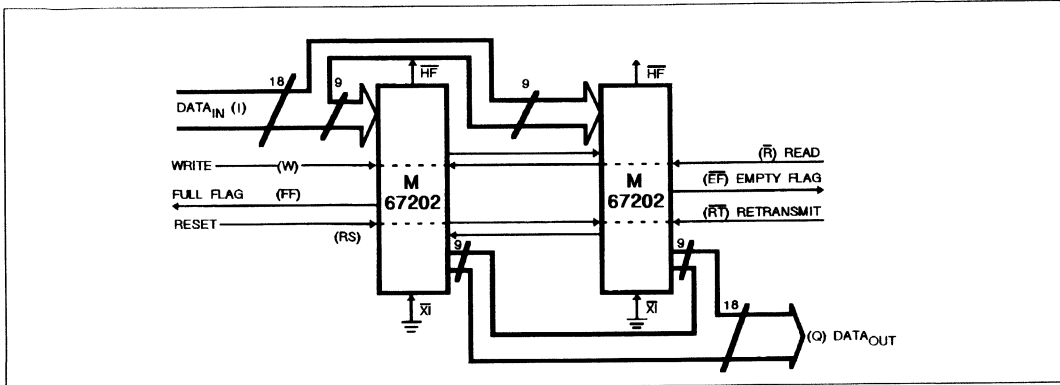


Figure 12 : Block Diagram of Single 1024 x 9 FIFO.

### WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags (EF, FF and HF) can be detected from any

one device. Figure 13 demonstrates an 18-bit word width by using two M 67202s. Any word width can be attained by adding additional M 67202s.



**Note 1 :** Flag detection is accomplished by monitoring the FF, EF and the HF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

**Figure 13 :** Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode.

### DEPTH EXPANSION (DAISY CHAIN) MODE

The M 67202 can be easily adapted for applications which require more than 1024 words. Figure 14 demonstrates Depth Expansion using three M 67202s. Any depth can be achieved by adding additional MM 67202s. The M 67202s operate in the Depth Expansion configuration if the following conditions are met :

1. The first device must be designated by connecting the First Load (FL) control input to earth.
2. All other devices must have FL in the high state.
3. The Expansion Out (XO) pin of each device must be connected to the Expansion In (XI) pin of the next device. See figure 14.
4. External logic is needed to generate a composite Full Flag (FF) and Empty Flag (EF). This requires that all EFs and all FFs be ORed (i.e. all must be set to generated the correct composite FF or EF). See figure 14.
5. The Retransmit (RT) function and Half-Full Flag (HF) are not available in the Depth Expansion Mode.

### COMPOUND EXPANSION MODULE

It is quite simple to apply the two expansion techniques described above together to create large FIFO arrays (see figure 15).

### BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system being capable of Read and Write operations) can be created by coupling M 67202s as shown in figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system (i.e. FF is monitored on the device on which W is in use ; EF

is monitored on the device on which R is in use). Both Depth Expansion and Width Expansion may be used in this mode.

### DATA FLOW - THROUGH MODES

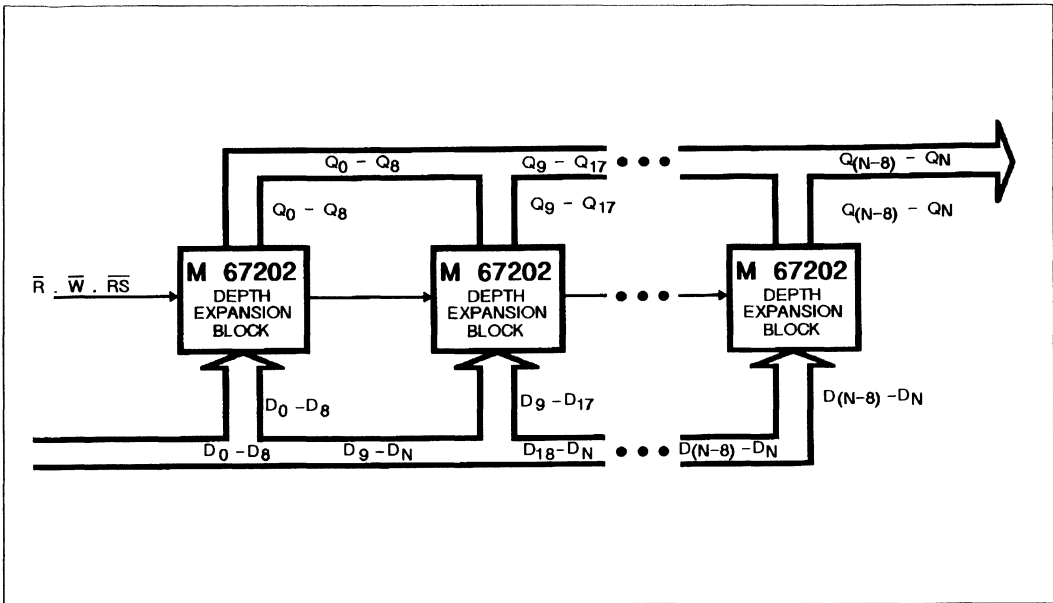
Two types of flow-through modes are permitted : a read flow-through and a write flow-through mode. In the read flow-through mode (figure 17) the FIFO stack allows a single word to be read after one word has been written to an empty FIFO stack. The data is enabled on the bus at  $(t_{WEF} + t_V)$  ns after the leading edge of W, which is known as the first write edge and remains on the bus until the R line is raised from low to high, after which the bus will go into a three-state mode after  $t_{MHS}$  ns. The EF line will show a pulse indicating temporary reset and then will be set. In the interval in which R is low, more words may be written to the FIFO stack (the subsequent writes after the first write edge will reset the Empty Flag) ; however, the same word (written on the first write edge) presented to the output bus as the read pointer will not be incremented if R is low. On toggling R, the remaining words written to the FIFO will appear on the output bus in accordance with the read cycle timings.

In the write flow-through mode (figure 18), the FIFO stack allows a single word of data to be written immediately a single word of data has been read from a full FIFO stack. The R line causes the FF to be reset but the W line, being low, causes it to be set again in anticipation of a new data word. The new word is loaded into the FIFO stack on the leading edge of W. The new word is loaded into the FIFO stack on the leading edge of W. The W line must be toggled when FF is not set in order to write new data into the FIFO stack and to increment the write pointer.

**TABLE I - RESET AND RETRANSMIT**

10





Note 2 : For Flag detection see section on Width Expansion an Figure 13.

Figure 15 : Compound FIFO Expansion.

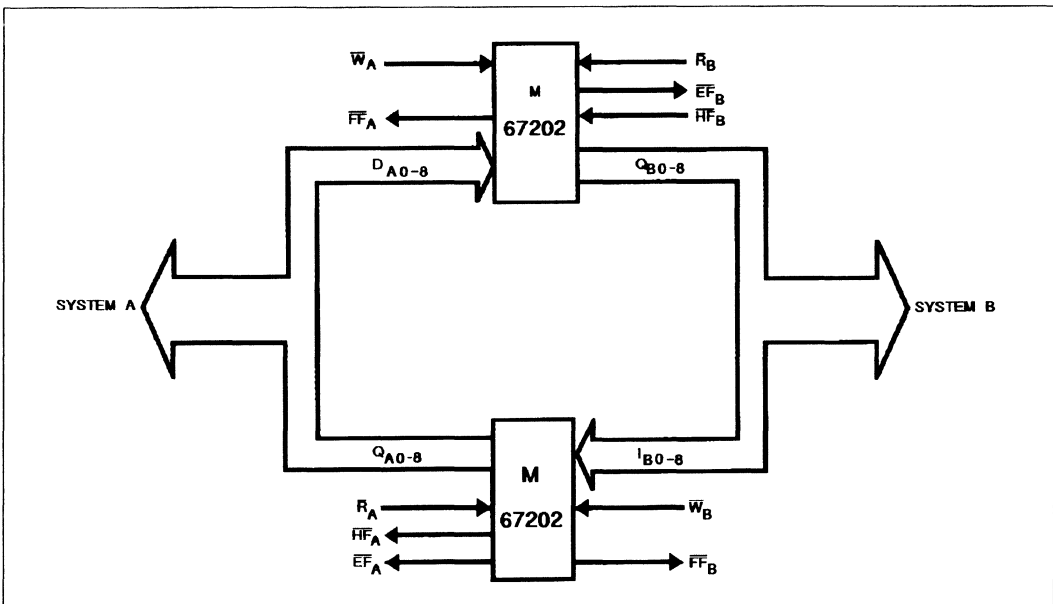


Figure 16 : Bidirectional FIFO Mode.

10

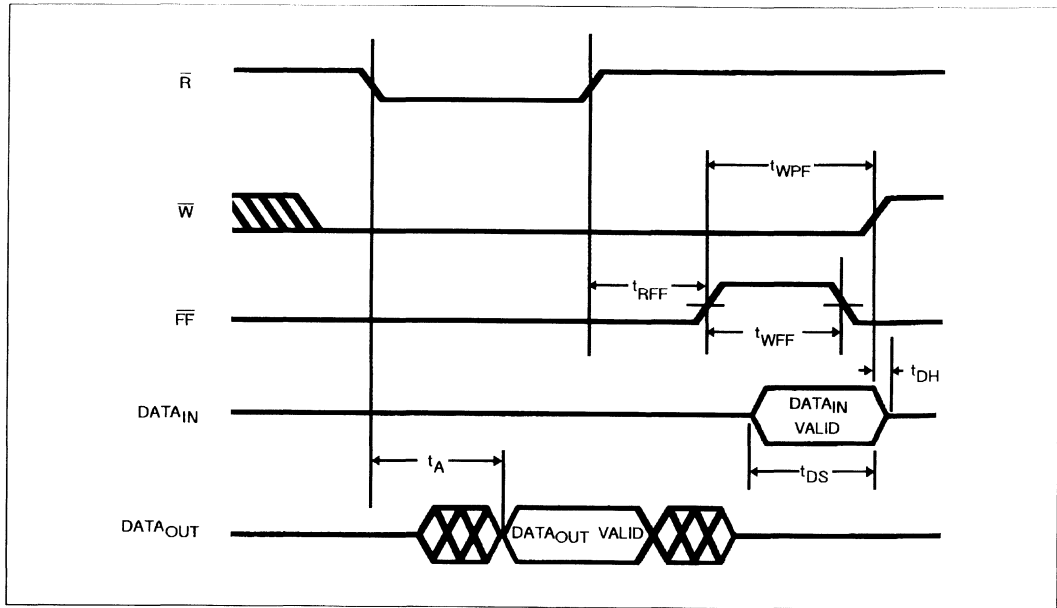


Figure 18 : Write Data Flow-Through Mode.

## ORDERING INFORMATION

| Temperature Range                                                                                                                                                                                                                                                                                                | Package | Device | Speed | Flow |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------|-------|------|
| IM                                                                                                                                                                                                                                                                                                               | 1P      | 67202  | 35    | MB   |
| 1P = 28 pins DIL Ceramic 300 mils<br>3P = 28 pins DIL Plastic 300 mils<br>TI = 28 pins SO L Plastic 300 mils<br>4J = 32 pins rectangular                                                                                                                                                                         |         |        |       |      |
| C = Commercial 0° to 70°C<br>I = Industrial - 40° to + 85°C<br>M = Military - 55° to + 125°C<br>S = Spatial - 55° to + 125°C                                                                                                                                                                                     |         |        |       |      |
| 1K x 9<br>FIRST-IN FIRST-OUT<br>DUAL PORT RAM                                                                                                                                                                                                                                                                    |         |        |       |      |
| 25 ns<br>35 ns<br>45 ns<br>55 ns                                                                                                                                                                                                                                                                                 |         |        |       |      |
| Blank = No special Flows<br>-8 = MHS MILITARY PROGRAM<br>MB = MIL-STD 883C CLASS B<br>CB = COMPLIANT CECC 90000<br>LEVEL<br>SHXXX = SPECIAL CUSTOMER<br>REQUEST<br>FHXXX = FLIGHT MODES (SPATIAL)<br>EHXXX = ENGINEERING MODELS<br>(SPATIAL)<br>MHXXX = MECHANICAL PARTS<br>(SPATIAL)<br>LHXXX = LIFE TEST PARTS |         |        |       |      |



# CACHE CONTROLLERS

**11**





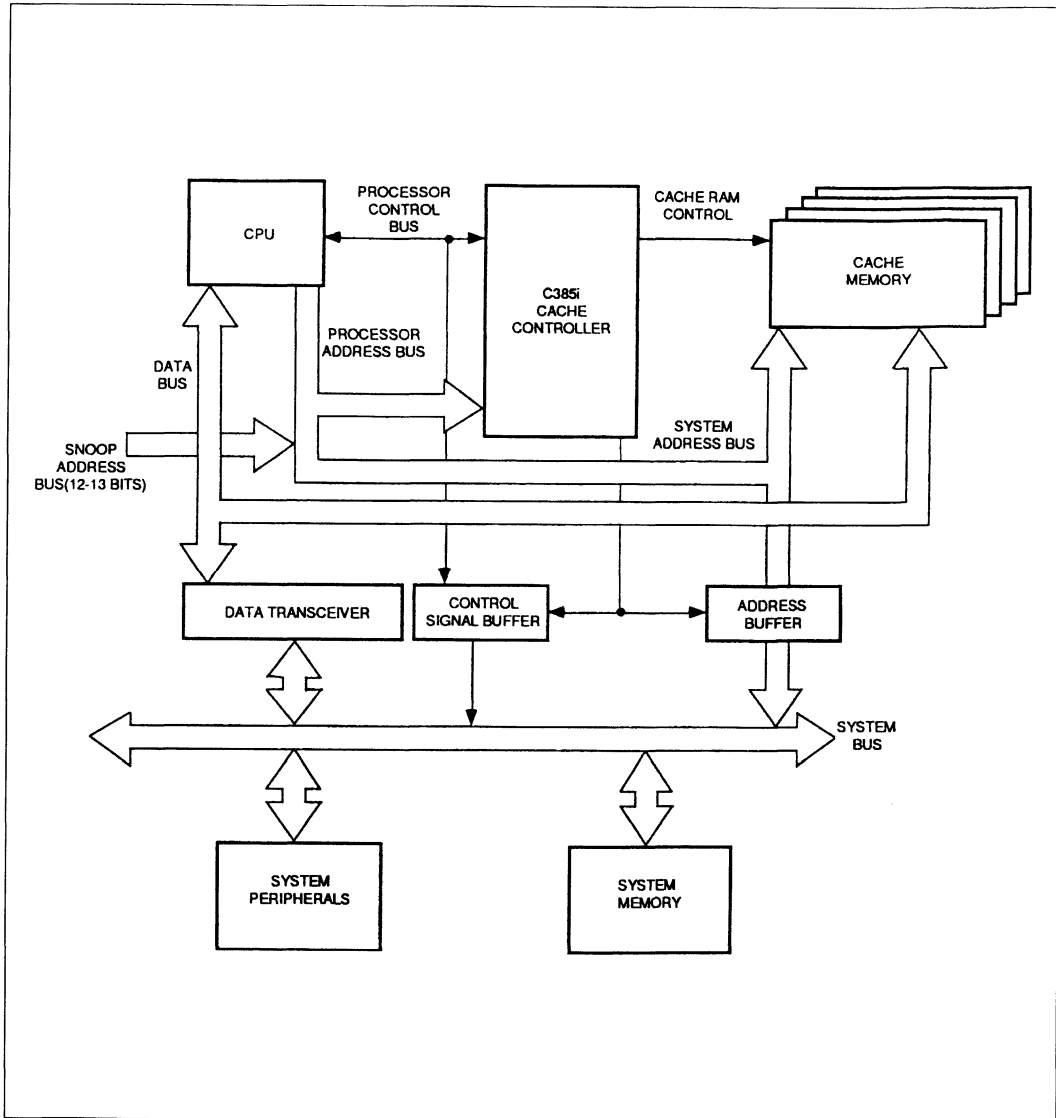
**DATA SHEET****M-82C385**

## 32 kB 32-BIT CACHE CONTROLLER

### FEATURES

- COMPATIBLE WITH INTEL 82385 32-BIT CACHE CONTROLLER
- HIGHLY INTEGRATED AND OPTIMIZED FOR 386™ DX CPU BASED SYSTEMS
  - TIGHTLY COUPLED 386 CPU INTERFACE
  - INTEGRATED SYSTEM INTERFACE, CPU INTERFACE, CACHE DIRECTORY, AND CACHE INTERFACE LOGIC
  - INTERFACES DIRECTLY WITH INDUSTRY-STANDARD HIGH-SPEED 16 k x 4, 8 k x 8, or 4 k x 16 STATIC RAMs, OR WITH 4 k x 16/18 and 8 k x 16 CACHE RAMs
- MAPS THE FULL 4 GIGABYTE ADDRESS SPACE OF THE 80386 CPU
- SUPPORTS 32 kB CACHE
- TWO CACHE-MAPPING OPTIONS
  - DIRECT-MAPPED
  - 2-WAY SET-ASSOCIATIVE
- WRITE-THRU SCHEME FOR UPDATING MAIN MEMORY, INCLUDING POSTED WRITE
- BUS SNOOPING FOR MAINTAINING COHERENCY WHILE ANOTHER BUS MASTER ACCESSES MAIN MEMORY LOCATIONS CURRENTLY IN CACHE
- LRU REPLACEMENT ALGORITHM
- CACHE FLUSH FOR MULTI-PROCESSOR AND DIAGNOSTIC SUPPORT
- FLEXIBLE SUPPORT FOR NON-CACHEABLE MEMORY LOCATIONS
- 20, 25 AND 33 MHz OPERATION
  - UPWARD MIGRATION PATH TO 42 MHz
- 0.8-MICRON (DRAWN) CMOS TECHNOLOGY
- 132-LEAD PGA PACKAGE WITH INTEL-COMPATIBLE PINOUT

**11**



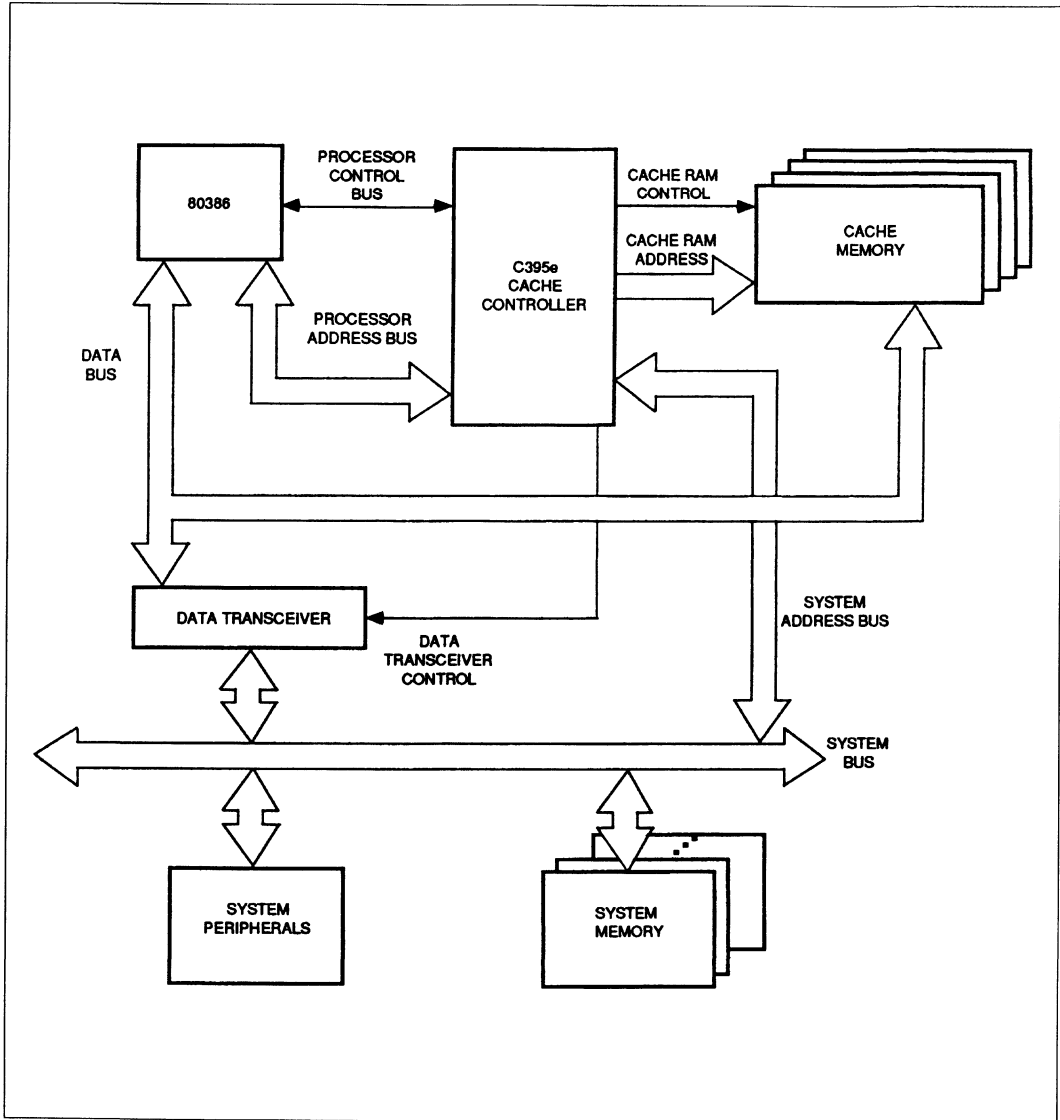
Block Diagram of a C385i-based Cache Sub-System

**DATA SHEET****M-82C395**

## ENHANCED VARIABLE-SIZE 32-BIT CACHE CONTROLLER

### FEATURES

- MOST HIGHLY INTEGRATED CONTROLLER FOR 386 AND 486 SYSTEMS
  - INTEGRATED SYSTEM INTERFACE, CPU INTERFACE, CACHE DIRECTORY, AND CACHE INTERFACE LOGIC
  - DIRECT INTERFACE TO 80386 CPU
  - COMPANION DEVICE (MDS-C415) FOR 80486 CPU
  - INTERFACES DIRECTLY TO INDUSTRY STANDARD HIGH-SPEED 16 K x 4, 8 K x 8 or 4 K x 16 STATIC RAMs, OR WITH 4 K x 16/18 AND 8 K x 16 CACHE RAMs
- MAPS THE FULL 4 GIGABYTE CPU ADDRESS SPACE
- 20, 25 AND 33 MHz OPERATION
- LARGE CACHE FOR BETTER HIT RATIOS FOR LARGER PROGRAMS, WITH MULTIPLE SIZE OPTIONS
  - 32 KB, 64 KB, 128 KB, and 256 KB in 386 CPU
  - 128 KB and 256 KB 486 CPU
- MULTIPLE CACHE MAPPING OPTIONS FOR BETTER HIT RATIO IN COMPLEX PROGRAMMING ENVIRONMENTS
  - DIRECT-MAPPED
  - 2-WAY SET-ASSOCIATIVE
  - 4-WAY SET-ASSOCIATIVE
- TWO OPTIONS FOR UPDATING MAIN MEMORY
  - WRITE-THRU, INCLUDING POSTED WRITE
  - COPY-BACK FOR IMPROVED SYSTEM BUS BANDWIDTH, ESPECIALLY USEFUL FOR DMA OPERATIONS ON SYSTEM BUS
- BUS SNOOPING FOR MAINTAINING COHERENCY WHILE ANOTHER BUS MASTER ACCESSES MAIN MEMORY LOCATIONS CURRENTLY IN CACHE
- FULL LRU REPLACEMENT ALGORITHM
- FLEXIBLE SUPPORT FOR NON-CACHEABLE MEMORY LOCATIONS
- ADVANCED CMOS TECHNOLOGIES  
0.8-MICRON CMOS TECHNOLOGY
- 164-LEAD JEDEC PQFP PACKAGE



Block Diagram of a Cache Sub-System using the C395e in an 80386-based System

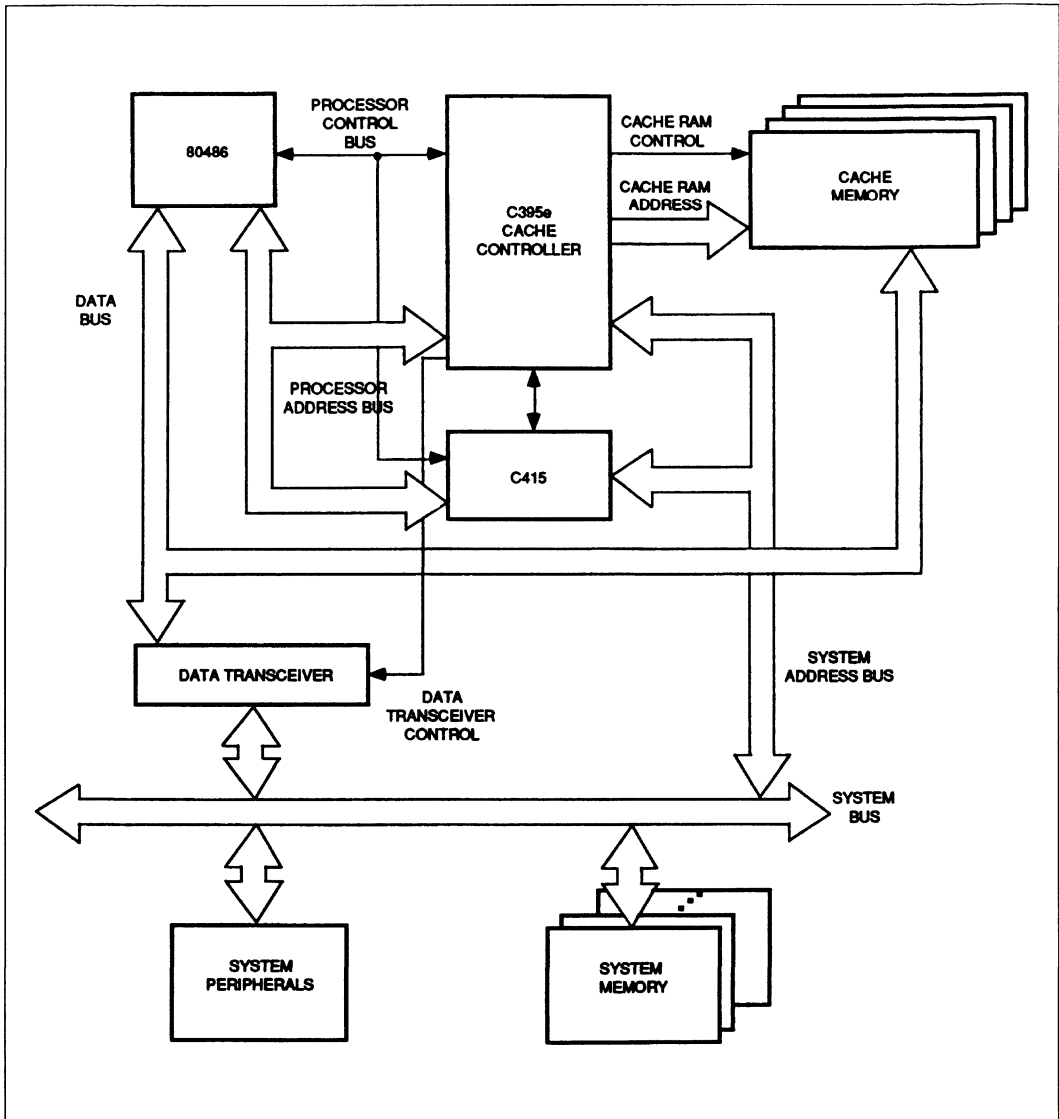
**DATA SHEET**

**M-82C415**

**80486/C395e INTERFACE  
ADAPTER**

**FEATURES**

- MOST OPTIMIZED AND HIGH-PERFORMANCE SOLUTION FOR EXTERNAL SECONDARY CACHE IN 80486 SYSTEMS
  - WORKS WITH THE M-82C395 CACHE CONTROLLER TO FORM A COMPLETE CACHE CONTROL SUBSYSTEM
- LARGE EXTERNAL CACHE SIZE OPTIONS FOR SIGNIFICANT IMPROVEMENT IN HIT RATIO
  - 128 KB AND 256 KB
- TWO OPTIONS FOR UPDATING MAIN MEMORY
  - COPYBACK AND WRITE-THRU
- COPYBACK SCHEME OPTIMIZED FOR SECONDARY CACHE IN HIGH-PERFORMANCE 80486 SYSTEMS
  - ABSORBS POSTED WRITE TRAFFIC GENERATED BY PRIMARY CACHE
  - PROVIDES SYMMETRIC PERFORMANCE IMPROVEMENT FOR READS AND WRITES
- 4-WAY SET ASSOCIATIVE MAPPING FOR BETTER HIT RATIOS IN COMPLEX ENVIRONMENTS SUCH AS MULTITASKING
  - CONSISTENT WITH MAPPING SCHEME OF 80486 INTERNAL CACHE
- DIRECT MAPPED AND 2-WAY SET-ASSOCIATIVE SCHEMES ALSO FULLY SUPPORTED
- GENERATES DIVIDED CLOCK FOR THE 80486 AS WELL AS BUFFERED 80386-TYPE 2X CLOCK FOR OTHER DEVICES
- GENERATES SYNCHRONIZED RESET FOR THE 80486 AND FOR 80386-TYPE DEVICES
- CONTAINS BURST MODE LOGIC FOR C395e
  - GENERATES CORRECT ADDRESS SEQUENCE FOR BURST ACCESSES
- SUPPORTS CACHE INVALIDATIONS IN THE PRIMARY CACHE
  - GENERATES NECESSARY SNOOP SUPPORT SIGNALS FOR 80486
  - PASSES ADDRESSES FROM SYSTEM BUS BACK TO THE 80486 FOR WRITE SNOOPS ON INTERNAL CACHE
- 20, 25 AND 33 MHz OPERATION
- PACKAGED IN 100-LEAD PQFP



Block Diagram of a Cache Sub-System using the C395e and C415 in an 80486-based System



# APPLICATION NOTES

**12**





## CMOS STATIC RAM

### TTL - CMOS INPUT - OUTPUT COMPATIBILITY

One of the feature of our CMOS static RAM is TTL compatibility. The inputs of CMOS Memories are not the same as the inputs found on TTL devices that most digital designers are familiar with.

If we look at our DC electrical characteristics, a parameter like  $V_{OH} = 2.4 \text{ V min.}$ , seems too high. The goal of this note is to define a method of interfacing for customer application.

#### TTL GATE CHARACTERISTICS

Figure 1 shows the electrical schematic of TTL and TTLG/S and TTL/S gates.

We shall mainly analyse TTL/CMOS interfacing : the approach for other families will be the same.

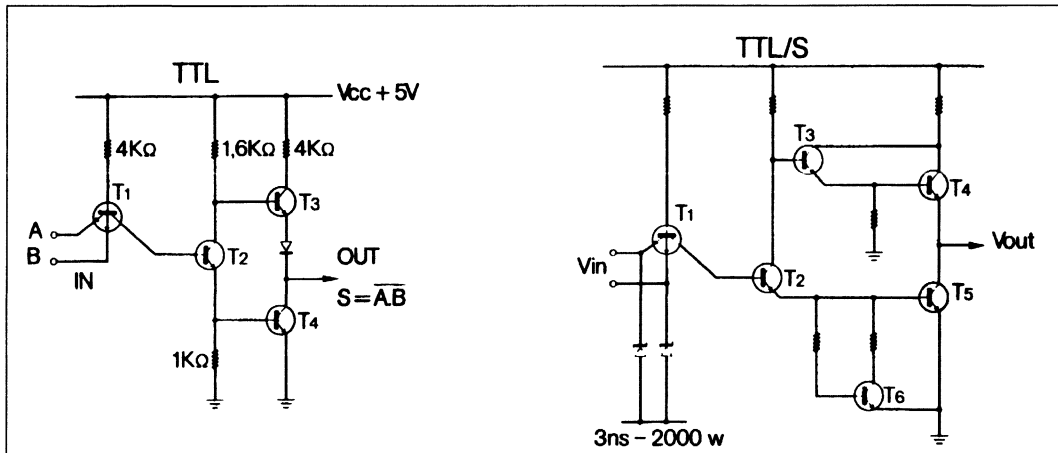


Figure 1.

#### 1. INPUT CHARACTERISTICS

##### 1.1 HIGH LEVEL (1) :

$V_{IH} \text{ min} = 2 \text{ V.}$

If we look at (figure 2), the only consumption is the emitter-base current of transistor T1. This  $I_{IH}$  current is in the range of  $40 \mu\text{A}$ .

##### 1.2. LOW LEVEL (0) :

$V_{IL} \text{ max} = 0.8 \text{ V.}$

Transistor T1 is now conducting and the consumption is in the range of  $1.6 \text{ mA}$ .



### 3.2 FAN-OUT

High level : If we look again at *fig. 3* we can see that the reversed bias of T1 can absorb 40  $\mu\text{A}$  and T3 can deliver a current  $1/3$  800  $\mu\text{A}$ .

Fanout at high level  $1/3 \frac{800}{40} 1/3 20$

Low level : T1 can deliver 1.6 mA, T4 can absorb 16 mA.

Fan-out at low level  $= \frac{16}{1.6} = 10$

THE FAN-OUT OF A TTL GATE IS 10.

Table 2.

| SERIES         | LOGIC LEVEL | INPUT CURRENT               | OUTPUT CURRENT                 |
|----------------|-------------|-----------------------------|--------------------------------|
| 54/74          | H<br>L      | 40 $\mu\text{A}$<br>1.6 mA  | 400/800 $\mu\text{A}$<br>16 mA |
| 54 H/74 H      | H<br>L      | 50 $\mu\text{A}$<br>2 mA    | 500 $\mu\text{A}$<br>20 mA     |
| 54 L/74 L      | H<br>L      | 10 $\mu\text{A}$<br>0.18 mA | 100 $\mu\text{A}$<br>2 mA      |
| 54 LS/74 LS    | H<br>L      | 20 $\mu\text{A}$<br>0.36 mA | 400 $\mu\text{A}$<br>5 mA      |
| 54 LS<br>74 LS | L           | 0.36 mA                     | 8 mA                           |
| 54 S/74 S      | H<br>L      | 50 $\mu\text{A}$<br>2 mA    | 1000 $\mu\text{A}$<br>20 mA    |

## CMOS GATE CHARACTERISTICS

(Fig. 4) shows a standard CMOS inverter.

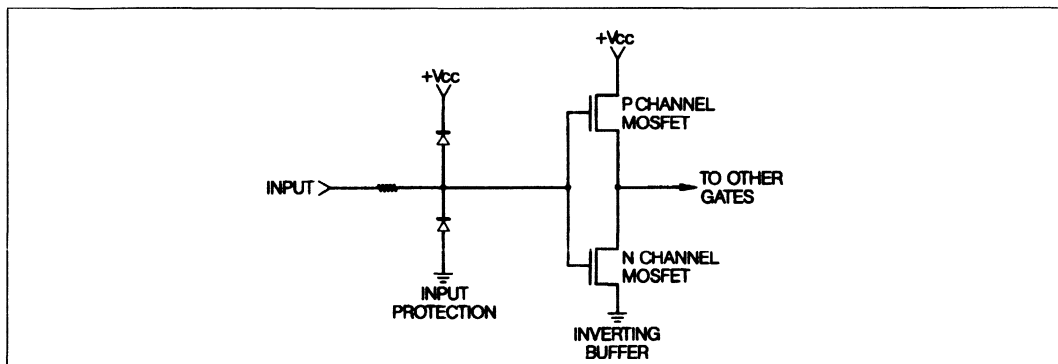


Figure 4.

Table 1.

| CHARACTERISTICS                                     | 54 S/74 S | 54 H/74 H | 54/74 | 54 LS/74 LS | 54 L/74 L | DTL | UNIT |
|-----------------------------------------------------|-----------|-----------|-------|-------------|-----------|-----|------|
| Power Supply                                        | 5         | 5         | 5     | 5           | 5         | 5   | V    |
| High Level Input VIH Min                            | 2         | 2         | 2     | 2           | 2         | 1.8 | V    |
| Low Level Input VIL Max                             | 0.8       | 0.8       | 0.8   | 0.8         | 0.7       | 1.1 | V    |
| High Level Output VOH Min for IOH Max               | 2.7       | 2.4       | 2.4   | 2.7         | 2.4       | 2.5 | V    |
| Low Level Output VOL Max for IOL Max                | 0.5       | 0.4       | 0.4   | 0.5         | 0.3       | 0.5 | V    |
| Lowest Noise Immunity (high level)                  | 700       | 400       | 400   | 700         | 400       | 500 | mV   |
| Highest Noise Immunity (low level)                  | 300       | 400       | 400   | 300         | 400       | 450 | mV   |
| Fan-out                                             | 10        | 10        | 10    | 10          | 10        | 8   |      |
| Maximum Power Dissipation (25°) with 50% Duty Cycle | 19        | 23        | 10    | 2           | 1         | 8   | mW   |
| Transition Time from Low to High Level              | 3         | 8         | 2     | 8           | 35        | 60  | ns   |
| Transition Time from High to Low Level              | 3         | 6         | 8     | 10          | 31        | 20  | ns   |
| Propagation Delay (average value)                   | 3         | 6         | 10    | 10          | 33        | 25  | ns   |
| Signal Rise Time                                    | 3         | 9         | 18    | 22          | 70        |     | ns   |
| Signal Fall Time                                    | 3         | 5         | 6     | 8           | 20        |     | ns   |
| Quality Factor                                      | 57        | 138       | 100   | 20          | 33        | 200 | pJ   |

The input circuit on CMOS devices is an inverting buffer stage with a protection network added against electrostatic discharge. A representative input buffer is shown in fig. 4. The FETs are both enhancement mode devices, which means that there is no current flow from the drain to the source unless the gate voltage is above threshold. With on P-FET and one N-PET in this complementary configuration, the output of the inverter is switched between Vcc and ground, but there is no current path from Vcc to ground because when one device is conducting the other device is biased off.

The input protection network protects the MOSFET gate dielectric from static damage. The purpose of the diodes is to clamp the input voltage of the gate. The gates are capacitive, so the resistor will cause an RC delay time to slow the rise of an applied potential and

give the diodes the time to turn on and protect the gates. The inverter will not allow any current to flow from Vcc to ground (except leakage current) because of the complementary design. With a low input voltage, VIL, the N-FET is biased off and the P-FET is on. The output is pulled high by the P-FET but no current flows directly from Vcc to ground. The opposite condition occurs with a high input. The N-FET is on the P-FET is off the output is pulled low, but there is still no direct current path from Vcc to ground. When an input is taken to an intermediate voltage, between 1.5 V and 3.5 V, both the N-FET and the P-FET will be partially conducting. There will be a dc path from Vcc to ground until the input is taken either high enough to fully bias off the P-FET, or low enough to turn off the N-FET.

## 1. INPUT CHARACTERISTICS

Like described above, whatever the level (high or low), there is no conduction between the gate and the source of a CMOS transistor.

The only consumption is a leakage current due to parasitic current caused by parasitic capacitance. The value of this current is very low :  $< 1 \mu\text{A}$ .

Whatever the temperature range and  $V_{CC}$  value we can say :

$$\begin{aligned} V_{IH} \text{ min.} &= V_{CC} - 2 \text{ V} \\ V_{IL} \text{ max.} &= 0.8 \text{ V} \end{aligned}$$

## 2. OUTPUT CHARACTERISTICS

### 2.1. HIGH LEVEL

We can compare a MOS transistor in a saturated state to a resistor. The resistance depends on the structure of the channel. (fig. 5)

The schematic of Fig. 5 shows the equivalent output circuit in a high state :  $VOH = V_{CC} - R_{DS1} \times I$ . Transistor T2 is biased off. The total current will depend on the value of  $R_{DS1}$ .

$$\begin{aligned} VOH &= V_{CC} - R_{DS1} \times I \\ \text{and} \\ R_{DS1} &= \frac{V_{CC} - VOH}{IO} = \frac{4.5 - 2.4}{10^{-3}} = 2.1 \text{ k}\Omega \\ R_{DS1} &= 2.1 \text{ K}\Omega \end{aligned}$$

#### Conditions when the loads is an other CMOS circuit

The only current that flows through  $R_{DS1}$  is the input leakage current of the second circuit :  $\approx 1 \mu\text{A}$ .

We can write :

$$\begin{aligned} V &= R_{DS1} \times I = 2.1 \times 10^3 \times 10^{-6} = 2.1 \text{ mV} \text{ and} \\ VOH &= 4.5 - 2.1 \times 10^{-3} = 4.4979 \text{ V} \\ VOH &\approx 4.50 \text{ V} \end{aligned}$$

$V_{IH}$  condition is :  $\geq V_{CC} - 2 \text{ V}$  ( $\geq 2.5 \text{ V}$ ).

**Conclusion :** no problem for CMOS interfacing at high level.

#### Conditions when the load is a TTL circuit

The current that flows through  $R_{DS1}$  will be the reverse junction current of T1 ( $\geq 40 \mu\text{A}$ ).

We can write :

$$\begin{aligned} V &= R_{DS1} \times I = 2.1 \times 10^3 \times 40 \cdot 10^{-6} = 84 \text{ mV} \\ \text{and } VOH &= 4.5 - 84 \times 10^{-3} = 4.416 \text{ V} \\ VOH &\approx 4.40 \text{ V} \end{aligned}$$

$V_{IH}$  condition is :  $\geq 2 \text{ V}$ .

**Conclusion :** no problem for TTL interfacing at high level. TTL noise immunity will not create any problems  $E_n > 400 \text{ mV}$  ( $4.416 - 2 = 2.416 \text{ V}$ ).

### 2.2 LOW LEVEL

The schematic of fig.6 shows the equivalent output circuit in a low stat.  $VOL = R_{DS2} \times I$ .

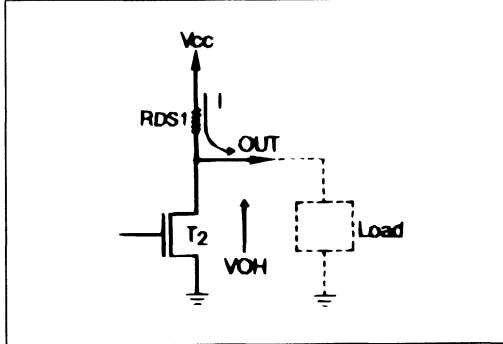


Figure 5.

If we look at the DC characteristics of a CMOS RAM (ex. 6514) for  $V_{CC} = 4.5 \text{ V}$ .

$VOH = 2.4 \text{ V}$  for  $IO = 1 \text{ mA}$  (load current).

We can easily deduce the value of  $R_{DS1}$  :

Transistor T1 is biased off; no current will flow through  $R_{DS2}$ , unless the load supplies this current.

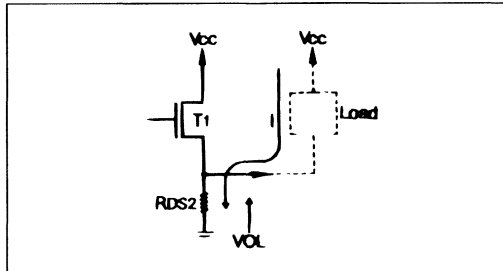


Figure 4.

If we look at the DC characteristic of CMOS RAM (6514 for example), for  $V_{CC} = 4.5 \text{ V}$ , we have :

$VOL = 0.45 \text{ V}$  for  $IO = 2 \text{ mA}$  and

$$R_{DS2} = \frac{0.45}{2 \cdot 10^{-3}} = 225 \Omega$$

#### Conditions when the load is an other CMOS circuit

The only current that flows through  $R_{DS2}$  is the leakage current of the second circuit :  $\approx 1 \mu\text{A}$ .

## DC ELECTRICAL CHARACTERISTICS (6514)

| SYMBOL | PARAMETER                     | TEMP. & $V_{CC}$<br>OPERATING<br>RANGE |                | TEMP. = 25°C1<br>$V_{CC} = 5.0$ V | UNIT    | TEST CONDITIONS                                  |
|--------|-------------------------------|----------------------------------------|----------------|-----------------------------------|---------|--------------------------------------------------|
|        |                               | MIN.                                   | MAX.           | TYPICAL                           |         |                                                  |
| ICCSB  | Standby Supply Current        |                                        | 50             | 1.0                               | $\mu$ A | $I_O = 0$<br>$V_I = V_{CC}$ or GND               |
| ICCOP  | Operating Supply Current 2    |                                        | 7              | 5                                 | mA      | $f = 1$ MHz, $I_O = 0$<br>$V_I = V_{CC}$ or GND  |
| ICCDR  | Data Retention Supply Current |                                        | 25             | 0.1                               | $\mu$ A | $V_{CC} = 2.0, I_O = 0$<br>$V_I = V_{CC}$ or GND |
| VCCDR  | Data Retention Supply Voltage | 2.0                                    |                | 1.4                               | V       |                                                  |
| II     | Input Leakage Current         | - 1.0                                  | + 1.0          | 0.0                               | $\mu$ A | $GND \leq V_I \leq V_{CC}$                       |
| IIOZ   | Input/Output Leakage Current  | - 1.0                                  | + 1.0          | 0.0                               | $\mu$ A | $GND \leq V_{IO} \leq V_{CC}$                    |
| VIL    | Input Low Voltage             | - 0.3                                  | 0.8            | 2.0                               | V       |                                                  |
| VIH    | Input High Voltage            | $V_{CC} - 2.0$                         | $V_{CC} + 0.3$ | 2.0                               | V       |                                                  |
| VOL    | Output Low Voltage            |                                        | 0.45           | 0.35                              | V       | $I_O = 2.0$ mA                                   |
| VOH    | Output High Voltage           | 2.4                                    |                | 4.0                               | V       | $I_O = - 1.0$ mA                                 |
| CI     | Input Capacitance 3           |                                        | 8.0            | 5.0                               | pF      | $V_I = V_{CC}$ or GND<br>:= 1 MHz                |
| CIO    | Input/Output Capacitance 3    |                                        | 10.0           | 6.0                               | pF      | $V_{IO} = V_{CC}$ or GND<br>:= 1 MHz             |

We can write :

$$VOL = R_{DS2} \times I = 225.10^6$$

$$VOL \approx 0,2 \text{ mV (negligible).}$$

VOL condition is  $\leq 0.8$  V.

**Conclusion** : no problem for CMOS interfacing at low level.

**Conditions when the load is a TTL circuit**

The current that flows through  $R_{DS2}$  will be the T1 transistor current (see fig. 6) of the TTL circuit. This current is in the range of  $\sim 1.6$  mA.

We can write :

$$VOL = R_{DS2} \times I = 225 \times 1.6.10 = 360 \text{ mV}$$

$$VOL = 360 \text{ mV.}$$

VIL condition is  $\leq 0.8$  V

**Conclusion** : no problem for TTL interfacing at low level with a noise immunity  $> 400$  mV  
( $800 - 360 = 440$  mV).

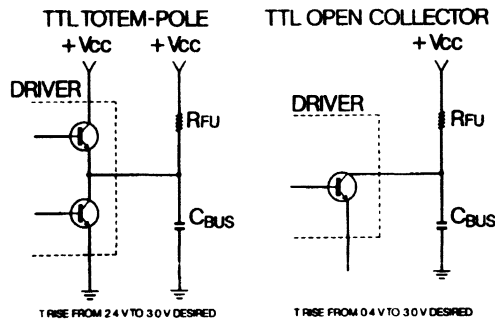


The CMOS static RAMS from MHS are :

- CMOS input/output, compatible with a CMOS noise immunity  $> 30\% V_{CC}$ .
- TTL output compatible with a TTL noise immunity  $\approx 400 \text{ mV}$ .
- TTL input compatible with pull-up resistors.

To guarantee high logic levels and noise margins, TTL buffers require external pull-up resistors. The value of the resistor is chosen by an RC based decision. The bus capacitance, and the allowable time for reaching  $V_{IH}$ , determine the resistor value. If the system speed is very slow, the pull-up resistor can be chosen to supply the bus leakage currents while maintaining a  $V_{IH}$  of at least 3.0 volts ( $V_{CC} = 2.0 \text{ volts}$ ). Figure 7 shows the basic circuit models and equation used.

(Fig. 7) - Choosing bus pull-up resistors.





## BATTERY BACK-UP SOLUTION AND APPLICATION

### SUMMARY

- USING A BATTERY WITH A VOLTAGE LESS THAN THAT OF THE MAIN POWER SUPPLY.
- BATTERY CHARGER USING A CONSTANT CURRENT SUPPLY WITH AUTOMATIC CUT-OFF AT FULLCHARGE.
- PROTECTION AGAINST MAIN POWER SUPPLY FAILURE.

### I - DESCRIPTION OF BATTERY BACK-UP SYSTEM

#### 1.1 BLOCK DIAGRAM

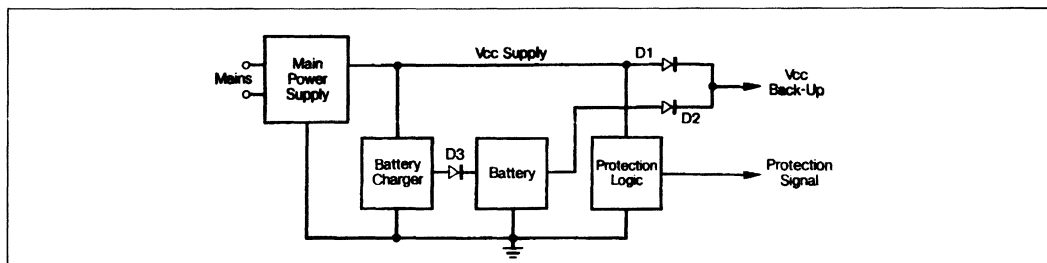


Figure 1.

#### 1.2 BATTERY CHARGER

##### A - DESCRIPTION

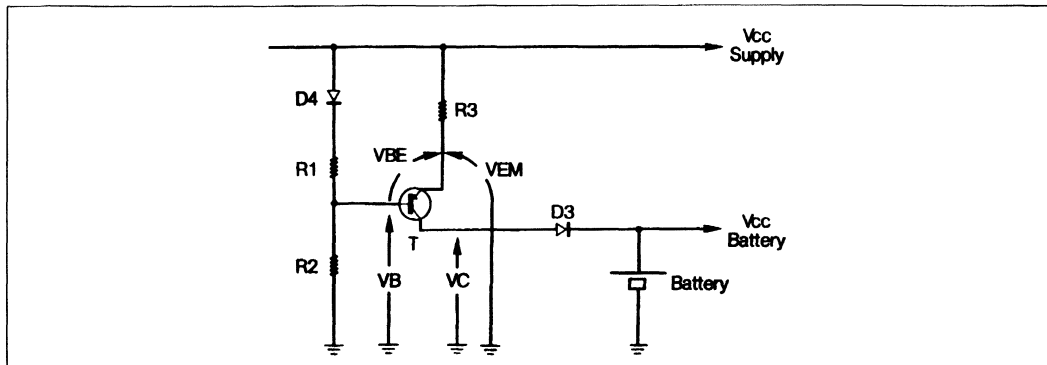


Figure 2.

## B - OPERATION

The charger is composed of a current generator formed by the transistor T (PNP) and its biasing components. The diode (D4) and resistors (R1, R2) fix the base voltage (VB) to the output voltage of the battery. The current that flows in the chain is of the order of 5 mA. The emitter voltage of the transistor (VE) :  
 $VE = VBE + VB$  ( $VBE = 0.6\text{ V}$ ).  
 Resistor R3 determines the charging current which, in turn, is dependent upon the battery characteristics. The

diode (D4) compensates for  $\Delta VBE$  of the transistor with temperature changes.

The battery charges until  $VC \approx VE$ , where cut-off occurs.

The germanium diode, D3 (having a low voltage-drop), isolates the battery from the charger.

Diodes D1 and D2 (also germanium), isolate the battery and the main power supply from each other.

## 1.3 PROTECTION AGAINST POWER-OFF AND POWER-ON

### A - OVERVIEW

#### • Poweroff

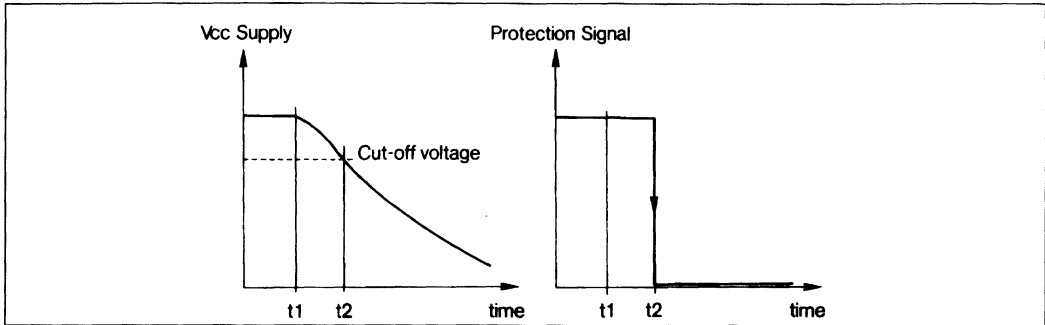


Figure 3.

During power-off conditions the protection signal must be active from the time the main power supply voltage drops below the limiting threshold, which is fixed by the

cut-off circuitry. This will depend upon the components used.

#### • Power-on

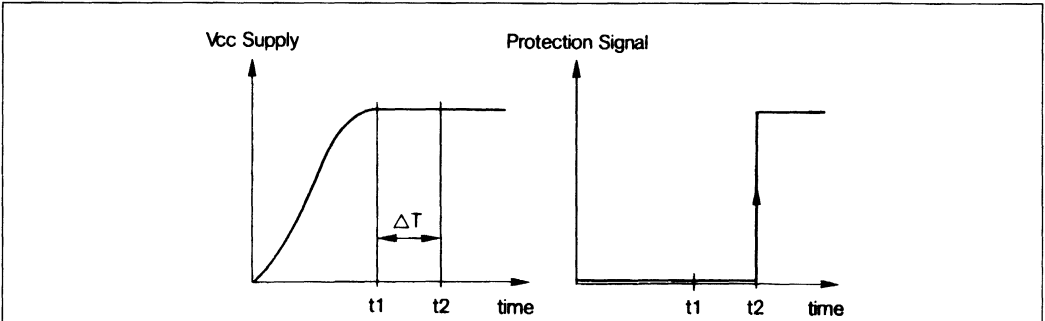


Figure 4.

At power-on the protection signal must be active until the main power supply is stable. Any random functioning must be avoided. The time  $\Delta T$  allows a safety margin.

#### • Introduction

The only stable reference during power supply transi-

tions is ground, hence the protection signal is active low.

The protection logic is not powered by the battery so as to reduce the current drawn to a minimum.

The protection logic must have a good noise immunity (CMOS advised) so that it is not affected by any disturbances.

The threshold value must not be too close the power supply voltage (to allow voltage fluctuations) nor too

close to ground to cause failure of circuits that are not adequately supplied.

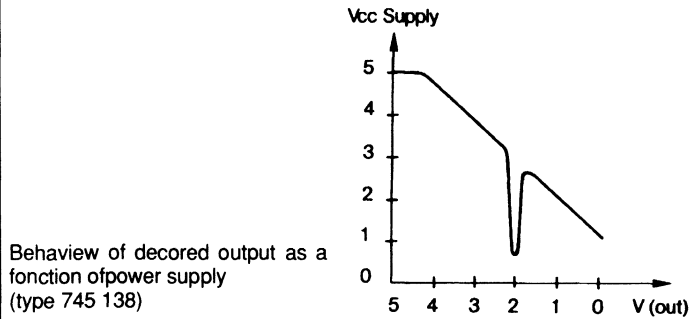


Figure 5.

## B - CIRCUIT OVERVIEW

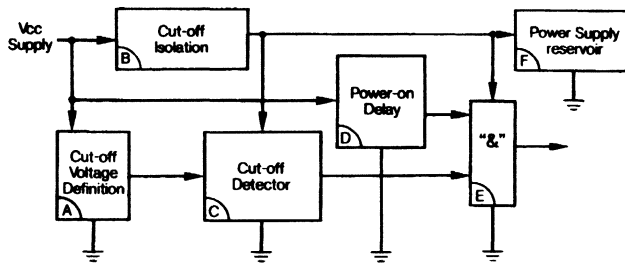


Figure 6.

The system is constructed around a Schmidt trigger (c) built using PNP transistors. This triggers around the cut-off voltage defined by circuitry (A). A power supply reservoir (F) allows the detector to continue operating under normal conditions. The supply isolation (B) stops

the rest of the circuitry from draining the supply reservoir (F) when the power is cut-off. The protection signal is obtained by an "AND" (E) between the signals provided by the cutoff detector (C) and the power-on delay (D). This is a low power CMOS gate.

## C - CIRCUIT DIAGRAM

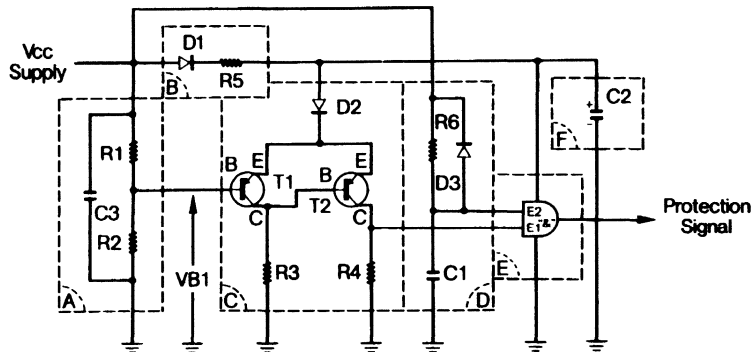


Figure 7.

### • Normal operation

Transistor T1 is cut-off, its base voltage being higher than its switching threshold.

$$\begin{aligned}\text{Switching threshold} &= \text{VCC Supply} - \text{VD1} - \\ &\quad \text{VD2} - \text{VBE1} \\ &= \text{VCC Supply} - 0,9 \text{ V}\end{aligned}$$

The quiescent base voltage, VB1, is fixed around the limiting power supply voltage during power-off (cut-off voltage : VCP).

So that :

$$\text{VB1} = \frac{\text{VCC Supply} (\text{VCC Supply} - \text{VEB1} - \text{VD2} - \text{VD1})}{\text{VCP}}$$

Since T1 is not conducting, the base of T2 is pulled towards ground across R3, hence the transistor T2 turns on and becomes saturated.

$$\text{VE2} = \text{VCC} - \text{VD1} - \text{VD2}$$

$$\text{VB2} = \text{VE2} - \text{VBE2}$$

$$\text{VR4} = \text{VCC Supply} - \text{VD1} - \text{VD2} - \text{VCE2}$$

### • Power off

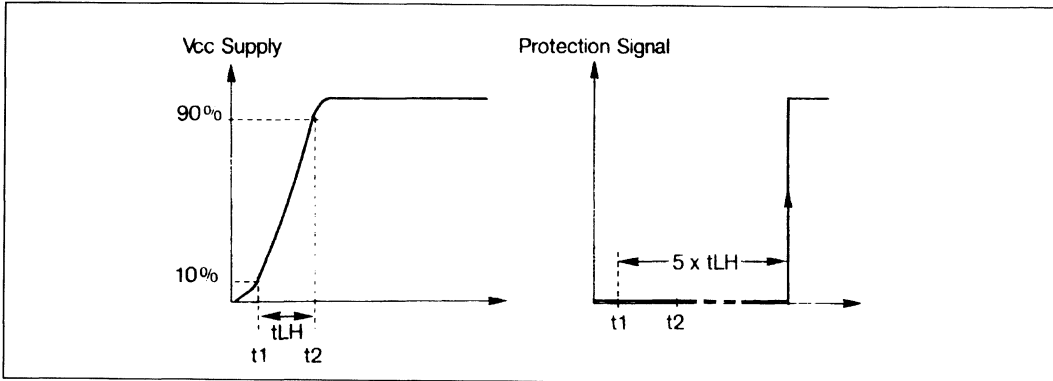
VCC Supply falls and reaches the limiting voltage VCP. The trigger threshold is reached so that T1 saturates. VR3 increases cutting off T2. The input E1 of the "AND" gate is at logic zero so that the protection signal becomes active. The supply reservoir, C2, maintains the emitter voltage levels until cut-off detection. It discharges across the equivalent resistance Req.

$$\text{Req} = \frac{\text{VC2}}{\text{IC1}} \quad \text{where } \text{IC1} \approx \text{IE1} \approx \text{IE2}$$

### • Power on

The protection signal depends only upon the network formed by R6 and C1. ( $\text{R6.C1} \geq \text{risetime of the power supply, VCC Supply}$ ). This network introduces a delay.

$$= \text{R6.C1} = 5.t_{\text{LH of VCC Supply}}$$



**Figure 8.**

The diode in parallel with R6 (D3) discharges C1 during power-off. It also the system to react efficiently when-

ever the power-off period is less than the time constant  $\text{R6.C1}$ .

## II - APPLICATION USING A 16K BYTE MEMORY BLOCK WITH BATTERY BACK-UP

### 2.1 PRESENTATION

This application allows :

- Selection of a single 2Kx8 RAM of a 16K byte block located in a 64K byte page.
- Access time of 140 nS (time between a read request and the data).
- Decoder protection during power-on and power-off.
- Constant current battery charger with automatic cut-off at full charge.
- Data retention of one month with a battery of 100 mAH.

### 2.2 COMPONENTS USED

#### A - MEMORY

2K byte static asynchronous CMOS RAMs, ref. HM651615 (see appendix 2).

#### B - MEMORY DECODER

3.8 CMOS decoder, ref. HD-6440 (see appendix 2).

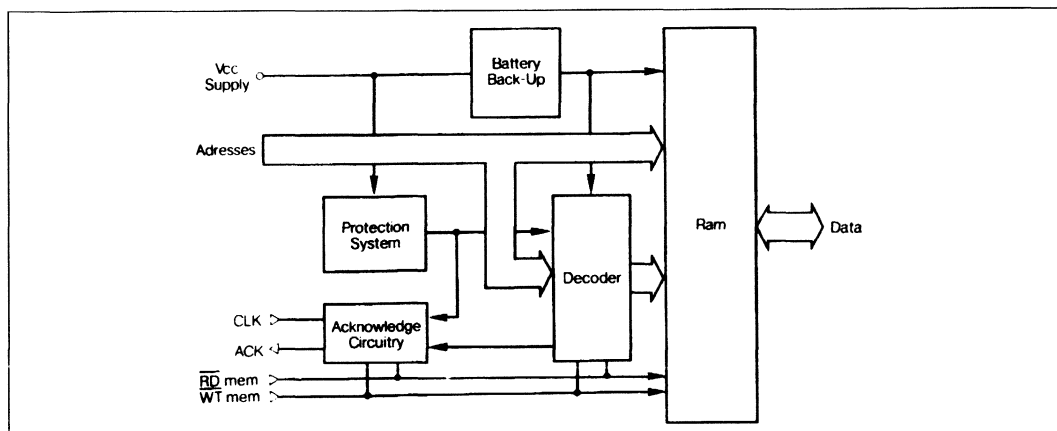


Figure 9.

**C - BATTERY** Capacity 100 mAh  
Charge current 4 mA Voltage output 2 ↔ 4.65 V

### 2.3 BATTERY BACK-UP SYSTEM

#### A - CIRCUIT DIAGRAM

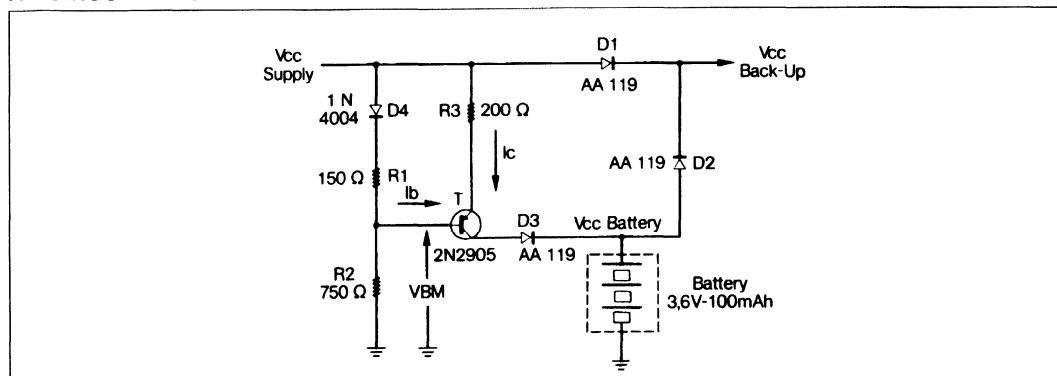


Figure 10.

**B - OPERATION**

- Biasing of transistor (type 2N2905)

VB = battery E.M.F. = 3.6 V

Ip = 5 mA (current necessary in D4)

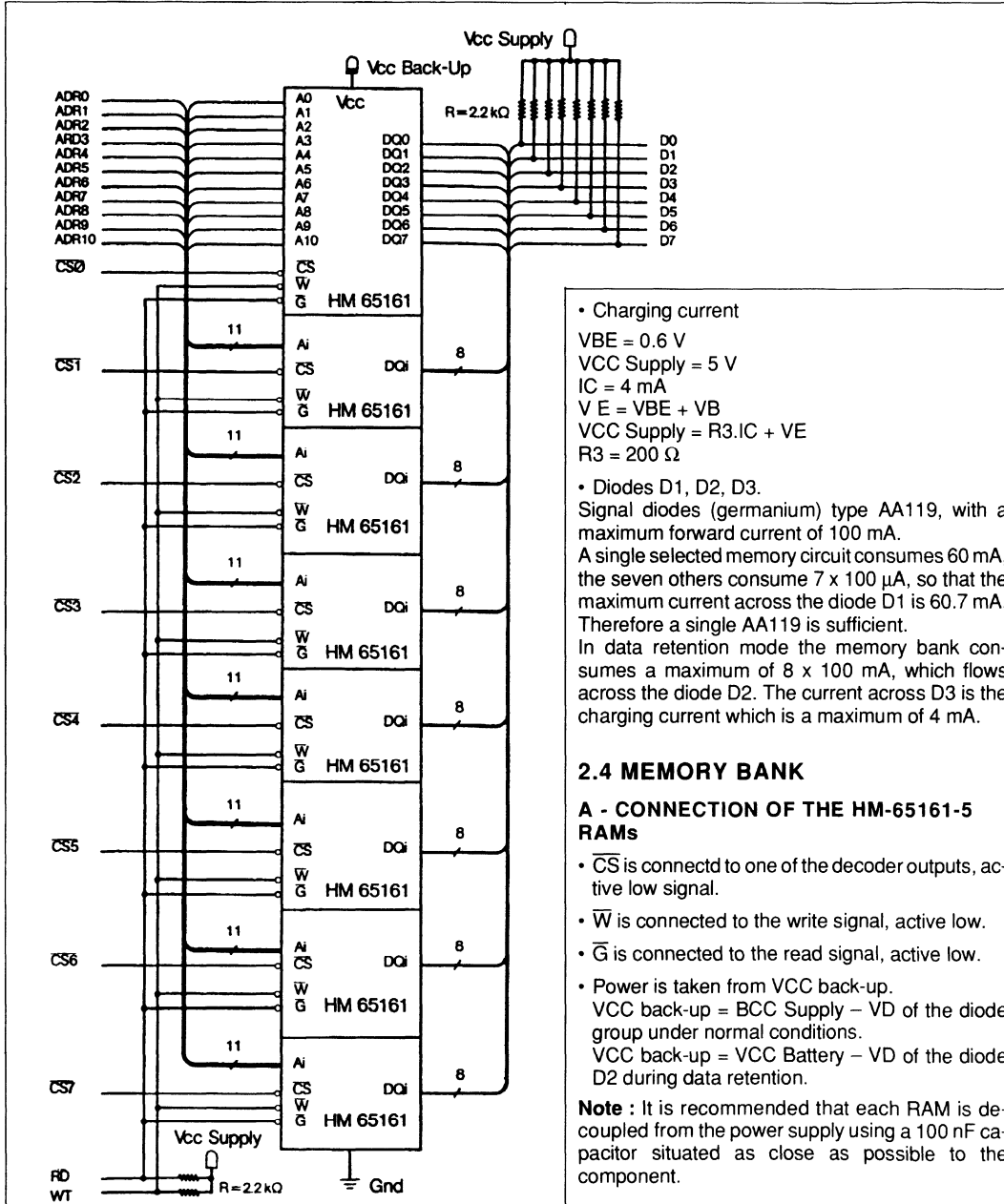
Diode voltage drop = 0.6 V (type 1N4004)

VCC Supply = 5 V

VCC Supply = VD + (R1 + R2), Ip (IB negligible)

VB = R2.Ip

R2 = 750 W R1 = 150 W





### B - MEMORY BANK PROTECTION

- A study of the architecture of the HM-65161-5 RAM indicates that the CS signal must be protected during the switch from normal operation and back-up operation.
- The  $\overline{G}$  and  $\overline{W}$  inputs do not require any special attention.

### C - RISING EDGE IMPROVEMENT

- The data bus and the read/write lines are pulled up to VCC Supply by resistors.

Capacitive load on these lines :  $8 \times 5 \text{ pF} = 40 \text{ pF}$

Pull-up resistor value :  $2.2 \text{ k}\Omega$

(Application Note : 1006)

- The addresses appear earlier than the other signals, so pull-up resistors are not necessary on these lines.

## 2.5 DECODING

### A - USING THE HD-6440 DECODER

- The latch ( $\overline{L1}$ ,  $\overline{L2}$ ) is not used. So that  $\overline{L1} = '0'$  and  $\overline{L2} = 1$ .

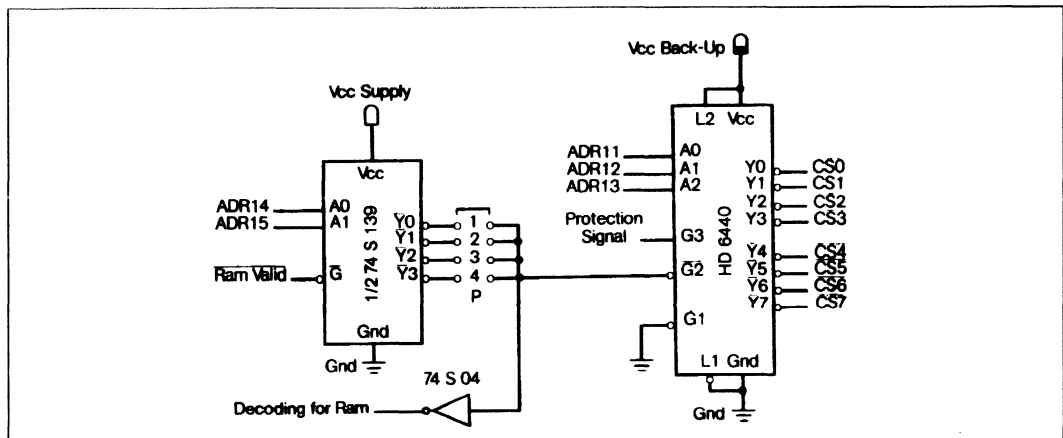


Figure 12.

## 2.6 PROTECTION SYSTEM

### A - CHARACTERISTICS OF THE CONSTRUCTED SYSTEM

- VCC Supply =  $5 \text{ V} \pm 5\%$
- During power-off the time for the voltage to fall be-

- The outputs of the decoder are used to select the RAMs ( $\overline{CS}$ ), therefore it is sufficient to disable the decoder to deselect the memory bank. To do this protection signal is connected to the G3 input of the decoder ; it is also necessary to safeguard the decoder power supply.
- The ground (logic zero level) being the only reference for the two supplies (VCC Supply, VCC Battery), it is sufficient to apply this signal to the G3 input to deselect both the decoder and the RAM.
- $\overline{G2}$  = Selection (active low) of the memory bank.

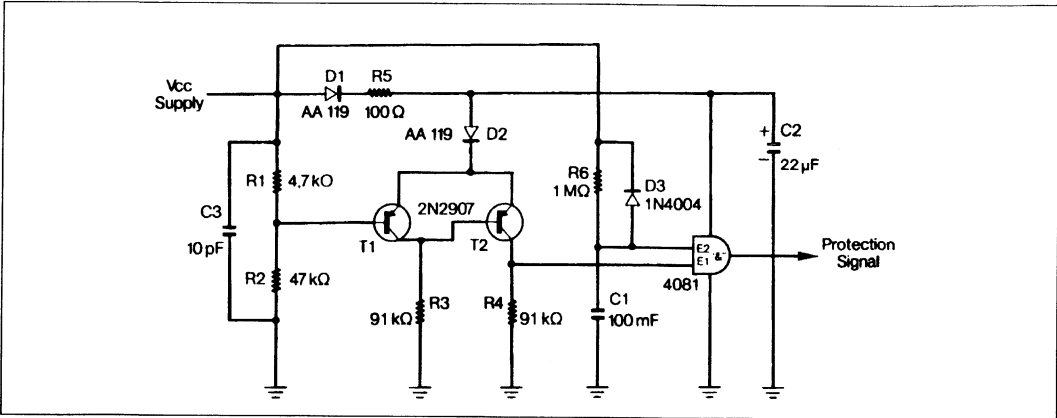
### B - SELECTION OF A MEMORY BANK WITHIN A 64K BYTE PAGE

- Using a 2 → 4 line decoder (type 74-S-139)
- Selection of memory bank address within a 64K byte page by jumpers.
- Selection of the decoder if the RAM valid signal is active.

tween VCC Supply and 37 % of this value is 240 mS.

- During power-on the risetime between 10 % to 90 % of VCC Supply is 20 mS.
- The cut-off voltage was chosen to be 4.5 V.

## B - CIRCUIT DIAGRAM



## C - OPERATION

- Input stage, (T1, R1, R2, R3, D1, D2, D5) D1 and D2 fix the potential VE of transistor T1 (VR5 negligible VE = VCC Supply VD1 VD2 = 4.7 V). The current IC1 of T1 is chosen to be small, IC1 ≈ 50 μA, to have low power consumption and to obtain a small value of C2, the reservoir capacitor. The chain R1 and R2 fixes the threshold of the trigger.

$$VB1 = \frac{VCC \text{ Supply} (VCC \text{ Supply} - VD1 - VD2 - VBE1)}{VCP}$$

$$= 4.55 \text{ V}$$

The current across R1 and R2 must be greater than IB1.

$$IR1 \approx 100 IB1 \Rightarrow IR1 \approx IR2$$

$$IB1 \approx 1 \mu A \Rightarrow IR1 \approx 100 \mu A$$

**Note :** If  $IR1 \geq IB1$  the noise immunity will be greater because the circuit is voltage sensitive. The capacitor C3 permits filtering of VB1.

$$R1 + R2 = \frac{VCC \text{ Supply}}{IR1} = \frac{5}{100 \times 10^{-6}} \quad R1 + R2 = 50 \text{ K}\Omega$$

$$R2 = \frac{VB1}{IR2} = \frac{4.5}{100 \times 10^{-6}} = 45.5 \text{ k}\Omega$$

$$R2 = 45.5 \text{ k}\Omega \text{ standardised to } 47 \text{ k}\Omega$$

$$R1 = 4.5 \text{ k}\Omega \text{ standardised to } 4.7 \text{ k}\Omega$$

$$R3 = \frac{VE - VCE1}{IC1} = \frac{4.7 - 0.2}{50 \times 10^{-6}} = 90 \text{ k}\Omega$$

$$R3 = 90 \text{ k}\Omega, \text{ standardised to } 91 \text{ k}\Omega.$$

Capacitor C3 serves as a small filter and has a value of 10 pF.

Resistor R5 limits the current through diode D1 that charges C2.

$$R5 = 100 \Omega$$

- Operation of the output stage (R4).

The current IC2 of transistor T2 is also small to keep consumption low and limit the value of C2. IC2 ≈ 50 μA.

$$R4 = \frac{VE - VCE2}{IC2} = \frac{4.7 - 0.2}{50 \times 10^{-6}} = 90 \text{ k}\Omega$$

$$R4 = 90 \text{ k}\Omega, \text{ standardised to } 91 \text{ K}\Omega.$$

Under normal operation : VR4 ≈ R4. IC2 = 4.5 V

Therefore VR4 effectively corresponds to a logic one level for the E2 input of the 'AND' gate.

- Voltage reservoir operation.

Capacitor C2 charges via D1 and R5. Whenever VCC Supply falls, C2 supplies power for the system. Diode D1 cuts off and isolates C2 from the main power supply. C2 discharges across T1 and R3, other components drawing a negligible current.

$\tau$  = time constant for the power supply cut-off ( $\tau = 240 \text{ mS}$ ).

$$VE = VCC \text{ Supply} \quad VD1 \quad VD2 = 4.7 \text{ V}$$

$$VCP = 4.5 \text{ V}$$

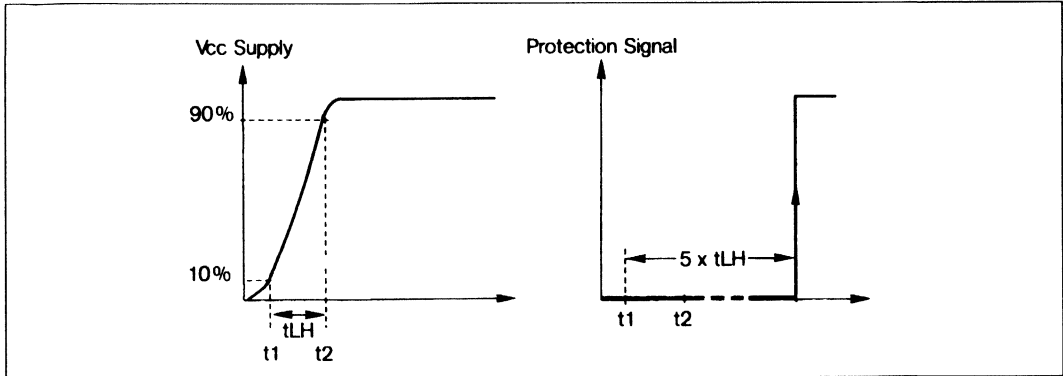
$$IC1 = 50 \mu A$$

$$VEB = 0.6 \text{ V}$$

$$C2 = \frac{0.9 \tau IC1 (1 - \frac{VCP}{VCC})}{VE - VBE - 0.9 VCP}$$

$$C2 = 20.9 \mu F, \text{ standardised to } 22 \mu F$$

### • Poweron delay operation



$t_{LH} = 20 \text{ mS} \Rightarrow \Delta t = 100 \text{ mS}$

$V_B$  : Logic one level, guaranteed for a 4081 AND gate, of 2.75 V.

$V_{SS}$  : Power supply for R6, C1

$V_{SS} = V_{CC} \text{ Supply } V_{D1} = 4.85 \text{ V.}$

$$V_B = V_{SS} \left( 1 - e^{-\frac{\Delta T}{R6 \cdot C1}} \right)$$

$$R6 \cdot C1 = \frac{\Delta T}{\text{Loge} \left( \frac{V_{SS}}{V_{SS} - V_B} \right)} = 0.12 \text{ S}$$

If  $C1 = 100 \text{ nF}$ ,  $R6 = 1 \text{ M}\Omega$ .

The discharge current of C1 having a large peak, D3 must be of the type 1N4004.

### D MODIFICATIONS FOR IMPROVED TEMPERATURE STABILITY

The circuit, as it is at present, can have temperature related problems which show themselves by a shift of  $\approx 180 \text{ mV}$  of VCP (cut-off voltage) at  $50^\circ \text{C}$ .

In this case a greater precision is necessary for VCP, the initial circuit must be modified.

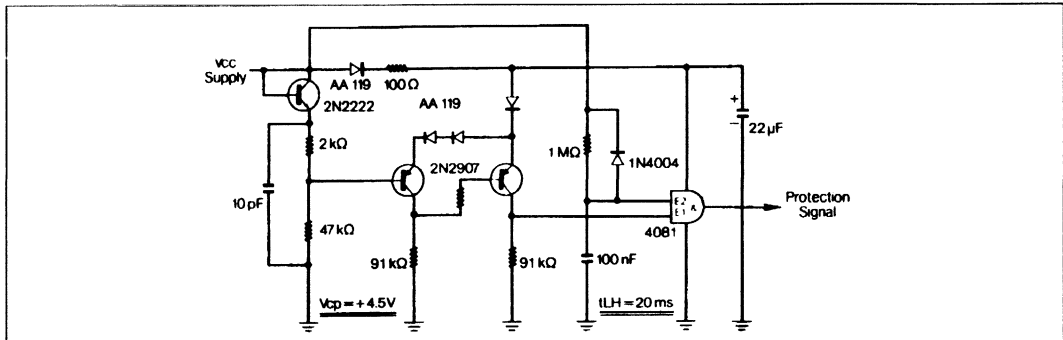


Figure 14.

## 2.7 RAM ACCESS ACKNOWLEDGE

### A - NECESSARY CONDITIONS

- To have decoded the memory address
- To be in read or write operation
- To be not in the state where RAM is disabled and/or protected

The signal obtained must be sent to the bus line ( $\overline{\text{ACK}}$ ), allowing the system controller to complete the cycle.

### B - DELAY OF ACKNOWLEDGE

If compatible slow memories are used (HM-6516) it may be necessary to delay the ACK signal with certain high-speed microprocessors.

### 3. CONCLUSION

The method used may also be applied to other CMOS memories and other decoding systems.

The application of a 16K byte memory block can be extended to have greater capacity for 8, 16 or 32 bit data buses. A recalculation of certain parameters will be necessary.

To delay the sending of ACK a counter is used in con-

junction with CLK. The counter is enabled whenever a read or write to memory occurs.

The use of a non-rechargeable battery (such as lithium cells) is also possible, having a life of several years. In this case the circuit becomes simpler because the charger is no longer required.

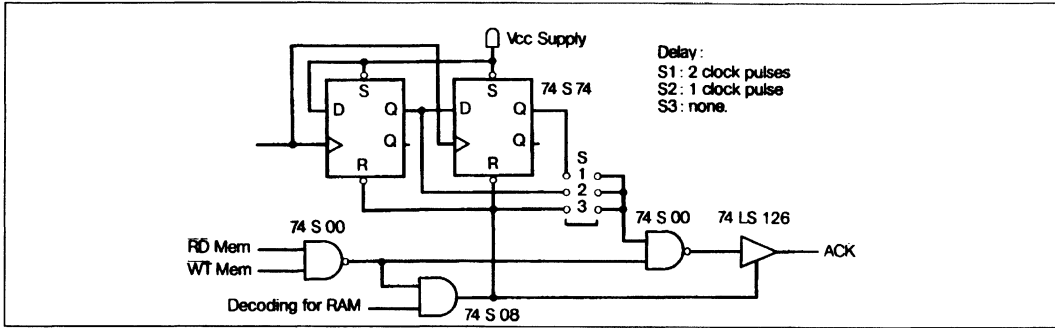


Figure 15.

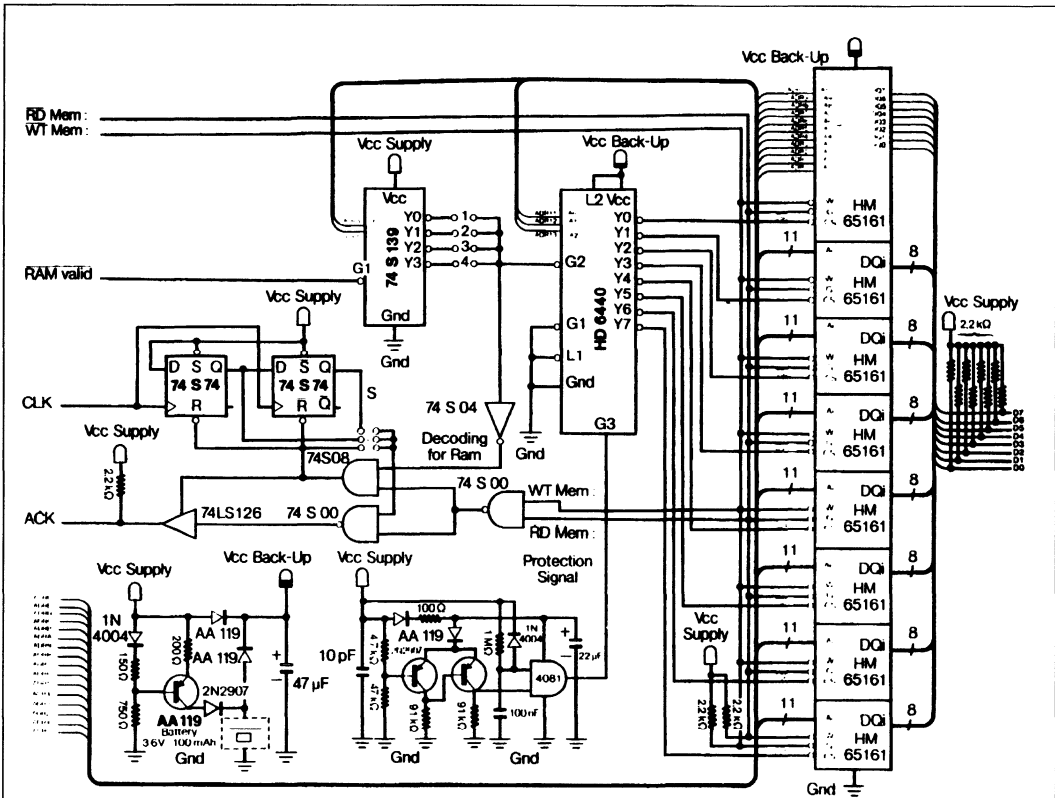


Figure 16.

# PACKAGING

13







## PACKAGING

### PRODUCT REFERENCES

| DEVICE TYPE | PINS COUNT | PDIL 300 MILS | PDIL 600 MILS | CDIL 300 MILS | CDIL 600 MILS | SOIC | LCC | PLCC | SOJ |
|-------------|------------|---------------|---------------|---------------|---------------|------|-----|------|-----|
| 65687       | 22p        | 054           | —             | C33           | —             | *    | *   | —    | *   |
| 65688       | 22p        | 054           | —             | C33           | —             | *    | *   | —    | *   |
| 65664       | 28p        | 051           | 033           | C31           | C32           | N10  | L32 | —    | P03 |
| 65767       | 20p        | 034           | —             | C23           | —             | N01  | L20 | —    | —   |
| 65768       | 20p        | 034           | —             | C23           | —             | N01  | L20 | —    | —   |
| 65770       | 22p        | 053           | —             | C33           | —             | N02  | —   | —    | —   |
| 65772       | 24p        | 043           | —             | C29           | —             | N02  | —   | —    | —   |
| 65728       | 24p        | 043           | 03            | C25           | —             | N02  | L17 | —    | —   |
| 65787       | 22p        | 041           | —             | C33           | —             | N02  | L23 | —    | P02 |
| 65788       | 22p        | 041           | —             | C33           | —             | N02  | L23 | —    | P02 |
| 65789       | 24p        | 044           | —             | C29           | —             | N02  | L15 | —    | P02 |
| 65790       | 28p        | 049           | —             | C31           | —             | N10  | L15 | —    | *   |
| 65791       | 28p        | 049           | —             | C31           | —             | N10  | L15 | —    | *   |
| 65764       | 28p        | 049           | 050           | C31           | C32           | N10  | L32 | —    | P03 |
| 65779       | 28p        | 049           | —             | —             | —             | N10  | —   | —    | P03 |
| 65262       | 20p        | X8            | —             | C1            | —             | —    | L22 | —    | —   |
| 65162       | 24p        | —             | X3            | —             | 5F            | —    | L17 | —    | —   |
| 65641       | 28p        | —             | X33           | —             | C20           | —    | L32 | —    | —   |
| 6116        | 24p        | —             | X3            | —             | 5F            | —    | LU  | —    | —   |
| 65161       | 24p        | —             | X3            | —             | 5F            | —    | LU  | —    | —   |
| 6207        | 40p        | —             | 3J            | —             | 5H            | —    | L09 | K04  | —   |
| 65231       | 48p        | —             | 036           | —             | C21           | —    | L04 | K01  | —   |
| 65797       | 24p        | 058           | —             | C37           | —             | N12  | L24 | —    | P05 |
| 65798       | 24p        | 058           | —             | C37           | —             | N12  | L24 | —    | P05 |
| 65799       | 28p        | 056           | —             | C36           | —             | N11  | L24 | —    | P04 |
| 65795       | 28p        | 056           | —             | C36           | —             | N11  | L24 | —    | P04 |
| 65796       | 28p        | 056           | —             | C36           | —             | N11  | L24 | —    | P04 |
| 65756       | 28p        | 056           | X33           | C36           | C20           | N11  | L24 | —    | P04 |
| 65783       | 52p        | —             | —             | —             | —             | —    | —   | K24  | —   |
| 65784       | 52p        | —             | —             | —             | —             | —    | —   | K24  | —   |
| 65656       | 28p        | *             | *             | *             | *             | —    | *   | —    | —   |
| 65697       | 24p        | *             | —             | *             | —             | —    | *   | —    | —   |
| 65698       | 24p        | *             | —             | *             | —             | —    | *   | —    | —   |

| DEVICE TYPE | PINS COUNT | PDIL 300 MILS | PDIL 600 MILS | CDIL 300 MILS | CDIL 600 MILS | SOIC | LCC | PLCC | SOJ |
|-------------|------------|---------------|---------------|---------------|---------------|------|-----|------|-----|
| 67024       | 84p        | —             | —             | —             | —             | —    | L85 | K06  | —   |
| 67201       | 28p        | 049           | —             | C31           | —             | N03  | L01 | —    | —   |
| 67202       | 28p        | 049           | —             | C31           | —             | N03  | L01 | —    | —   |
| 65864       | 28p        | *             | —             | *             | —             | —    | —   | —    | *   |
| 65888       | 22p        | *             | —             | *             | —             | —    | —   | —    | *   |
| 65889       | 24p        | *             | —             | *             | —             | —    | —   | —    | *   |

For Dual port ram 67024 : PGA (G19) and CQPJ (Q05) also available.  
 \* Consult sales office

#### STANDARD NOTES FOR PLASTIC D.I.L.

- 1 - Controlling dimensions : inches  
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.
- 2 - Dimensioning and tolerancing per ansi y 14.5M-1982.
- 3 - Dimensioning A.A1. and L are measured with the package seated in jedec seatind plane gauge GS-3.
- 4 - D and E1 dimensions do not include mold flash or protusions. Mold flash or protusions shall not exceed .010 inch (0.25 mm).
- 5 - E and eA measured at the leads constrained to be perpendicular to the base plane.
- 6 - eB is measured at the lead tips with the leads unconstrained.
- 7 - Corner leads may be configured as shown in figure 2.

#### STANDARD NOTES OR CERAMIC D.I.L.

- 1 - Controlling dimensions : inches.  
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.
- 2 - Dimensioning and tolerancing per ansi y 14.5M-1982.
- 3 - Dimensions A.A1. and L are measured with the package seated in jedec seatind plane gauge GS-3.
- 4 - E and eA measured at the leads constrained to be perpendicular to the base plane.
- 5 - eB is measured at the lead tips with the leads unconstrained.
- 6 - Corner leads may be configured as shown in figure 2.
- 7 - Leads within 0.127 radius of true position at gauge plane with MMC (maximum material condition) and unit installed.

#### STANDARD NOTES FOR PLCC

- 1 - Controlling dimensions : inches.  
In case of conflict or interpretation between the english and metric tabulation, the inch dimensions are controlling.
- 2 - Dimensioning and tolerancing per ansi y 14.5M-1982.
- 3 - D and E1 dimensions do not include mold flash or protusions. Mold flash or protusions shall not exceed 0.25 mm (.010 inch).

#### STANDARD NOTES FOR S.O.

- 1 - Controlling dimensions : mm.
- 2 - Dimensioning and tolerancing per ansi y 14.5M-1982.
- 3 - D is a reference datum.
- 4 - A and B are reference datums and do not include mold flash or protusion. Mold flash and protusions shall not exceed 0.15 mm (.0086 inch).
- 5 - The chmfer h on the body is optional.

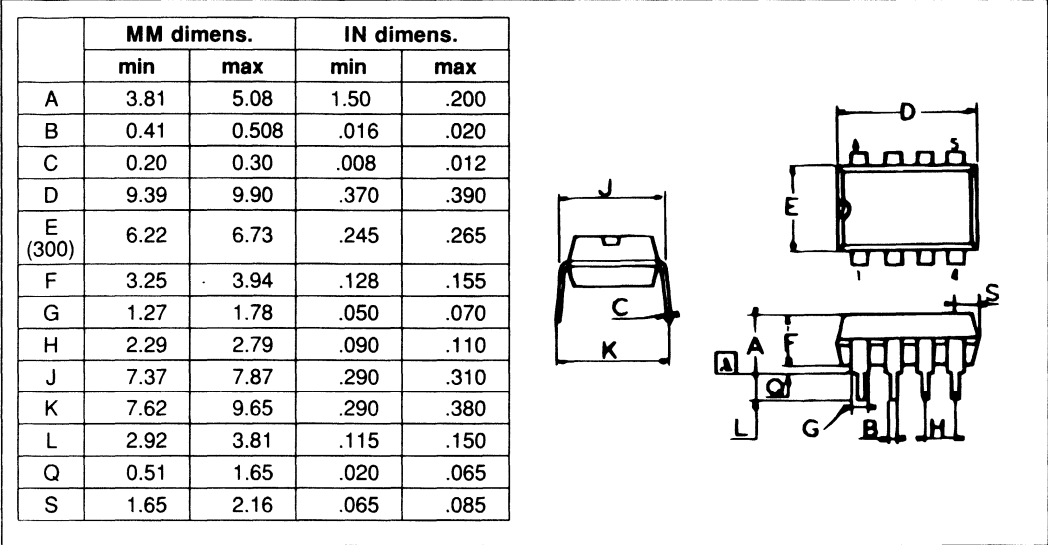
#### STANDARD NOTES FOR SO TYPE J

- 1 - Controlling dimensions : inches.
- 2 - Dimensioning and tolerancing per ansi y 14.5M-1982.
- 3 - Dim eA to be determine at seating plane .DATUM C.
- 4 - D and E dimensions do not include mod flash or protusions. Mold flash or protusions shall not exceed 0.15 mm (.006 inch).
- 5 - The chamfer h is optional.



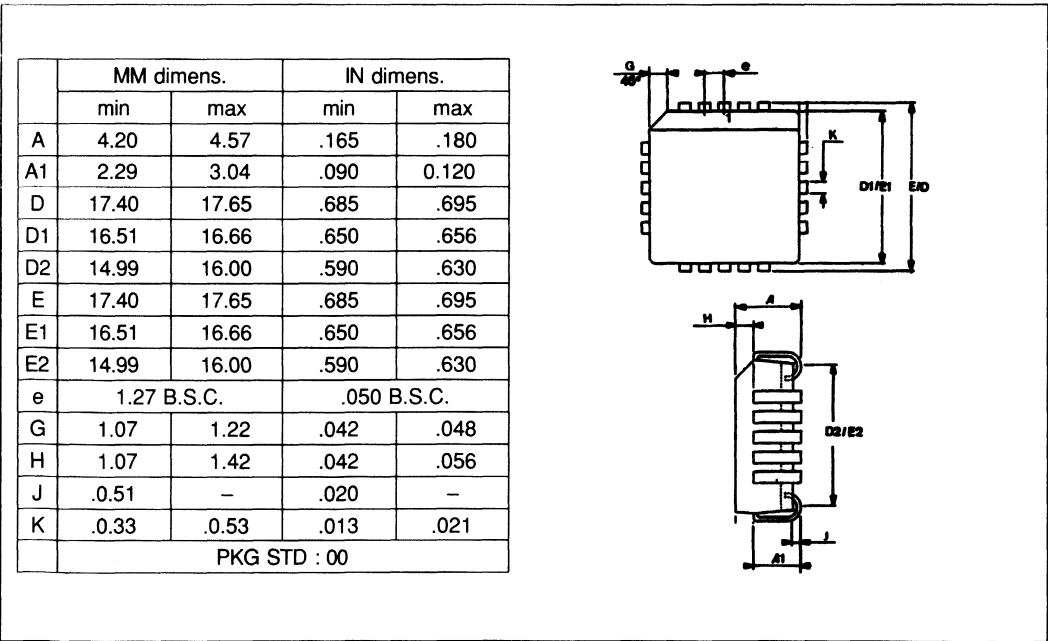
# PLCC PACKAGE DRAWING

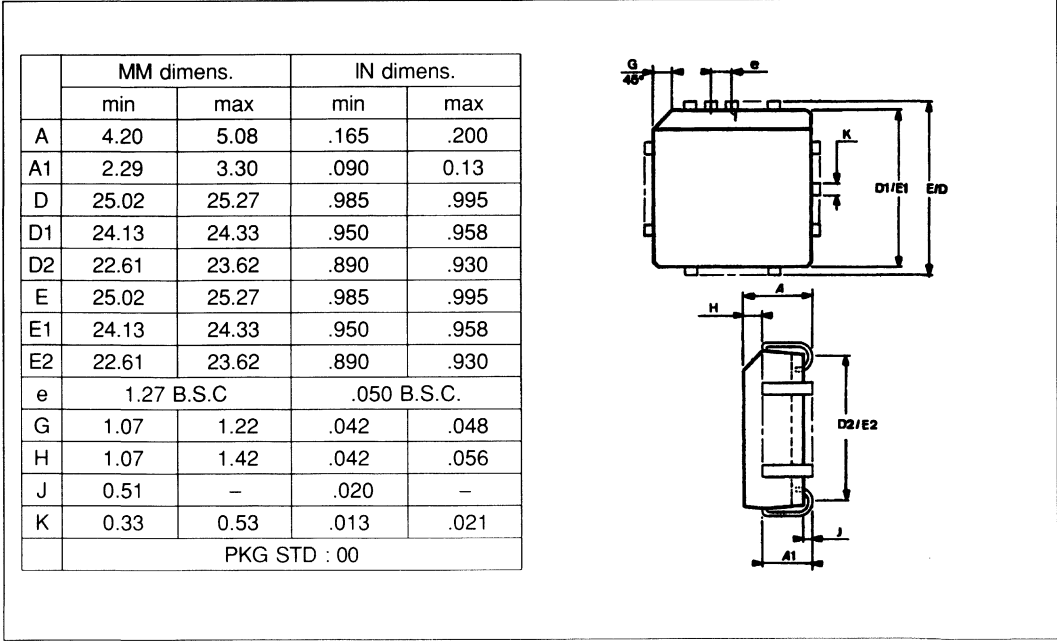
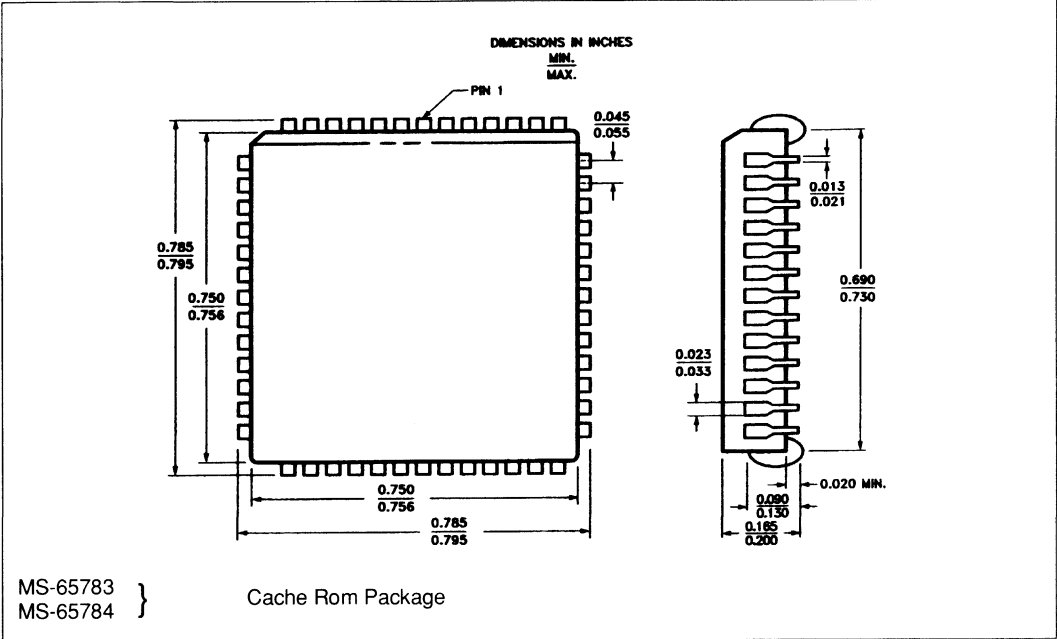
CODE : X39     8 PIN PLASTIC DIL



CODE : K04     44 PIN PLCC

REV : C





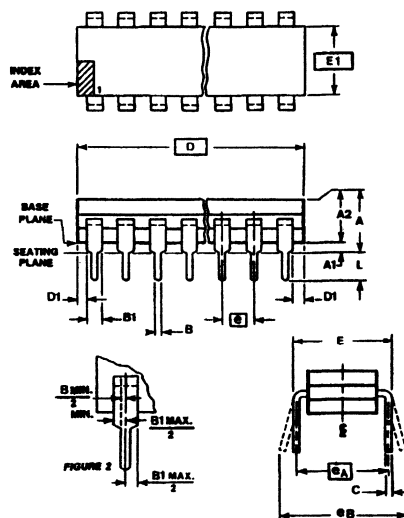
## CERDIP DUAL IN LINE

CODES : C1 - C23    20 PINS CERDIP.300

REV : C

|    | MM dims.    |       | IN dims.    |      |
|----|-------------|-------|-------------|------|
|    | min         | max   | min         | max  |
| A  | 4.32        | 5.71  | .170        | .225 |
| A1 | 0.18        | 0.74  | .007        | .029 |
| A2 | 4.14        | 5.03  | .163        | .198 |
| B  | 0.38        | 0.58  | .015        | .023 |
| B1 | 0.76        | 1.78  | .030        | .070 |
| C  | 0.20        | 0.38  | .008        | .015 |
| D  | 23.87       | 24.63 | .940        | .970 |
| D1 | 0.13        | —     | .005        | —    |
| E  | 8.00        | 8.38  | .315        | .330 |
| E1 | 7.24        | 7.87  | .285        | .310 |
| e  | 2.54 B.S.C. |       | .100 B.S.C. |      |
| eA | 7.90 B.S.C. |       | .311 B.S.C. |      |
| eB | 8.08        | 10.82 | .318        | .426 |
| L  | 3.17        | 3.81  | .125        | .150 |

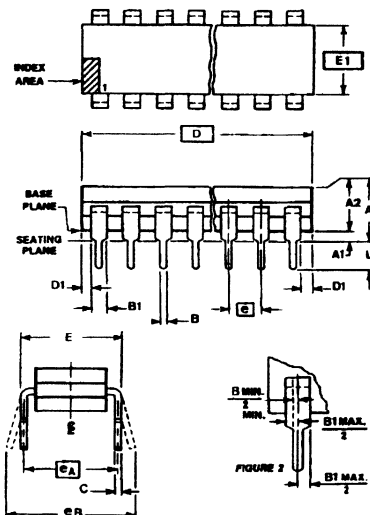
PKG STD : 01



CODE : C33    22 PINS CERDIP.300

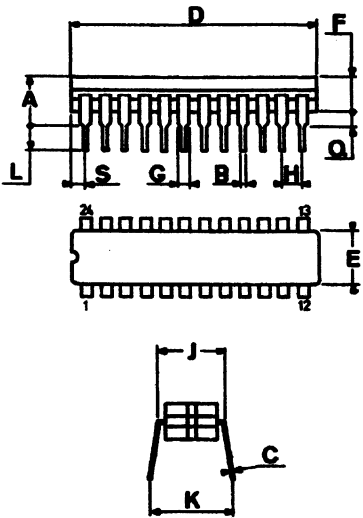
|    | MM dims.    |       | IN dims.    |       |
|----|-------------|-------|-------------|-------|
|    | min         | max   | min         | max   |
| A  | 4.47        | 5.84  | .176        | .230  |
| A1 | 0.51        | —     | .020        | —     |
| A2 | 3.17        | 4.95  | .125        | .195  |
| B  | 0.36        | 0.58  | .014        | .023  |
| B1 | 0.89        | 1.78  | .035        | .070  |
| C  | 0.20        | 0.38  | .008        | .015  |
| D  | 26.92       | 28.19 | 1.060       | 1.110 |
| D1 | 0.13        | —     | .005        | —     |
| E  | 7.82        | 8.00  | .308        | .315  |
| E1 | 7.24        | 9.91  | .285        | .310  |
| e  | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB | —           | 10.82 | —           | .426  |
| L  | 3.05        | 5.08  | .125        | .200  |

PKG STD : 01

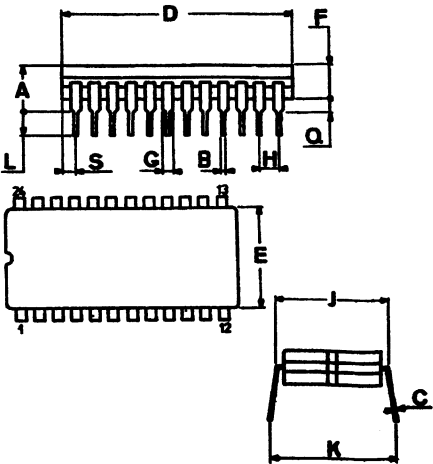


13

|              | MM dims. |       | IN dims. |       |
|--------------|----------|-------|----------|-------|
|              | min      | max   | min      | max   |
| A            | 4.31     | 5.71  | .170     | .225  |
| B            | 0.36     | 0.58  | .014     | .023  |
| C            | 0.20     | 0.38  | .008     | .015  |
| D            | 31.50    | 32.26 | 1.240    | 1.270 |
| E            | 7.24     | 7.87  | .285     | .310  |
| F            | 3.81     | 4.57  | .150     | .180  |
| G            | 0.76     | 1.78  | .030     | .070  |
| H            | 2.54 TYP |       | .100 TYP |       |
| J            | 8.00     | 8.38  | .315     | .330  |
| K            | 8.25     | 10.16 | .325     | .400  |
| L            | 3.17     | 5.08  | .125     | .200  |
| Q            | 0.50     | 1.52  | .020     | .060  |
| S            | 0.76     | 2.54  | .030     | .100  |
| PKG STD : 00 |          |       |          |       |

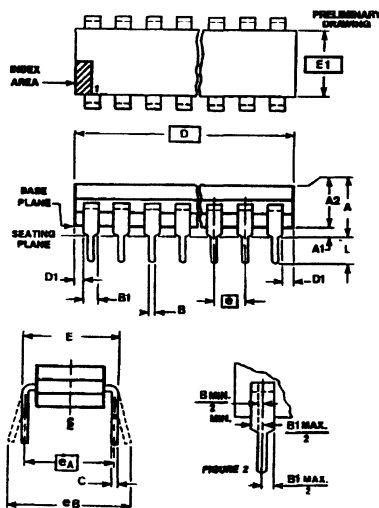


|              | MM dims. |       | IN dims. |       |
|--------------|----------|-------|----------|-------|
|              | min      | max   | min      | max   |
| A            | 4.31     | 5.71  | .170     | .225  |
| B            | 0.36     | 0.58  | .014     | .023  |
| C            | 0.20     | 0.38  | .008     | .015  |
| D            | 31.50    | 32.51 | 1.240    | 1.280 |
| E            | 13.05    | 13.66 | .514     | .538  |
| F            | 3.81     | 4.57  | .150     | .180  |
| G            | 1.27     | 1.78  | .050     | .070  |
| H            | 2.54 TYP |       | .100 TYP |       |
| J            | 15.24    | 15.75 | .600     | .620  |
| K            | 15.24    | 17.78 | .600     | .700  |
| L            | 3.17     | 5.08  | .125     | .200  |
| Q            | 0.51     | 1.52  | .020     | .060  |
| S            | 1.52     | 2.29  | .060     | .090  |
| PKG STD : 00 |          |       |          |       |



CODE : C31 - C 36 28 PINS Cerdip.300

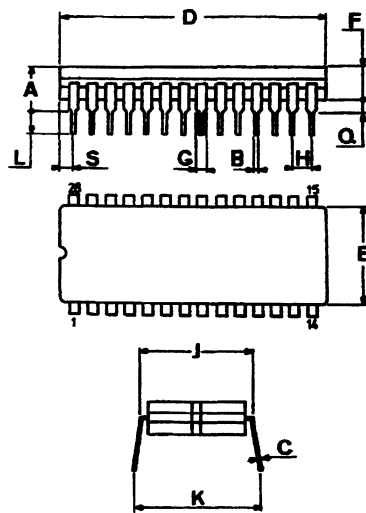
|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 3.30        | 5.84  | .130        | .230  |
| A1           | 0.38        | —     | .015        | —     |
| A2           | 2.92        | 4.95  | .115        | .195  |
| B            | 0.36        | .058  | .014        | .023  |
| B1           | 1.14        | 1.78  | .045        | .070  |
| C            | 0.20        | 0.38  | .008        | .015  |
| D            | 29.97       | 32.64 | 1.180       | 1.285 |
| D1           | 0.13        | —     | .005        | —     |
| E            | 7.62        | 8.25  | .300        | .325  |
| E1           | 6.10        | 7.87  | .240        | .310  |
| e            | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA           | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB           | —           | 11.43 | —           | .450  |
| L            | 3.05        | 5.08  | .125        | .200  |
| PKG STD : 01 |             |       |             |       |



CODE : C32 Cerdip 28 PINS.600

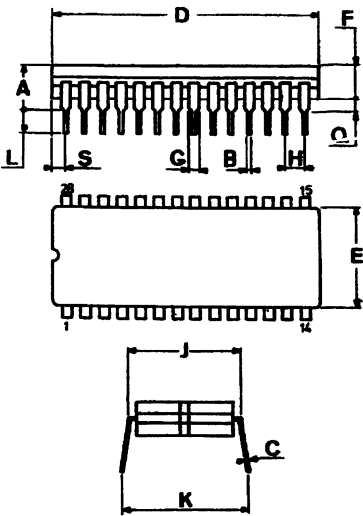
REV : B

|              | MM dims. |       | IN dims. |       |
|--------------|----------|-------|----------|-------|
|              | min      | max   | min      | max   |
| A            | 4.31     | 5.71  | .170     | .225  |
| B            | 0.36     | 0.58  | .014     | .023  |
| C            | 0.20     | 0.38  | .008     | .015  |
| D            | 36.58    | 37.85 | 1.440    | 1.490 |
| E            | 13.05    | 13.66 | .514     | .538  |
| F            | 3.81     | 4.57  | .150     | .180  |
| G            | 1.27     | 1.78  | .050     | .070  |
| H            | 2.54 TYP |       | .100 TYP |       |
| J            | 15.24    | 15.75 | .600     | .620  |
| K            | 15.24    | 17.78 | .600     | .700  |
| L            | 3.17     | 5.08  | .125     | .200  |
| Q            | 0.51     | 1.52  | .020     | .060  |
| S            | 1.52     | 2.29  | .060     | .090  |
| PKG STD : 00 |          |       |          |       |

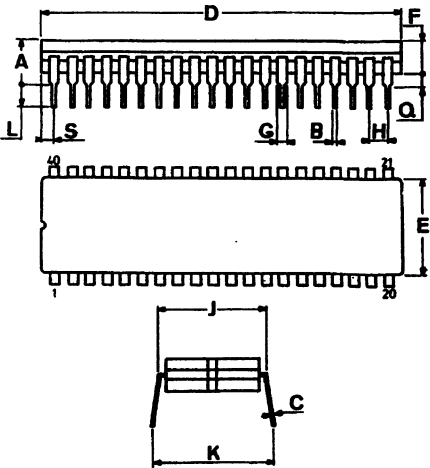


13

|              | MM dimens. |       | IN dimens. |       |
|--------------|------------|-------|------------|-------|
|              | min        | max   | min        | max   |
| A            | 4.31       | 5.71  | .170       | .225  |
| B            | 0.36       | 0.58  | .014       | .023  |
| C            | 0.20       | 0.38  | .008       | .015  |
| D            | 36.58      | 37.85 | 1.440      | 1.490 |
| E            | 14.50      | 15.11 | .571       | .595  |
| F            | 3.81       | 4.57  | .150       | .180  |
| G            | 1.27       | 1.78  | .050       | .070  |
| H            | 2.54 TYP   |       | .100 TYP   |       |
| J            | 15.24      | 15.75 | .600       | .620  |
| K            | 15.24      | 17.78 | .600       | .700  |
| L            | 3.17       | 5.08  | .125       | .200  |
| Q            | 0.51       | 1.52  | .020       | .060  |
| S            | 1.52       | 2.29  | .060       | .090  |
| PKG STD : 00 |            |       |            |       |

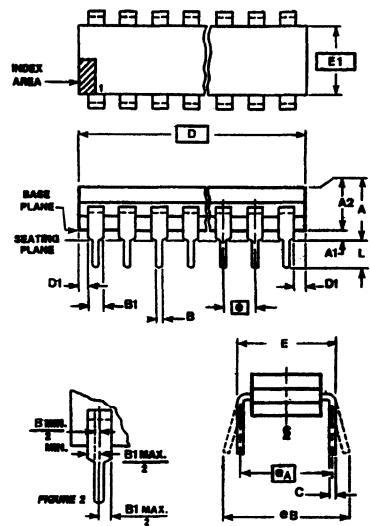


|              | MM dimens. |       | IN dimens. |       |
|--------------|------------|-------|------------|-------|
|              | min        | max   | min        | max   |
| A            | 4.31       | 5.71  | .170       | .225  |
| B            | 0.36       | 0.58  | .014       | .023  |
| C            | 0.20       | 0.38  | .008       | .015  |
| D            | 51.69      | 52.83 | 2.035      | 2.080 |
| E            | 13.05      | 13.66 | .514       | .538  |
| F            | 3.81       | 4.57  | .150       | .180  |
| G            | 1.27       | 1.78  | .050       | .070  |
| H            | 2.54 TYP   |       | .100 TYP   |       |
| J            | 15.24      | 15.75 | .600       | .620  |
| K            | 15.24      | 17.78 | .600       | .700  |
| L            | 3.17       | 5.08  | .125       | .200  |
| Q            | 0.51       | 1.52  | .020       | .060  |
| S            | 1.52       | 2.29  | .060       | .090  |
| PKG STD : 00 |            |       |            |       |



|    | MM dimens.   |       | IN dimens.  |       |
|----|--------------|-------|-------------|-------|
|    | min          | max   | min         | max   |
| A  | 4.31         | 5.71  | .170        | .225  |
| A1 | 0.51         | 1.52  | .020        | .060  |
| A2 | 3.81         | 4.57  | .150        | .180  |
| B  | 0.36         | 0.58  | .014        | .023  |
| B1 | 1.27         | 1.78  | .050        | .070  |
| C  | 0.20         | 0.38  | .008        | .015  |
| D  | 62.23        | 63.65 | 2.440       | 2.506 |
| D1 | 0.13         | —     | .005        | —     |
| E  | 15.70        | 15.85 | .618        | .624  |
| E1 | 14.78        | 15.39 | .582        | .606  |
| e  | 2.54 B.S.C.  |       | .100 B.S.C. |       |
| eA | 15.24 B.S.C. |       | .600 B.S.C. |       |
| eB | —            | 17.78 | —           | .700  |
| L  | 3.17         | 3.94  | .125        | .155  |

PKG STD : 01



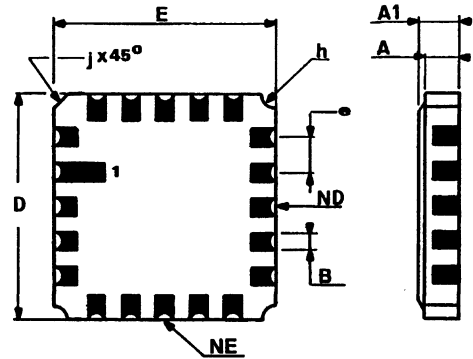
## CHIP CARRIER

CODE : L04

48 LDS.040 CENTER LEADLESS SQUARE CHIP CARRIER

REV : C

|              | MM dimens.   |       | IN dimens.   |      |
|--------------|--------------|-------|--------------|------|
|              | min          | max   | min          | max  |
| A            | 1.47         | 1.83  | .058         | .072 |
| A1           | 1.73         | 2.26  | .068         | .089 |
| B            | 0.43         | 0.58  | .017         | .023 |
| D            | 14.10        | 14.53 | .555         | .572 |
| E            | 14.10        | 14.53 | .555         | .572 |
| e            | 1.016 B.S.C. |       | .040 B.S.C.  |      |
| h            | 0.19 R.A.D.  |       | .0075 R.A.D. |      |
| j            | 0.51         |       | .020         |      |
| ND           | 12           |       | 12           |      |
| NE           | 12           |       | 12           |      |
| PKG STD : 01 |              |       |              |      |

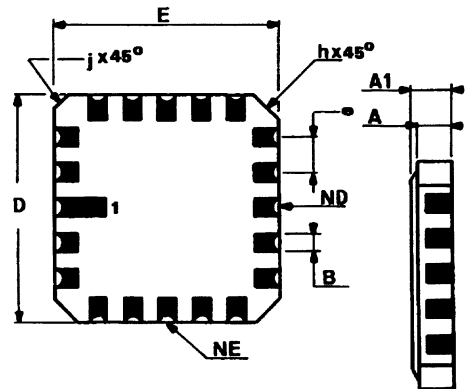


CODE : L09

48 LDS.050 CENTER LEADLESS SQUARE CHIP CARRIER

REV : C

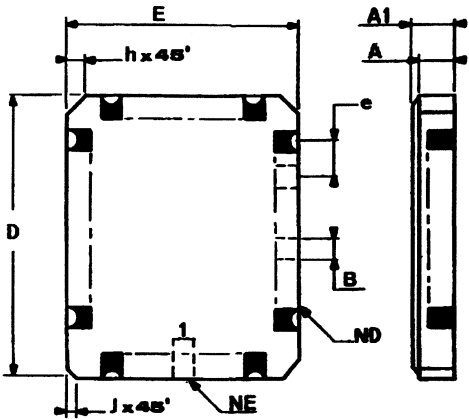
|              | MM dimens.  |       | IN dimens.  |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 1.47        | 1.83  | .058        | .072 |
| A1           | 1.73        | 2.26  | .068        | .089 |
| B            | 0.635 TYP   |       | .025 TYP    |      |
| D            | 16.33       | 16.82 | .643        | .662 |
| E            | 16.33       | 16.82 | .643        | .662 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| h            | 1.016       |       | .040        |      |
| j            | 0.51        |       | .020        |      |
| ND           | 11          |       | 11          |      |
| NE           | 11          |       | 11          |      |
| PKG STD : 01 |             |       |             |      |



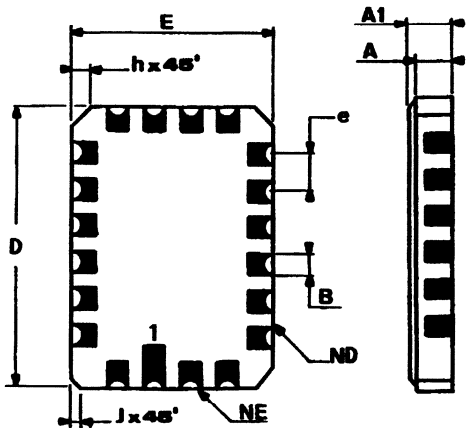
13



|              | MM dims.    |       | IN dims.    |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 1.37        | 1.65  | .054        | .063 |
| A1           | 1.62        | 2.00  | .064        | .079 |
| B            | 0.56        | 0.71  | .022        | .028 |
| D            | 13.81       | 14.22 | .544        | .560 |
| E            | 8.74        | 9.14  | .344        | .360 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| h            | 0.64 T.Y.P. |       | .025 T.Y.P. |      |
| j            | 0.38 T.Y.P. |       | .015 T.Y.P. |      |
| ND           | 9           |       | 9           |      |
| NE           | 5           |       | 5           |      |
| PKG STD : 01 |             |       |             |      |

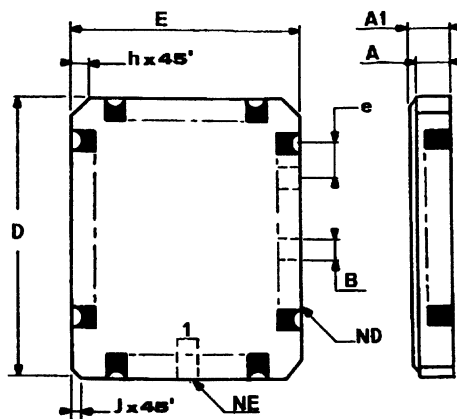


|              | MM dims.    |       | IN dims.    |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 1.37        | 1.68  | .054        | .066 |
| A1           | 1.62        | 1.98  | .064        | .078 |
| B            | 0.53        | 0.76  | .021        | .030 |
| D            | 10.64       | 10.94 | .419        | .431 |
| E            | 7.21        | 7.52  | .284        | .296 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| h            | 0.51 T.Y.P. |       | .020 T.Y.P. |      |
| j            | 0.25 T.Y.P. |       | .010 T.Y.P. |      |
| ND           | 6           |       | 6           |      |
| NE           | 4           |       | 4           |      |
| PKG STD : 02 |             |       |             |      |



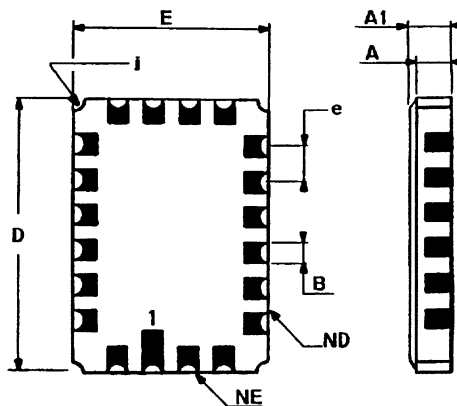
**CODES : LU, L17, L32, L19 32 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER REV : G**

|              | MM dims.     |       | IN dims.    |      |
|--------------|--------------|-------|-------------|------|
|              | min          | max   | min         | max  |
| A            | 1.62         | 1.88  | .064        | .074 |
| A1           | 1.88         | 2.18  | .074        | .086 |
| B            | 0.635 T.Y.P. |       | .025 T.Y.P. |      |
| D            | 13.81        | 14.22 | .544        | .560 |
| E            | 11.30        | 11.63 | .445        | .458 |
| e            | 1.27 B.S.C.  |       | .050 B.S.C. |      |
| h            | 1.016        |       | .040        |      |
| j            | 0.51         |       | .020        |      |
| ND           | 9            |       | 9           |      |
| NE           | 7            |       | 7           |      |
| PKG STD : 01 |              |       |             |      |



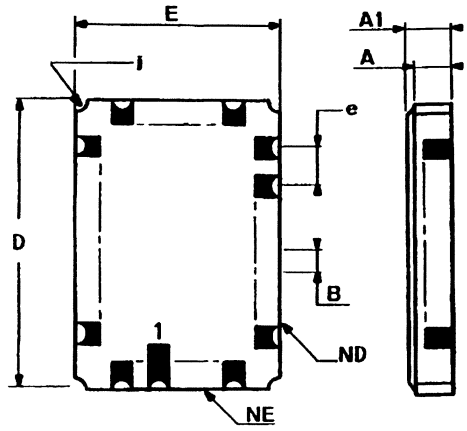
**CODE : L22      20 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER      REV : C**

|              | MM dims.    |       | IN dims.    |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 1.37        | 1.68  | .054        | .066 |
| A1           | 1.62        | 1.98  | .064        | .078 |
| B            | 0.53        | 0.76  | .021        | .030 |
| D            | 10.64       | 10.94 | .419        | .431 |
| E            | 7.46        | 7.52  | .294        | .296 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| h            |             |       |             |      |
| j            | 0.30 R.A.D. |       | .010 R.A.D. |      |
| ND           | 6           |       | 6           |      |
| NE           | 4           |       | 4           |      |
| PKG STD : 02 |             |       |             |      |



CODE : L23, L16    22 LDS.050 CENTER LEADLESS RECTANGULAR CHIP CARRIER    REV : A

|              | MM dims.    |       | IN dims.    |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 1.52        | 1.73  | .055        | .068 |
| A1           | 1.78        | 2.03  | .070        | .080 |
| B            | 0.15        | —     | .006        | —    |
| D            | 12.31       | 12.57 | .485        | .495 |
| E            | 7.24        | 7.49  | .285        | .295 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| h            |             |       |             |      |
| j            | 0.30 R.A.D. |       | 0.12 R.A.D. |      |
| ND           | 7           |       | 7           |      |
| NE           | 4           |       | 4           |      |
| PKG STD : 00 |             |       |             |      |



CODE : L01    32 LDS .040 CENTER LEADLESS SQUARE CHIP CARRIER

|                    | MM        |       | INCH      |      |
|--------------------|-----------|-------|-----------|------|
| A                  | 10.54     | 10.92 | .415      | .430 |
| B                  | 10.54     | 10.92 | .415      | .430 |
| C                  | 1.85      | 2.26  | .073      | .089 |
| D                  | 1.016 BSC |       | .040 BSC  |      |
| E                  | 0.51 TYP  |       | .020 TYP  |      |
| F                  | 0.84      | 1.20  | .033      | .047 |
| G                  | 0.19 RAD  |       | .0075 RAD |      |
| H                  | 0.51 × 45 |       | .020 × 45 |      |
| PKG STD : OBSOLETE |           |       |           |      |

|                | MM        |       | INCH      |      |
|----------------|-----------|-------|-----------|------|
| A              | 1.47      | 1.83  | .058      | .072 |
| A1             |           | 2.03  | .063      | .080 |
| B              | 0.51 TYP  |       | .020 TYP  |      |
| D              | 10.00     | 10.32 | .394      | .406 |
| E              | 10.00     | 10.32 | .394      | .406 |
| e              | 1.016 BSC |       | .040 BSC  |      |
| h              | 0.19 RAD  |       | .0075 RAD |      |
| j              | 0.51      |       | .020      |      |
| ND             | 8         |       | 8         |      |
| NE             | 8         |       | 8         |      |
| PKG STD : -01- |           |       |           |      |

## PLASTIC DUAL IN LINE

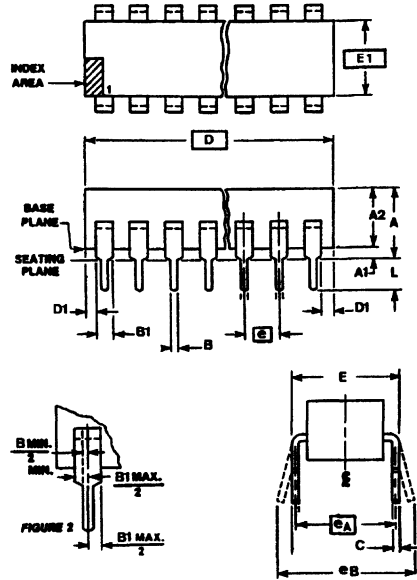
CODES : X8 - O34

20 PINS PLASTIC.300

REV : G

|    | MM dims.    |       | IN dims.    |       |
|----|-------------|-------|-------------|-------|
|    | min         | max   | min         | max   |
| A  | —           | 5.33  | —           | .210  |
| A1 | 0.39        | —     | .015        | —     |
| A2 | 2.92        | 4.95  | .115        | .195  |
| B  | 0.36        | —     | .014        | —     |
| B1 | 1.14        | 1.78  | .045        | .070  |
| C  | 0.20        | 0.38  | .008        | .015  |
| D  | 23.50       | 26.90 | .925        | 1.060 |
| E  | 7.62        | 8.25  | .300        | .325  |
| E1 | 6.10        | 7.11  | .240        | .280  |
| e  | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB | —           | 10.92 | —           | .430  |
| L  | 2.92        | 4.06  | .115        | .160  |
| D1 | 0.13        | —     | .005        | —     |

PKG STD :



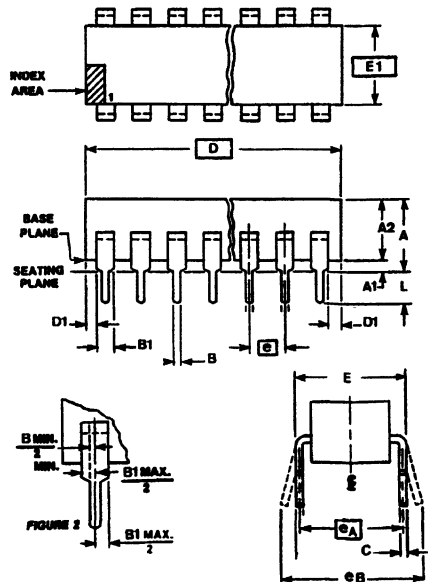
CODES : O41, O53, O54

22 PINS PLASTIC.300

REV : A

|    | MM dims.    |       | IN dims.    |       |
|----|-------------|-------|-------------|-------|
|    | min         | max   | min         | max   |
| A  | —           | 5.33  | —           | .210  |
| A1 | 0.39        | —     | .015        | —     |
| A2 | 2.92        | 4.95  | .115        | .195  |
| B  | 0.36        | —     | .014        | —     |
| B1 | 1.14        | 1.78  | .045        | .070  |
| C  | 0.20        | 0.38  | .008        | .015  |
| D  | 26.67       | 28.45 | 1.050       | 1.120 |
| E  | 7.62        | 8.25  | .300        | .325  |
| E1 | 6.10        | 7.11  | .240        | .280  |
| e  | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB | —           | 10.92 | —           | .430  |
| L  | 2.92        | 4.06  | .115        | .160  |
| D1 | 0.13        | —     | .005        | —     |

PKG STD : 00



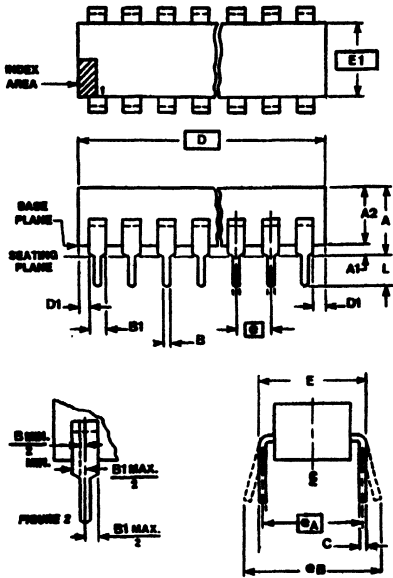
13

CODES : O43, O44

24 PINS PLASTIC.300

REV : G

|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | —           | 5.33  | —           | .210  |
| A1           | 0.39        | —     | .015        | —     |
| A2           | 2.92        | 4.95  | .115        | .195  |
| B            | 0.36        | —     | .014        | —     |
| B1           | 1.14        | 1.78  | .045        | .070  |
| C            | 0.20        | 0.38  | .008        | .015  |
| D            | 28.60       | 32.30 | 1.125       | 1.275 |
| E            | 7.62        | 8.25  | .300        | .325  |
| E1           | 6.10        | 7.10  | .240        | .280  |
| e            | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA           | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB           | —           | 10.92 | —           | .430  |
| L            | 2.92        | 4.06  | .115        | .160  |
| D1           | 0.13        | —     | .005        | —     |
| PKG STD : 02 |             |       |             |       |

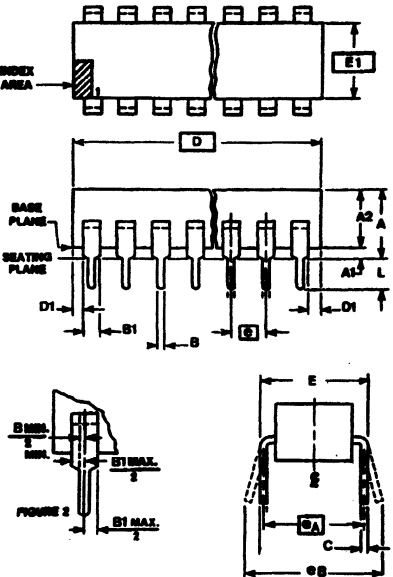


CODES : O3, X3, X40

24 PINS PLASTIC.300

REV : D

|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | —            | 6.35  | —           | .250  |
| A1           | 0.38         | —     | .015        | —     |
| A2           | 3.18         | 4.95  | .125        | .195  |
| B            | 0.36         | 0.56  | .014        | .022  |
| B1           | 0.76         | 1.78  | .030        | .070  |
| C            | 0.20         | 0.38  | .008        | .015  |
| D            | 29.21        | 32.77 | 1.150       | 1.290 |
| E            | 15.24        | 15.87 | .600        | .625  |
| E1           | 12.32        | 14.73 | .485        | .580  |
| e            | 2.54 B.S.C.  |       | .100 B.S.C. |       |
| eA           | 15.24 B.S.C. |       | .600 B.S.C. |       |
| eB           | —            | 17.78 | —           | .700  |
| L            | 2.93         | 5.08  | .115        | .200  |
| D1           | 0.13         | —     | .005        | —     |
| PKG STD : 02 |              |       |             |       |

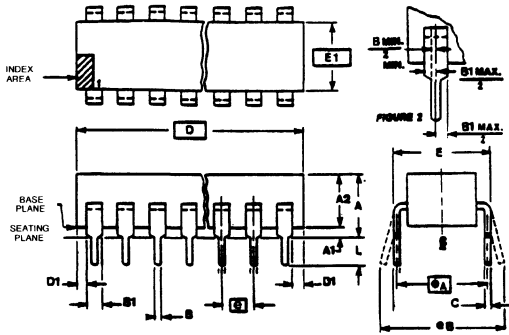


13

CODES : O49, O51

28 PINS PLASTIC.300

|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | —           | 4.57  | —           | .180  |
| A1           | 0.51        | —     | .020        | —     |
| A2           | —           | 3.30  | —           | .130  |
| B            | 0.36        | —     | .014        | —     |
| B1           | 1.14        | 1.78  | .045        | .070  |
| C            | 0.20        | 0.38  | .008        | .015  |
| D            | 34.54       | 34.80 | 1.360       | 1.370 |
| E            | 7.62        | 8.25  | .300        | .325  |
| E1           | 7.11        | 7.62  | .280        | .300  |
| e            | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA           | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB           | —           | 10.92 | —           | .430  |
| L            | 3.18        | 3.43  | .125        | .135  |
| D1           | 0.71        | 0.97  | .028        | .038  |
| PKG STD : 00 |             |       |             |       |

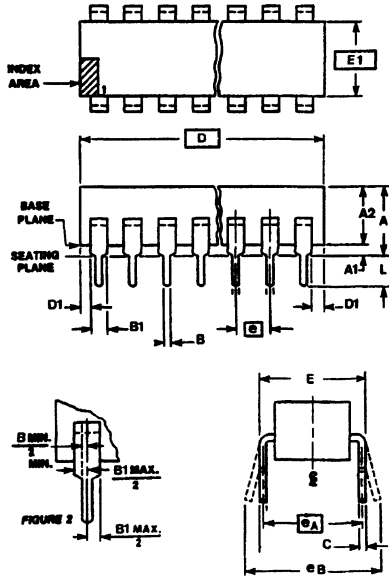


CODES : X33, O50, O33

28 PINS PLASTIC.600

REV : C

|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | —            | 6.35  | —           | .250  |
| A1           | 0.38         | —     | .015        | —     |
| A2           | 3.18         | 4.95  | .125        | .195  |
| B            | 0.36         | 0.56  | .014        | .022  |
| B1           | 0.76         | 1.78  | .030        | .070  |
| C            | 0.20         | 0.38  | .008        | .015  |
| D            | 35.05        | 39.75 | 1.380       | 1.565 |
| E            | 15.24        | 15.87 | .600        | .625  |
| E1           | 12.32        | 14.73 | .485        | .580  |
| e            | 2.54 B.S.C.  |       | .100 B.S.C. |       |
| eA           | 15.24 B.S.C. |       | .600 B.S.C. |       |
| eB           | —            | 17.78 | —           | .700  |
| L            | 2.93         | 5.08  | .115        | .200  |
| D1           | 0.13         | —     | .005        | —     |
| PKG STD : 02 |              |       |             |       |

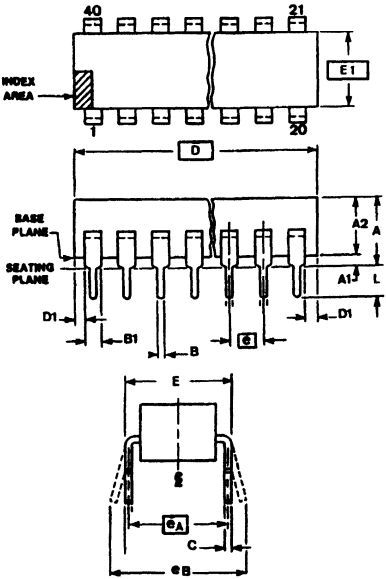


CODE : 3J

40 PINS PLASTIC.600

REV : C

|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | —            | 6.35  | —           | .250  |
| A1           | 0.38         | —     | .015        | —     |
| A2           | 3.18         | 4.95  | .125        | .195  |
| B            | 0.36         | 0.56  | .014        | .022  |
| B1           | 0.76         | 1.78  | .030        | .070  |
| C            | 0.20         | 0.38  | .008        | .015  |
| D            | 50.29        | 53.21 | 1.980       | 2.095 |
| E            | 15.24        | 15.87 | .600        | .625  |
| E1           | 12.32        | 14.73 | .485        | .580  |
| e            | 2.54 B.S.C.  |       | .100 B.S.C. |       |
| eA           | 15.24 B.S.C. |       | .600 B.S.C. |       |
| eB           | —            | 17.78 | —           | .700  |
| L            | 2.93         | 5.08  | .115        | .200  |
| D1           | 0.13         | —     | .005        | —     |
| PKG STD : 02 |              |       |             |       |

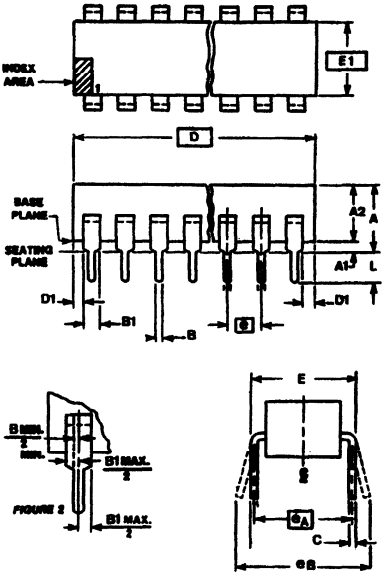


CODES : 036

48 PINS PLASTIC.600

REV : C

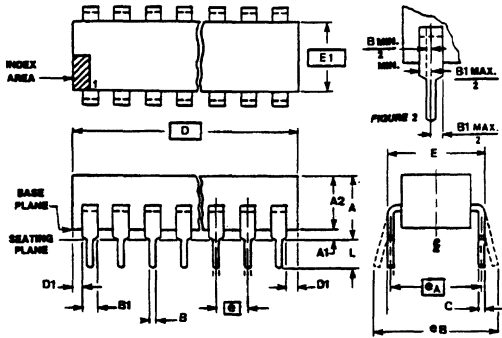
|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | —            | 6.35  | —           | .250  |
| A1           | 0.38         | —     | .015        | —     |
| A2           | 3.18         | 4.95  | .125        | .195  |
| B            | 0.36         | 0.56  | .014        | .022  |
| B1           | 0.76         | 1.78  | .030        | .070  |
| C            | 0.20         | 0.38  | .008        | .015  |
| D            | 61.98        | 62.48 | 2.440       | 2.460 |
| E            | 15.24        | 15.87 | .600        | .625  |
| E1           | 12.32        | 14.73 | .485        | .580  |
| e            | 2.54 B.S.C.  |       | .100 B.S.C. |       |
| eA           | 15.24 B.S.C. |       | .600 B.S.C. |       |
| eB           | —            | 17.78 | —           | .700  |
| L            | 2.93         | 5.08  | .115        | .200  |
| D1           | 0.13         | —     | .005        | —     |
| PKG STD : 01 |              |       |             |       |



13

CODES : 049, 051    28 PINS PLASTIC.300

|              | MM dimens.  |       | IN dimens.  |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | —           | 4.57  | —           | .180  |
| A1           | 0.51        | —     | .020        | —     |
| A2           | —           | 3.30  | —           | .130  |
| B            | 0.36        | —     | .014        | —     |
| B1           | 1.14        | 1.78  | .045        | .070  |
| C            | 0.20        | 0.38  | .008        | .015  |
| D            | 34.54       | 34.80 | 1.360       | 1.370 |
| E            | 7.62        | 8.25  | .300        | .325  |
| E1           | 7.11        | 7.62  | .280        | .300  |
| e            | 2.54 B.S.C. |       | .100 B.S.C. |       |
| eA           | 7.62 B.S.C. |       | .300 B.S.C. |       |
| eB           | —           | 10.92 | —           | .430  |
| L            | 3.18        | 3.43  | .125        | .135  |
| D1           | 0.71        | 0.97  | .028        | .038  |
| PKG STD : 00 |             |       |             |       |



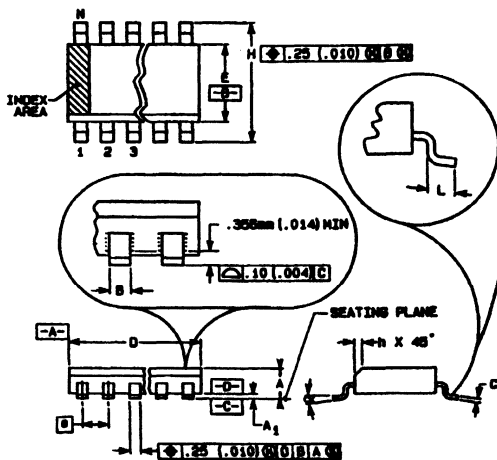


## SMALL OUTLINE

**CODES : N01    20 PINS S.O. (.300)**

**REV : F**

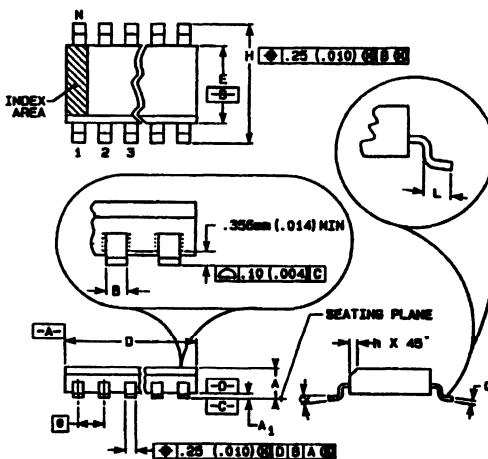
|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 2.35        | 2.65  | .0926       | .1043 |
| A1           | 0.10        | 0.30  | .0040       | .0118 |
| B            | 0.35        | 0.49  | .0138       | .0192 |
| C            | 0.23        | 0.32  | .0091       | .0125 |
| D            | 12.60       | 13.00 | .4961       | .5118 |
| E            | 7.40        | 7.60  | .2914       | .2992 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |       |
| H            | 10.00       | 10.65 | .394        | .419  |
| h            | 0.25        | 0.75  | .010        | .029  |
| L            | 0.40        | 1.27  | .016        | .050  |
| N            | 20          |       | 20          |       |
| $\alpha$     | 0*          |       | 8*          |       |
| PKG STD : 01 |             |       |             |       |



**CODES : N02 24 PINS S.O. (.300)**

REV : F

|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 2.35        | 2.65  | .0926       | .1043 |
| A1           | 0.10        | 0.30  | .0040       | .0118 |
| B            | 0.35        | 0.49  | .0138       | .0192 |
| C            | 0.23        | 0.32  | .0091       | .0125 |
| D            | 15.20       | 15.60 | .5985       | .6141 |
| E            | 7.40        | 7.60  | .2914       | .2992 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |       |
| H            | 10.00       | 10.65 | .394        | .419  |
| h            | 0.25        | 0.75  | .010        | .029  |
| L            | 0.40        | 1.27  | .016        | .050  |
| N            | 24          |       | 24          |       |
| $\alpha$     | 0°          |       | 8°          |       |
| PKG STD : 01 |             |       |             |       |

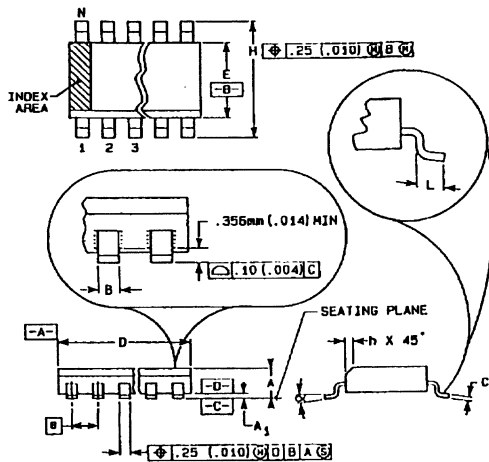


**CODE : N10**

**28 PINS S.O.(300)**

**REV : F**

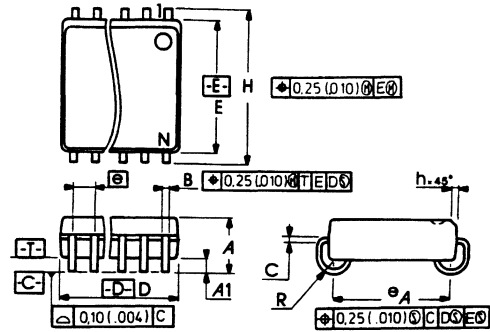
|              | MM dims.    |       | IN dims.    |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 2.35        | 2.65  | .0926       | .1043 |
| A1           | 0.10        | 0.30  | .0040       | .0118 |
| B            | 0.35        | 0.49  | .0138       | .0192 |
| C            | 0.23        | 0.32  | .0091       | .0125 |
| D            | 17.70       | 18.10 | .6969       | .7125 |
| E            | 7.40        | 7.60  | .2914       | .2992 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |       |
| H            | 10.00       | 10.65 | .394        | .419  |
| h            | 0.25        | 0.75  | .010        | .029  |
| L            | 0.40        | 1.27  | .016        | .050  |
| N            | 28          |       | 28          |       |
| $\alpha$     | 0*          |       | 8*          |       |
| PKG STD : 01 |             |       |             |       |



## SOJ PACKAGES

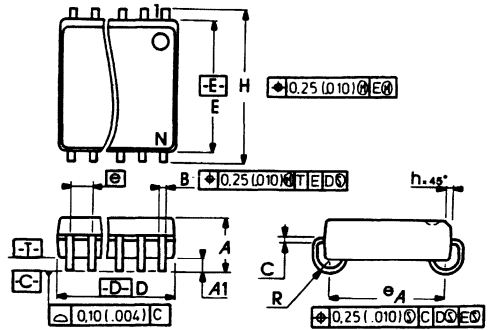
CODES : P02 24 PINS S.O.J.(.300)

|              | MM dimens.  |       | IN dimens.  |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 3.05        | 3.56  | .120        | .140 |
| A1           | 0.71        | 0.91  | .028        | .036 |
| B            | 0.35        | 0.48  | .014        | .019 |
| C            | 0.254       |       | .010        |      |
| D            | 15.29       | 15.54 | .602        | .612 |
| E            | 7.42        | 7.59  | .292        | .299 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| H            | 8.51        | 8.81  | .335        | .347 |
| h            | 0.25        | 0.41  | .010        | .016 |
| eA           | 6.65        | 6.91  | .262        | .272 |
| N            | 24          |       | 24          |      |
| R            | 0.79        | 1.07  | .031        | .042 |
| PKG STD : 01 |             |       |             |      |



CODES : P03 28 PINS S.O.J.(.300)

|              | MM dimens.  |       | IN dimens.  |      |
|--------------|-------------|-------|-------------|------|
|              | min         | max   | min         | max  |
| A            | 3.05        | 3.56  | .120        | .140 |
| A1           | 0.71        | 0.91  | .028        | .036 |
| B            | 0.35        | 0.48  | .014        | .019 |
| C            | 0.254       |       | .010        |      |
| D            | 17.81       | 18.06 | .701        | .711 |
| E            | 7.42        | 7.59  | .292        | .299 |
| e            | 1.27 B.S.C. |       | .050 B.S.C. |      |
| H            | 8.51        | 8.81  | .335        | .347 |
| h            | 0.25        | 0.41  | .010        | .016 |
| eA           | 6.65        | 6.91  | .262        | .272 |
| N            | 28          |       | 28          |      |
| R            | 0.79        | 1.07  | .031        | .042 |
| PKG STD : 01 |             |       |             |      |

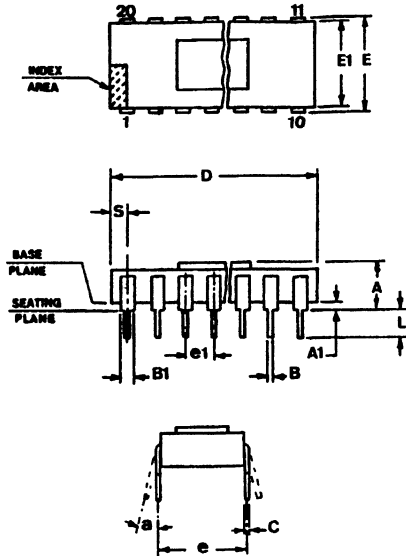


## SIDE BRAZE

CODES : S15, S25 20 LEAD (.300) SIDE BRAZE

REV : O

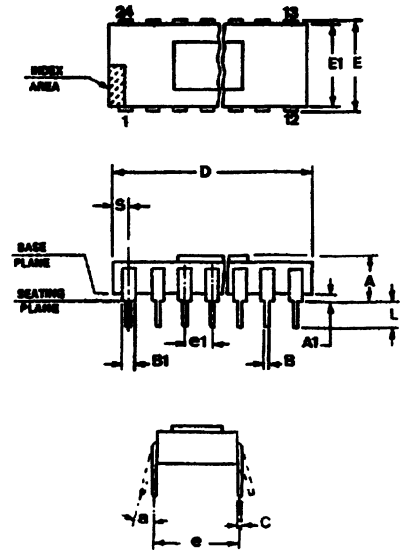
|              | MM dimens.  |       | IN dimens.  |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 2.82        | 3.94  | .111        | .155  |
| B            | 0.38        | 0.53  | .015        | .021  |
| C            | 0.20        | 0.30  | .008        | .012  |
| D            | 25.14       | 25.65 | .990        | 1.010 |
| E1           | 7.49 R.E.F  |       | .295 R.E.F. |       |
| B1           | 1.22        | 1.32  | .048        | .052  |
| e1           | 2.54 T.Y.P. |       | .100 T.Y.P. |       |
| E            | 7.37        | 8.25  | .290        | .325  |
| L            | 3.18        | 4.44  | .125        | .175  |
| A1           | 0.63        | 1.14  | .025        | .045  |
| S            | 2.41        | 2.67  | .095        | .105  |
| a            | 0*          | 15*   | 0*          | 15*   |
| PKG STD : 00 |             |       |             |       |

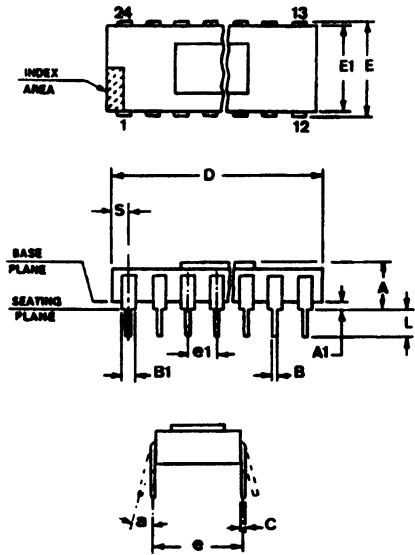


CODE : S31 24 LEAD (.300) SIDE BRAZE

REV : O

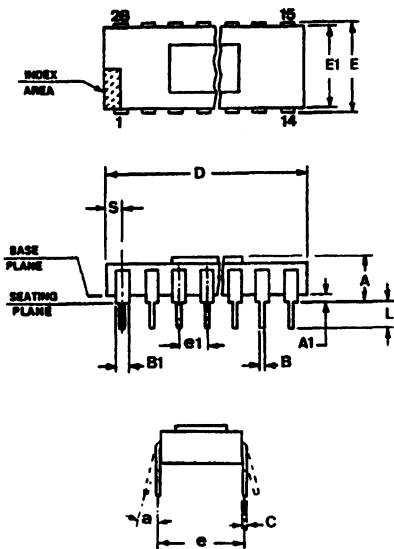
|              | MM dimens.  |       | IN dimens.  |       |
|--------------|-------------|-------|-------------|-------|
|              | min         | max   | min         | max   |
| A            | 2.67        | 4.44  | .105        | .175  |
| B            | 0.38        | 0.58  | .015        | .023  |
| C            | 0.20        | 0.30  | .008        | .012  |
| D            | 28.39       | 30.78 | 1.188       | 1.212 |
| E1           | 7.29        | 8.26  | .287        | .325  |
| B1           | 0.97        | 1.52  | .038        | .060  |
| e1           | 2.54 T.Y.P. |       | .100 T.Y.P. |       |
| E            | 7.37        | 8.25  | .290        | .325  |
| e            | 7.62 T.Y.P. |       | .300 T.Y.P. |       |
| L            | 3.18        | 4.44  | .125        | .175  |
| A1           | 0.64        | 1.39  | .025        | .055  |
| S            | 2.11        | 2.97  | .083        | .117  |
| e            | 0*          | 15*   | 0*          | 15*   |
| PKG STD : 00 |             |       |             |       |





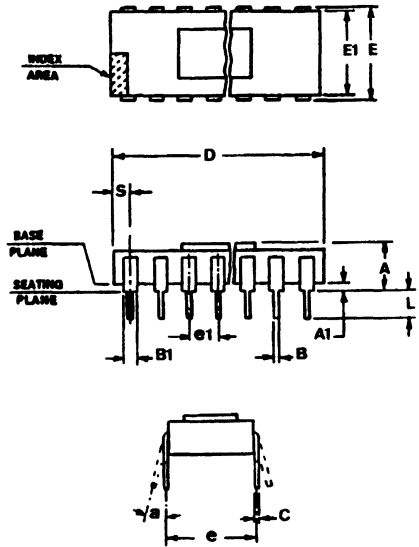
|                    | MM dims. |       | IN dims. |       |
|--------------------|----------|-------|----------|-------|
|                    | min      | max   | min      | max   |
| A                  | 1.90     | 3.18  | .075     | .125  |
| B                  | 0.41     | 0.51  | .016     | .020  |
| C                  | 0.22     | 0.30  | .009     | .012  |
| D                  | 30.10    | 31.10 | 1.185    | 1.224 |
| E                  | 14.75    | 15.25 | .580     | .600  |
| F                  |          |       |          |       |
| G                  | 1.27 TYP |       | .050 TYP |       |
| H                  | 2.27     | 2.79  | .090     | .110  |
| J                  |          |       |          |       |
| K                  | 14.99    | 15.49 | .590     | .610  |
| L                  | 3.18     | 5.08  | .125     | .200  |
| Q                  | 1.02     | 1.52  | .040     | .060  |
| S                  | 1.02     | 1.52  | .040     | .060  |
| PKG STD : OBSOLETE |          |       |          |       |

|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | 2.20         | 4.80  | .085        | .190  |
| B            | 0.38         | 0.58  | .015        | .023  |
| C            | 0.20         | 0.30  | .008        | .012  |
| D            | 29.88        | 30.98 | 1.180       | 1.220 |
| E1           | 14.61        | 15.49 | .575        | .610  |
| B1           | 0.97         | 1.52  | .038        | .060  |
| e1           | 2.54 T.Y.P.  |       | .100 T.Y.P. |       |
| E            | 15.12        | 15.87 | .595        | .625  |
| e            | 15.24 T.Y.P. |       | .600 T.Y.P. |       |
| L            | 3.18         | 4.44  | .125        | .175  |
| A1           | 0.51         | 1.77  | .020        | .070  |
| S            | 0.77         | 1.65  | .030        | .065  |
| e            | 0*           | 15*   | 0*          | 15*   |
| PKG STD : 01 |              |       |             |       |



|                    | MM dims. |       | IN dims. |      |
|--------------------|----------|-------|----------|------|
|                    | min      | max   | min      | max  |
| A                  | 1.90     | 3.18  | .075     | .125 |
| B                  | 0.41     | 0.51  | .016     | .020 |
| C                  | 0.22     | 0.30  | .009     | .012 |
| D                  | 35.20    | 36.20 | .380     | .420 |
| E                  | 14.75    | 15.25 | .580     | .600 |
| F                  |          |       |          |      |
| G                  | 1.27 TYP |       | .050 TYP |      |
| H                  | 2.27     | 2.79  | .090     | .110 |
| J                  |          |       |          |      |
| K                  | 14.99    | 15.49 | .590     | .610 |
| L                  | 3.18     | 5.08  | .125     | .200 |
| Q                  | 1.02     | 1.52  | .040     | .060 |
| S                  | 1.02     | 1.52  | .040     | .060 |
| PKG STD : OBSOLETE |          |       |          |      |

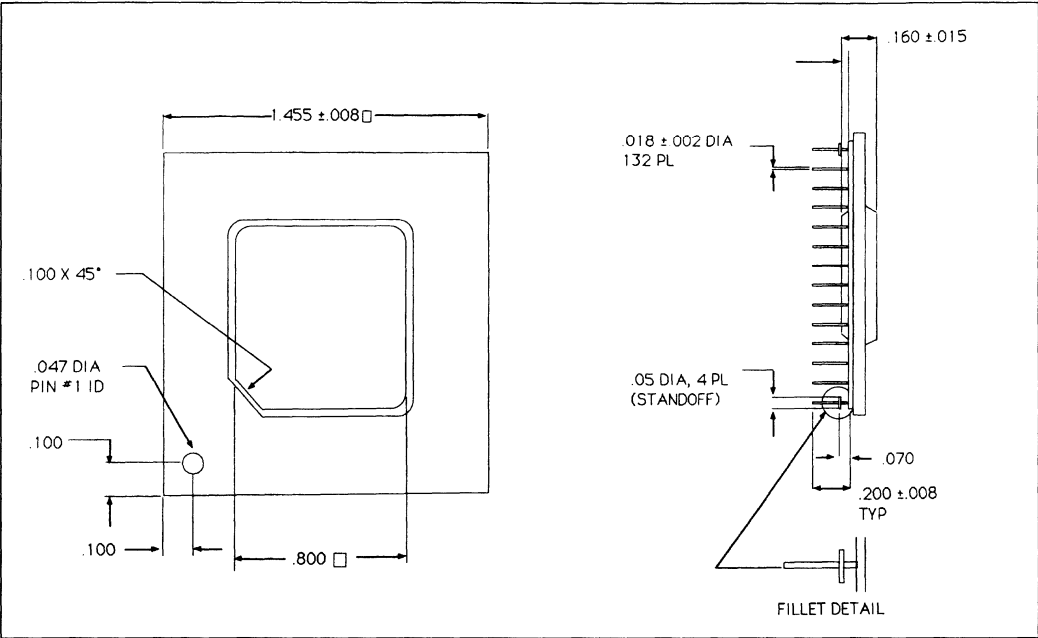
|              | MM dims.     |       | IN dims.    |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | 2.20         | 4.80  | .085        | .190  |
| B            | 0.38         | 0.58  | .015        | .023  |
| C            | 0.20         | 0.30  | .008        | .012  |
| D            | 35.06        | 36.22 | 1.180       | 1.220 |
| E1           | 14.74        | 15.49 | .580        | .610  |
| B1           | 0.97         | 1.52  | .038        | .060  |
| e1           | 2.54 T.Y.P.  |       | .100 T.Y.P. |       |
| E            | 15.12        | 15.87 | .595        | .625  |
| e            | 15.24 T.Y.P. |       | .600 T.Y.P. |       |
| L            | 3.18         | 4.44  | .125        | .175  |
| A1           | 0.51         | 1.77  | .020        | .070  |
| S            | 0.77         | 1.65  | .030        | .065  |
| e            | 0*           | 15*   | 0*          | 15*   |
| PKG STD : 01 |              |       |             |       |



|                    | MM dimens. |       | IN dimens. |       |
|--------------------|------------|-------|------------|-------|
|                    | min        | max   | min        | max   |
| A                  | 1.90       | 3.18  | .075       | .125  |
| B                  | 0.41       | 0.51  | .016       | .020  |
| C                  | 0.22       | 0.30  | .009       | .012  |
| D                  | 50.29      | 51.31 | 1.980      | 2.020 |
| E                  | 14.75      | 15.25 | .580       | .600  |
| F                  |            |       |            |       |
| G                  | 1.27 TYP   |       | .050 TYP   |       |
| H                  | 2.27       | 2.79  | .090       | .110  |
| J                  |            |       |            |       |
| K                  | 14.99      | 15.49 | .590       | .610  |
| L                  | 3.18       | 5.08  | .125       | .200  |
| Q                  | 1.02       | 1.52  | .040       | .060  |
| S                  | 1.02       | 1.52  | .040       | .060  |
| PKG STD : OBSOLETE |            |       |            |       |

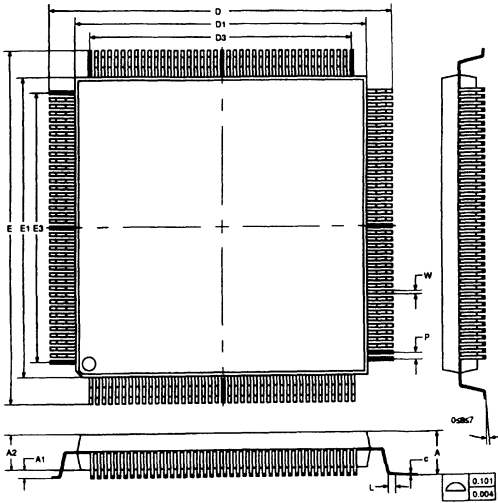
|              | MM dimens.   |       | IN dimens.  |       |
|--------------|--------------|-------|-------------|-------|
|              | min          | max   | min         | max   |
| A            | 2.20         | 4.80  | .085        | .190  |
| B            | 0.38         | 0.58  | .015        | .023  |
| C            | 0.20         | 0.30  | .008        | .012  |
| D            | 50.30        | 51.56 | 1.980       | 2.030 |
| E1           | 14.74        | 15.49 | .580        | .610  |
| B1           | 0.97         | 1.52  | .038        | .060  |
| e1           | 2.54 T.Y.P.  |       | .100 T.Y.P. |       |
| E            | 15.12        | 15.87 | .595        | .625  |
| e            | 15.24 T.Y.P. |       | .600 T.Y.P. |       |
| L            | 3.18         | 4.44  | .125        | .175  |
| A1           | 0.51         | 1.77  | .020        | .070  |
| S            | 0.77         | 1.65  | .030        | .065  |
| e            | 0*           | 15*   | 0*          | 15*   |
| PKG STD : 01 |              |       |             |       |

132 LEAD PGA



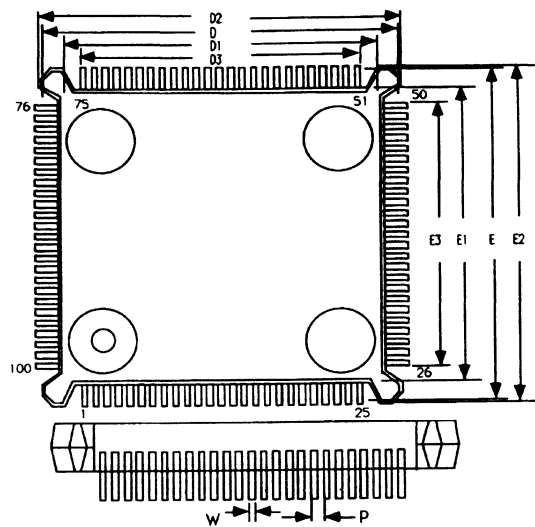
164 LEAD PQFP

| SYMBOL | MILLIMETER |       | INCH  |       |
|--------|------------|-------|-------|-------|
|        | MIN        | MAX   | MIN   | MAX   |
| A      | 3.91       | 4.34  | 0.154 | 0.171 |
| A1     | 0.50       | 0.75  | 0.020 | 0.030 |
| A2     | 3.43       | 3.55  | 0.135 | 0.140 |
| D      | 32.39      | 32.64 | 1.275 | 1.285 |
| D1     | 27.90      | 28.10 | 1.098 | 1.106 |
| D3     | 25.40      | REF.  | 1.000 | REF.  |
| E      | 32.39      | 32.64 | 1.275 | 1.285 |
| E1     | 27.90      | 28.10 | 1.098 | 1.106 |
| E3     | 25.40      | REF.  | 1.000 | REF.  |
| P      | 0.635      | BSC.  | 0.025 | BSC.  |
| W      | 0.25       | 0.33  | 0.009 | 0.013 |
| c      | 0.15       | 0.20  | 0.006 | 0.008 |
| L      | 0.51       | 0.76  | 0.020 | 0.030 |



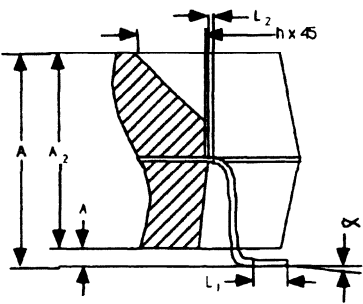


100 LEAD PQFP



| SYMBOL | MILLIMETER |       | INCHES   |       |
|--------|------------|-------|----------|-------|
|        | MIN        | MAX   | MIN      | MAX   |
| A      | 4.06       | 4.57  | 0.160    | 0.180 |
| A1     | 0.51       | 1.02  | 0.020    | 0.40  |
| A2     | 3.05       | 4.06  | .120     | .160  |
| D      | 22.23      | 22.48 | .875     | .885  |
| D1     | 18.97      | 19.13 | .747     | .753  |
| D2     | 22.78      | 22.94 | .897     | .903  |
| D3     | 15.24 REF  |       | .600 REF |       |
| E      | 22.23      | 22.48 | .875     | .885  |
| E1     | 18.97      | 19.13 | .747     | .753  |
| E2     | 22.78      | 22.86 | .897     | .903  |
| E3     | 15.24 REF  |       | .600 REF |       |
| h      | 1.07       | 1.42  | .042     | .056  |
| L1     | 0.51       | 0.76  | .020     | .030  |
| L2     | 0.076      | 0.176 | .003     | .007  |
| P      | .635       |       | .025     |       |
| W      | .254       |       | .008     |       |
| α      | 0 deg      | 8 deg | 0 deg    | 8 deg |

C415  
100-lead JEDEC PQFP





# QUALITY

14







---

# QUALITY

---

## 1 - INTRODUCTION

### 1 - INTRODUCTION

This section aims to describe the quality policy and the quality system implemented by MATRA MHS in order to provide customers with highest quality and reliability products and services.

### 2 - APPLICABLE DOCUMENTS

The following documents form a part of this section to the extent referenced herein and provide the foundation of MHS quality system :

MIL - M - 38510H "General specification of microcircuits"

MIL - STD - 883C "Test methods and procedures for microelectronics"

ESA/SCC 9000 "European Space Agency specifications for microelectronics"

CECC 9000 "Monolithic Integrated Circuits, generic specification".

The MATRA MHS Quality Manual, which is available upon request, describes the total functions and policies applied by the organisation to ensure product reliability and quality. Every customer is encouraged to visit the MHS facilities and survey the deployment of the quality function.

MHS maintains a quality system using the above defined documents as a reference. This system guarantees full compliance of delivered products with customer specifications.

Using the enclosed MHS standard test tables and test parameters will help customers in defining their own procurement requirements and save specification negotiation time.

### 3 - BUILT-IN QUALITY AND RELIABILITY

MATRA MHS quality management strives to ensure that the products shipped to the customers are of high quality level and commitment with customer's needs.

In order to achieve those requirements, MHS started early 1988 a Quality Improvement Process, which calls for continuous progress and commitment of every employee to Total Quality Management (TQM).

The reliability approach at MHS is based upon designing reliability rather than only finding screening for it.

This built-in reliability is achieved through drastic ground rules and procedures executed in a new product design.

Reliability engineering is involved from the concept review up to the final release to production, through tough participation to design and layout reviews.

Quality of design is finally proved by mandatory first runs evaluation. This internal qualification procedure aims to approve any new design, technology or assembly process implemented at MHS.

Both maximum rated and accelerated stress conditions are applied to the devices. From the related data results, necessary changes may be implemented to ensure a wider and safer margin between the maximum rated stress conditions and the devices' stress tolerance characteristics.

### 4 - PARTNERSHIP DEPLOYMENT

Quality and reliability maintenance and improvement are easier to achieve through a close and permanent collaboration between MHS and its customers.

Therefore MHS proposes for high volume and standard products a PPM agreement program, which aims to implement at both customer and MHS facilities systematic analyses and data exchange in order to improve quality (zero defect philosophy) continuously.

Such a process leads to the introduction of new approaches such as "SHIP TO LINE" and "JUST IN TIME".

### 5 - AGENCIES QUALIFICATION

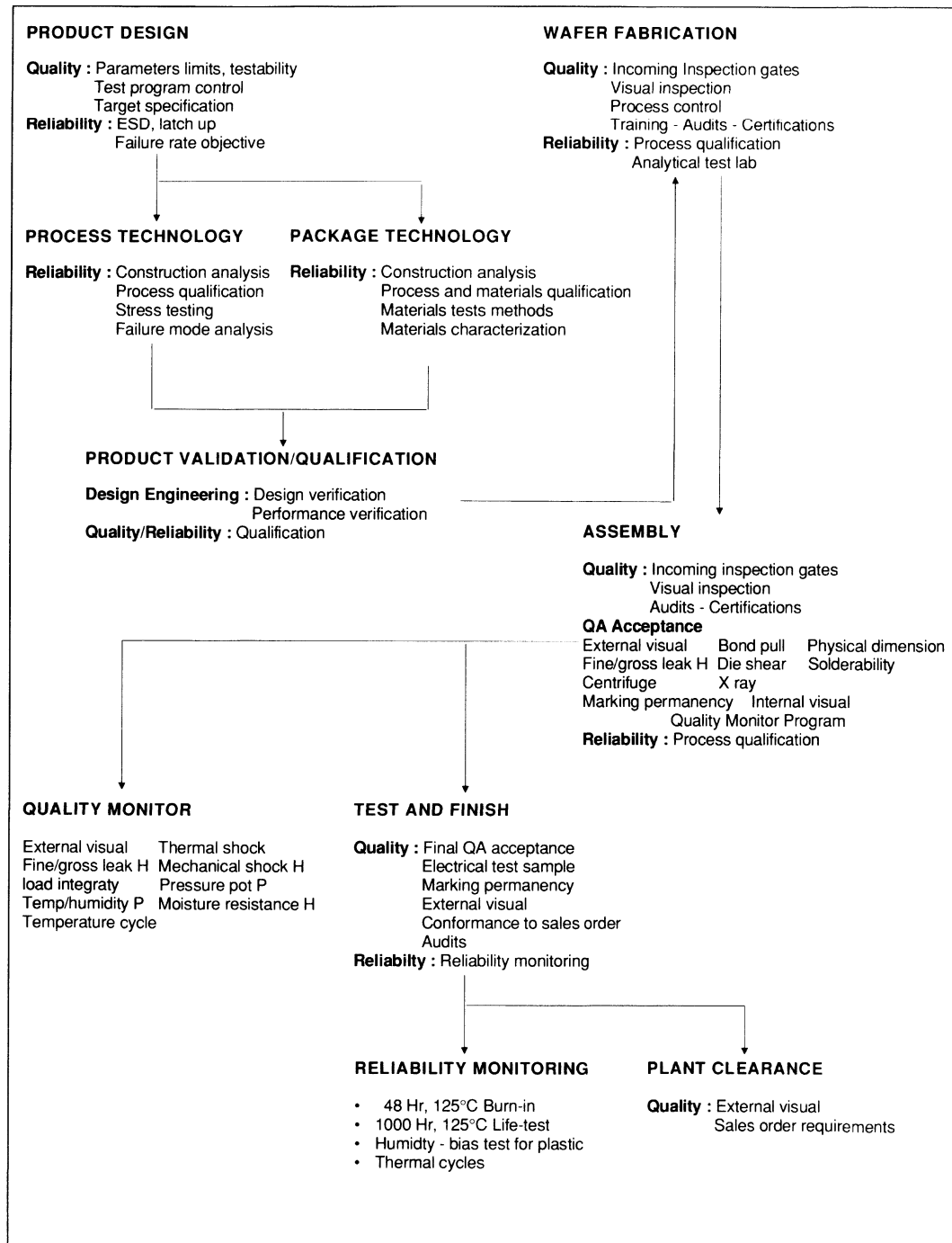
As part of specific qualification on military and space programs, MHS received several agreements from French and European agencies.

In 1986, MHS received the RAQ1 certification (RACQ1/AQAP1 regulation quality assurance Level 1) from the SIAR (Service de Surveillance Industrielle de l'Armement).

The RAQ1 certification covers every MHS internal quality procedure from the design (industry customer support on custom design) up to final quality control. The major MHS technologies and products are agreed by French Telecommunication Agency (CNET). These products are in qualified list (LNZ).

In 1989 MHS received the CECC Manufacturer Agreement and is now involved in products qualifications and capability approval for its 1  $\mu$ m technology.

## 6 – QUALITY PROCEDURE



### 6.1 - PROCESS CONTROLS

As shown by table 1 each integrated circuit is constructed by manufacturing processes which are under the surveillance of MHS Quality Control Department. The processes are monitored and controlled by use of statistical techniques\* and computerization in accordance with published specifications and procedures. MHS prepares and maintains suitable documentation

(such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in - process specification. The customer may verify, with the permission of and in the company of MHS's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by MHS is made available to the customer or its

## 2 - QUALITY CONTROL

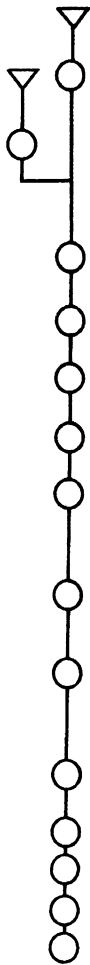
| FLOW                                                                               | PROCESS                            | TYPICAL ITEM                                                                                                                                                                      | FREQUENCY                 | REQUIREMENTS                   |
|------------------------------------------------------------------------------------|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------------------|
|  | Silicon wafers Incoming Inspection | <ul style="list-style-type: none"><li>• Resistivity</li><li>• Bow</li><li>• Flatness</li><li>• Taper</li><li>• Oxygen content</li><li>• Dimensions</li><li>• Appearance</li></ul> | Every lot                 | Sampling 1 %                   |
|                                                                                    | Masks Incoming Inspection          | <ul style="list-style-type: none"><li>• Defects</li><li>• Dimensions</li><li>• Registration</li><li>• Conformity</li></ul>                                                        | Every mask                |                                |
|                                                                                    | Oxidize                            | Thickness                                                                                                                                                                         | Every lot                 | 3 Wafers/lot<br>3 points/wafer |
|                                                                                    | Implant                            | Resistivity<br>C (V)                                                                                                                                                              | Every lot                 | 2 Wafers/lot<br>3 points/wafer |
|                                                                                    | Diffuse                            | Resistivity<br>Thickness                                                                                                                                                          | Every run                 | 4 Wafers/lot<br>3 points/wafer |
|                                                                                    | Silicon nitride                    | Thickness<br>Critical dimensions                                                                                                                                                  | Every lot                 | 2 Wafers/lot<br>5 points/wafer |
|                                                                                    | Gate oxide                         | Defect rates<br>VFBDVFB                                                                                                                                                           | Every run                 | 2 Wafers/lot<br>2 points/wafer |
|                                                                                    | Polysilicon                        | <ul style="list-style-type: none"><li>• Resistivity</li><li>• Thickness</li><li>• Critical dimensions</li><li>• Sem Inspection</li></ul>                                          | Every lot                 | 5 wafers/lot<br>5 points/wafer |
|                                                                                    | Metalization                       | <ul style="list-style-type: none"><li>• Resistivity</li><li>• Thickness</li><li>• Critical dimensions</li><li>• Sem Inspection</li></ul>                                          | Every run<br>• Periodical | 2 Wafers/run                   |
|                                                                                    | Passivation                        | <ul style="list-style-type: none"><li>• Doping</li><li>• CVD thickness</li><li>• Sem inspection</li></ul>                                                                         | Every run<br>• Periodical | 3 points/wafer                 |
|                                                                                    | Test site                          | Electrical charact.                                                                                                                                                               |                           |                                |
|                                                                                    | Blacklap                           | Thickness                                                                                                                                                                         | Every lot                 | 1 wafer/lot                    |
|                                                                                    | Gold evaporation                   | Tickness                                                                                                                                                                          | Every lot                 | 1 wafer/lot                    |
|                                                                                    | QC visual gate                     | Visual                                                                                                                                                                            | Every lot                 | 4 wafer/lot                    |
|                                                                                    | Wafer sort                         | Electrical charact.                                                                                                                                                               | 100 % chips               |                                |

Table 1 : Quality flow chart of wafer processing.

---

representative, that suitable documentation exists and is being applied. Information designated as proprietary by MHS is made available to the customer or its representative only with the written permission of MHS.

Process control is recognized as being vital to the concept of "built-in" quality. The process control program includes a scanning electron microscope (SEM) monitor program. The SEM analysis is defined in a Quality & Reliability Assurance document.

## **6.2 - CONTROL OF PROCUREMENT SOURCES**

### **– MHS/SUPPLIER CONVENTION**

Prior to use in production, MHS verifies the capability of the supplier QA, manufacturing engineering and services to deliver material conform to specification and kept under control evolution until Formal agreement is established between the two partners.

### **– RECEIVING INSPECTION**

Purchased supplies are subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration is given to the controls exercised by the procurement source and evidence of sustained quality conformance.

– MHS initiates corrective with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

## **6.3 INSPECTION RECORDS**

M.H.S. maintains a reliability data and records library. This library has on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and any other pertinent data generated on devices manufactured to this specification.

Reliability reports per product/package are available.

## **6.4 - CHANGE NOTIFICATION**

Unless otherwise specified, orders are placed following design, process and material in use or qualified at MHS at the moment ; Further major changes will be notified 3 month before the delivery of the first lot incorporating the change and submitted for approval to the customer's qualifying activity. Customer's procurement specification shall define the range of major change.

## **6.5 - CERTIFICATE OF CONFORMITY**

MHS includes a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate indicates that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate bears the name and signature of MHS Quality Control representative, the date of acceptance or signing, and any pertinent note as applicable.

## **6.6 - RELIABILITY PERFORMANCE**

Key figures in terms of reliability are that any product should reach the level of :

– 1000 ppm Early failure Rate (48 h, 125°C Dynamic Burn-in)

and

– 100 fits Long Failure Rate ( $\lambda$ , lambda).

This applies both for initial qualification or reliability data base are available upon request.

## **7. PRODUCT FLOWS**

MHS offers a broad range of screening flows starting from commercial up to space flows ! Methods associated with each step is either an MHS procedure or the standard procedure (883C, ...) depending on the flow reference. Details regarding Quality Conformity Inspection or any specific procedure could be available upon request.



| FLOW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | PROCESS MATERIALS                         | INSPECTION              | METHOD                        | FREQUENCY                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------------|-------------------------------|------------------------------|
| <pre> graph TD     S1[ ] --&gt; S2(( ))     S2 --&gt; S3[ ]     S3 --&gt; S4(( ))     S4 --&gt; S5[ ]     S5 --&gt; S6(( ))     S6 --&gt; S7[ ]     S7 --&gt; S8(( ))     S8 --&gt; S9[ ]     S9 --&gt; S10(( ))     S10 --&gt; S11[ ]     S11 --&gt; S12(( ))     S12 --&gt; S13[ ]     S13 --&gt; S14(( ))     S14 --&gt; S15[ ]     S15 --&gt; S16(( ))     S16 --&gt; S17[ ]     S17 --&gt; S18(( ))     S18 --&gt; S19[ ]     S19 --&gt; S20(( ))     S20 --&gt; S21(( ))           </pre> | Scribing                                  | Visual                  | 2010 Cond B                   | L3 : 100 %<br>L7 : AQL 2.5 % |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | QC inspection                             | Visual                  | 2010 Cond B                   | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Lead Frame, base<br>(incoming inspection) |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Frame and base<br>cleaning                |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Die Bonding                               |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | QC Inspection                             | Appearance              |                               | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Wire<br>(incoming inspection)             |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Wire Bonding                              | Bond sirength           | 2011                          | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Praseal inspection                        | Visual                  |                               | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | QC Inspection                             | Visual                  |                               | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Prestabilization<br>sealing               | Appearance              |                               | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Stabilisation bake                        |                         | L3 : method 1008<br>24H 150°C | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Temperature Cycling                       |                         | 1010<br>Condition C           | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Centrifuge                                |                         | 2001<br>Condition E           | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Plating                                   |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Plating inspection                        | Appearance<br>thickness |                               | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Fine leak                                 |                         | 1014<br>Condition A or B      | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Gross leak                                |                         | 1014<br>Condition C           | 100 %                        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Lead cut                                  |                         |                               |                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Marking                                   | Permanency              | 2015                          | Every lot                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | QA final inspection                       |                         | LTPD 7 Acc on 0               |                              |

**Table 2 :** QC flow charts of assembly process (1).  
 CERAMIC TYPE : L7 commercial and industrial  
 L3 military

| FAMILY / TEMP.<br>RANGE                    | COMMERCIAL<br>0°C/+70°C |                       | INDUSTRIAL<br>-40°C/-85°C |                       | AUTOMOTIVE<br>-40°C/+125°C |
|--------------------------------------------|-------------------------|-----------------------|---------------------------|-----------------------|----------------------------|
|                                            |                         |                       |                           |                       |                            |
| Memory &<br>Asic<br>SUFFIX                 | -5                      | -Q                    | -9                        | -L                    | CUST. CODE                 |
| Micro's<br>PREFIX                          | _x----                  | Qx----                | Ix----                    | Lx----                | Ax----                     |
| QA Wafer Visual<br>Insp.                   | Monitoring              | Monitoring            | Monitoring                | Monitoring            | Monitoring                 |
| Electrical PROBE                           | 100 %                   | 100 %                 | 100 %                     | 100 %                 | 100 %                      |
| ASSEMBLY                                   | L4/L7                   | L4/L7                 | L4/L7                     | L4/L7                 | L4/L7                      |
| Marking                                    | Test<br>Date-Code       | Test<br>Date-Code     | Test<br>Date-Code         | Test<br>Date-Code     | Test<br>Date-Code          |
| Pre Burn-In Test                           | -                       | OPTIONAL              | -                         | OPTIONAL              | -                          |
| DYNAMIC BURN-IN<br>(Minimum<br>Conditions) | -                       | 100 %<br>24 h / 140°C | -                         | 100 %<br>24 h / 140°C | -                          |
| Final Room Temps.                          | OPTIONAL                | OPTIONAL              | OPTIONAL                  | OPTIONAL              | OPTIONAL                   |
| Electrical High<br>Temps.                  | 100 %                   | 100 %                 | 100 %                     | 100 %                 | 100 %                      |
| Test Low Temp.                             | OPTIONAL                | OPTIONAL              | OPTIONAL                  | OPTIONAL              | OPTIONAL                   |
| P.D.A                                      | -                       | 5 %                   | -                         | 5 %                   | -                          |
| QA Electrical Gate<br>AQL=.1%              | YES                     | YES                   | YES                       | YES                   | YES                        |
| Gross & Fine Leaks                         | -                       | -                     | -                         | -                     | -                          |
| RX Inspection                              | -                       | -                     | -                         | -                     | -                          |
| External Visual                            | 100 %                   | 100 %                 | 100 %                     | 100 %                 | 100 %                      |
| Electrical<br>Conformance                  | Monitoring              | Monitoring            | Monitoring                | Monitoring            | Monitoring                 |
| Mechanical<br>Conformance                  | Monitoring              | Monitoring            | Monitoring                | Monitoring            | Monitoring                 |
| Reliability<br>Conformance                 | Monitoring              | Monitoring            | Monitoring                | Monitoring            | Monitoring                 |
| C.S.I                                      | On REQUEST              | On REQUEST            | On REQUEST                | On REQUEST            | On REQUEST                 |
| Database and CoC                           | On REQUEST              | On REQUEST            | On REQUEST                | On REQUEST            | On REQUEST                 |
| Shipping Inspection                        | All Delivery            | All Delivery          | All Delivery              | All Delivery          | All Delivery               |

| FAMILY / TEMP.<br>RANGE                    | MILITARY<br>55°C/+125°C   |                                        |                                      |                                      | SPACE<br>-55°C/-125°C |                                        |
|--------------------------------------------|---------------------------|----------------------------------------|--------------------------------------|--------------------------------------|-----------------------|----------------------------------------|
|                                            | MIL - STD 883C CECC 90000 |                                        |                                      |                                      | ESA:SCC 9000          |                                        |
| Memory &<br>Asic<br>SUFFIX                 | -2                        | -8                                     | -MB                                  | -CB                                  | -SCx                  | -SBx                                   |
| Micro's<br>PREFIX                          | Mx----                    | Mx---- /B                              | Mx---- -MB                           | Mx---- -CB                           | Mx---- -SCx           | Mx---- -SBx                            |
| QA Wafer Visual<br>Insp.                   | Monitoring                | Monitoring                             | Monitoring                           | Monitoring                           | S.E.M.                | S.E.M.                                 |
| Electrical PROBE                           | 100 %                     | 100 %                                  | 100 %                                | 100 %                                | 100 %                 | 100 %                                  |
| ASSEMBLY                                   | L3                        | L3                                     | L3                                   | L3                                   | L2                    | L2                                     |
| Marking                                    | Test<br>Date-Code         | Test<br>Date-Code                      | Sealing<br>Date-Code                 | Sealing<br>Date-Code                 | Sealing<br>Date-Code  | Sealing<br>Date-Code<br>&Serialization |
| Pre Burn-In Test                           | -                         | OPTIONAL                               | 100 %                                | 100 %                                | 100 %                 | 100 % +<br>RECORDS                     |
| DYNAMIC BURN-IN<br>(Minimum<br>Conditions) | -                         | 100 %<br>168h / 125°C<br>or equivalent | 100 %<br>168h/125°C<br>or equivalent | 100 %<br>168h/125°C<br>or equivalent | 100 %<br>168h / 125°C | 100 %<br>240h / 125°C                  |
| Final Room Temps.                          | OPTIONAL                  | OPTIONAL                               | 100 %                                | 100 %                                | 100 %                 | 100 % +<br>RECORDS                     |
| Electrical High<br>Temps.                  | 100 %                     | 100 %                                  | 100 %                                | 100 %                                | 100 %                 | 100 % +<br>RECORDS                     |
| Test Low Temp.                             | 100 %                     | 100 %                                  | 100 %                                | 100 %                                | 100 %                 | 100 % +<br>RECORDS                     |
| P.D.A                                      | -                         | 5 %                                    | 5 %                                  | 10 %                                 | 10 %                  | 10 % + DRIFT                           |
| QA Electrical Gate<br>AQL=.1%              | YES                       | YES                                    | N/A                                  | N/A                                  | N/A                   | N/A                                    |
| Gross & Fine Leaks                         | -                         | -                                      | -                                    | -                                    | 100 %                 | 100 %                                  |
| RX Inspection                              | -                         | -                                      | -                                    | -                                    | -                     | 100 %                                  |
| External Visual                            | 100 %                     | 100 %                                  | 100 %                                | 100 %                                | 100 %                 | 100 %                                  |
| Electrical<br>Conformance                  | Monitoring                | Monitoring                             | Group A                              | Group A/B                            | LAT3                  | LAT3                                   |
| Mechanical<br>Conformance                  | Monitoring                | Monitoring                             | Group B                              | Group A/B                            | LAT3                  | LAT3                                   |
| Reliability<br>Conformance                 | Monitoring                | Monitoring                             | Group C/D                            | Group C                              | LAT2 + LAT1           | LAT2 + LAT1                            |
| C.S.I                                      | On<br>REQUEST             | On<br>REQUEST                          | On<br>REQUEST                        | On<br>REQUEST                        | All Delivery          | All Delivery                           |
| Database and CoC                           | On<br>REQUEST             | On<br>REQUEST                          | On<br>REQUEST                        | On<br>REQUEST                        | All Delivery          | All Delivery                           |
| Shipping Inspection                        | All Delivery              | All Delivery                           | All Delivery                         | All Delivery                         | All Delivery          | All Delivery                           |



# MHS LOCATIONS







## M.H.S. LOCATIONS

---

### MHS ELECTRONIC CENTER

---

La Chantrerie/Route de Gachet  
CP 3008  
44087 Nantes Cedex 03/France  
Tel. : (33) 40303030 - Twx : 711930 - Fax : (33) 40300216

---

### SALES OFFICES

---

#### FRANCE

"Les Quadrants"  
3, avenue du Centre  
BP 309  
78054 St-Quentin-Yvelines Cedex  
Tel. : (33) 1-30607000  
Twx : 697317  
Fax : (33) 1-30640693

#### GERMANY

Erfurterstrasse 29  
D-8057 Eching  
Tel. : (49) 89-31900550  
Twx : 524126  
Fax : (49) 89-31900555

#### ITALY

Via Vigliani 13  
I-20148 Milano  
Tel. : (39) 2-4984586  
Twx : 334595  
Fax : (39) 2-4818660

#### SCANDINAVIA

MD SEMICONDUCTOR AB  
Kavallerivagen 24  
Box 2042 - 17202 Sundbyberg  
Sweden  
Tel. : (46) 8-733.00.90  
Fax : (46) 8-733.05.58

#### UNITED KINGDOM

Easthampstead Road  
Bracknell  
Berkshire RG12 1LX  
Tel. : (44) 344-485757  
Twx : 849392  
Fax : (44) 344-427371

#### FAR EAST

MATRA DESIGN SEMICONDUCTOR  
ASIA  
10/FI., 111 Leighton Road  
Causeway Bay  
Hong Kong  
Tel. : (852) 8901899  
Fax : (852) 8907270  
Twx : 70483

#### USA

2895 Northwestern Parkway  
Santa Clara, CA 95051  
Tel. : (1) 408/748-9362  
Twx : 299656  
Fax : (1) 408/748-0439

---

### EUROPEAN DISTRIBUTORS

---

#### AUSTRIA

TRANSISTOR  
VERTRIEBSGESELLSCHAFT  
mbH CO-KG  
Auhofstrasse 41A  
A-1130 Wien  
Tel. : (43) 222-829401  
Twx : 133738  
Fax : (43) 222-826440

#### BELGIUM

MICROTRON NV S.A.  
Generaal Dewitelaan 7  
2800 Mechelen  
Tel. : (32) 15-212223  
Twx : 22606  
Fax : (32) 15-210069

#### DENMARK

DITZ SCHWEITZER A.S.  
Vallensbakvej 41  
Post Box 5  
DK-2605 Brøndby  
Tel. : (45) 42-453044  
Twx : 33257  
Fax : (45) 42-459206

#### FINLAND

YLEISELEKTRONIKKA OY  
P.O. Box 73  
SF-02201 Espoo  
Tel. : (358) 0-4521255  
Twx : 123212  
Fax : (358) 0-428932

#### FRANCE

A2M  
6, av. Charles-de-Gaulle  
78150 Le Chesnay  
Tel. : (33) 1-39549113  
Twx : 698376  
Fax : (33) 1-39543061

#### ALMEX

48, rue de l'Aubépine  
92160 Antony  
Tel. : (33) 1-46662112  
Twx : 250067  
Fax : (33) 1-46666028

## LOCATIONS

### EUROPEAN DISTRIBUTORS (continued)

#### FRANCE (continued)

RTF  
81, rue Pierre Semard  
92320 Chatillon  
Tel. : (33) 1-49652700  
Twx : 632247  
Fax : (33) 1-49652738

ERICSSON COMPOSANTS  
1, Parc Club Ariane  
Rue Hélène Boucher  
78284 Guyancourt  
Tel. : (33) 1-30640900  
Twx : 697347  
Fax : (33) 1-30641146

#### GERMANY

ALFRED NEYE ENATECHNIK GMBH  
Schillerstrasse 14  
D-2085 Quickborn  
Tel. : (49) 4106-6121  
Twx : 213590  
Fax : (49) 4106-612268

JERMYN GMBH  
Im Dachsstück 9  
D-6250 Limburg  
Tel. : (49) 6431-5080  
Twx : 4152570  
Fax : (49) 6431-508289

SPOERLE ELECTRONICS GMBH  
Max-Planck-Strasse 1-3  
Postfach 102140  
D-6072 Dreieich 1  
Tel. : (49) 6103-3040  
Twx : 417972  
Fax : (49) 6103-304201

#### ITALY

CAMEL ELETTRONICA  
Via Tiziano 18  
I-20145 Milano  
Tel. : (39) 2-4981481  
Twx : 325237  
Fax : (39) 2-4818637

KONTRON SPA  
Via Fantoli 16/15  
I-20138 Milano  
Tel. : (39) 2-50721  
Twx : 312288  
Fax : (39) 2-5060918

#### ITALY (continued)

LASI ELETTRONICA SPA  
Viale Fulvio Testi 126  
I-20092 Cinisello Balsamo  
Tel. : (39) 2-2440012  
Twx : 352040  
Fax : (39) 2-2487717

#### NETHERLANDS

NIJCKER  
Drentestraat 7  
1083 HK AMSTERDAM  
Postbus 7920  
1008 AC AMSTERDAM  
Tel. : (31) 20-5495-969  
Twx : 11625 NESCO  
Fax : (31) 20-423-948

#### NORWAY

TAHONIC A/S  
P.O. Box 140/KALBAKKEN  
N-0902 OSLO 9  
Tel. : (47) 2-161610  
Twx : 77397  
Fax : (47) 2-257317

#### SPAIN

SELCO SA  
Paseo de la Habana 190  
28036 Madrid  
Tel. : (34) 1-4054213  
Twx : 45458  
Fax : (34) 1-2592284

#### SWEDEN

EGEVO ELEKTRONIK AB  
Box 8100  
S-16308 Spånga  
Tel. : (46) 8.795 96 50  
Fax : (46) 8.795 78 83

#### SWITZERLAND

ELECTRONITEL  
Chemin du Grand Clos 1  
B.P. 93  
CH-1752 VILLARS-SUR-GLANE  
Tel. : (37) 41.00.60  
Fax : (37) 41.00.70

#### UNITED KINGDOM AND IRELAND

MACRO MARKETING LTD  
Burnham Lane - SLOUGH  
Berkshire SL1 6LN.  
Tel. : (44) 6286 4422  
Twx : 8479 45  
Fax : (44) 62 86 66 89

MTL MICROTECHNOLOGY LIMITED  
(Die Distributor)  
Test House - Mill Lane - ALTON  
Hampshire. GU34 2QG.  
Tel. : (44) 420 88022  
Tlx : 858456  
Fax : (44) 420 87 25

POLAR ELECTRONICS LIMITED  
Cherrycourt Way  
Leighton Buzzard  
Bedfordshire. LU7 8YY.  
Tel. : (44) 525 377093  
Tlx : 825238  
Fax : (44) 525 3783

R R ELECTRONICS LIMITED  
St. Martin's Way Industrial Estate  
Cambridge Road - BEDFORD  
Bedfordshire. MK42 0LF  
Tel. : (44) 234 47188  
Tlx : 826251  
Fax : (44) 234 21 063

THAME COMPONENTS LIMITED  
Thame Park Road - THAME  
Oxfordshire OX9 3XD.  
Tel. : (44) 84426 1188  
Twx : 837917  
Fax : (44) 84 42 61 68

### FAR EAST REPRESENTATIVES AND DISTRIBUTORS

#### INDIA

SPARTEX SYSTEMS & SERVICES  
Pvt Ltd.,  
N° 68, Michael Palyam,  
Near Deccan Studio,  
C.V. RAMAN NAGAR POST,  
BANGALORE - 560 093,  
INDIA  
Tel. : 564211, 568772  
Tlx : 0845 - 2190 MLHR IN

#### JAPAN

CHRONIX INCORPORATED  
Maruyama Bld 4F  
7-9-7, Nishishinjuku  
Shinjuku-ku, Tokyo, 160  
Tel. : (81) 3-371-5711  
Twx : 26244  
Fax : (81) 3-371-5738

#### KOREA

DEVICE TECHNOLOGY Co.  
Rm 3021, Sun In Sang Ka-21 Dong  
16-1, Han Kang Ho-2Ka  
Yong San-Ku, Seoul  
Tel. : (82) 2-71 64273  
Fax : (82) 2-71 51170



## LOCATIONS

### FAR EAST REPRESENTATIVES AND DISTRIBUTORS (continued)

#### KOREA (continued)

SEOLEXON TECHNOLOGY Co.  
Rm 501, Keonsul Office Bdg  
200-10, Docksan-Dong  
Guro-Ku, Seoul  
Tel.: (82) 2-8587167  
Fax.: (82) 2-8587169

#### HONG KONG

PROTECH COMPONENTS Ltd.  
Unit 2, 3/FI, Wah Shing Centre  
11 Shing Yip Street  
Kwun Tong, Kowloon  
Tel.: (852) 793 08 82  
Fax.: (852) 793 08 11

WILLAS Co. Ltd.  
8/FI, Wing Tai Centre  
12 Hing Yip Street  
Kwun Tong, Kowloon  
Tel.: (852) 34 14 281  
Fax.: (852) 34 31 229  
Twx.: 39 315

#### SINGAPORE

SCAN TECHNOLOGY (S)  
Pte Ltd.  
50 Kallang Bahru # 04-01/03  
Kallang Basin Industrial Estate  
Singapore 1233  
Tel.: (65) 2942112  
Fax.: (65) 2961685  
Twx.: 24983 STECH

SOUTH WEST ELECTRONICS  
Pte Ltd.  
23, Genting Road  
# 06-02 Ryosan Complex  
Singapore 1334  
Tel.: (65) 7431813  
Fax.: (65) 7471128

WESTECH ELECTRONICS Pte Ltd.  
12 Loron Bakar Batu 05-072  
Kolam Ayer Industrial Park  
Singapore 1334  
Tel.: (65) 7436355  
Fax.: (65) 7461396  
Twx.: 55070

#### TAIWAN

CELLTRIX Co. Ltd.  
3F-2, N. 151 Sec 4, Shin-Yi Rd  
Taipeh, R.O.C  
Tel.: (886) 2-7011497  
Fax.: (886) 2-7077205

UNION TECHNOLOGY Co.  
8/FI, N. 270 Sec 3, Nanking E. Rd  
Taipeh  
Tel.: (886) 2-7753666  
Fax.: (886) 2-7317666  
Twx.: 20261 MEET

WORLD PEACE INDUSTRIAL Co. Ltd.  
5/FI, 309, ung Chiang Rd  
Taipeh  
Tel.: (886) 2-7883252  
Fax.: (886) 2-7883255

#### AUSTRALIA

CONSULAUST INTERNATIONAL Ltd.  
1, Norfolk Road, Surrey Hills  
Po Box 357, Camberwell  
Victoria 3124  
Tel.: (61) 3-8362566  
Fax.: (61) 3-8301764  
Twx.: AA37455 CONAUS

### US REPRESENTATIVES

#### ANCHOR ENGR.

11 WALKUP DR.  
WESTBORO  
MASSACHUSETTS 01581-1018  
Tel.: 508-898-2724  
Fax.: 508-870-0573

#### ARBOTEK

10404 W. JOPPA RD.  
TOWSON  
MARYLAND 21204  
Tel.: 301-825-0775  
Fax.: 301-337-2781

2201 ANGUS RD., SUITE 14  
CHARLOTTESVILLE  
VIRGINIA 22901  
Tel.: 804-971-5736

#### C.C. ELECTRO

5335 N. TACOMA AVE., SUITE #1  
INDIANAPOLIS  
INDIANA 48220  
Tel.: 317-255-1508  
Fax.: 317-266-6875

5635 FORDHAM CIRCLE #203  
CANTON  
MICHIGAN 48187  
Tel.: 313-981-9298

9735 RAVENNA RD.  
TWINSBURG  
OHIO 44087  
Tel.: 216-425-8338  
Fax.: 216-425-2147

#### CAHILL, SCHMITZ & HOWE

4905 Lakeside Drive  
N.E. SUITE 100  
CEDAR RAPIDS  
IOWA 52402  
Tel.: 319-377-8219  
Fax.: 319-377-0958

#### E.M.A.

6695 PEACHTREE IND. BLVD.,  
SUITE 101  
ATLANTA  
GEORGIA 30360  
Tel.: 404-448-1215  
Fax.: 404-446-9363

210 W. STONE AVE.  
GREENVILLE  
S. CAROLINA 29609  
Tel.: 803-233-4637  
Fax.: 803-242-3089

7501 South Memorial Parkway, #202  
HUNTSVILLE  
ALABAMA 35802  
Tel.: 205-880-8050  
Fax.: 205-880-8054

8512 SIX FORKS RD., SUITE 601 A  
RALEIGH  
N. CAROLINA 27615  
Tel.: 919-847-8800  
Fax.: 919-848-1787

#### ELECTEC

3211 SCOTT BLVD., SUITE 101  
SANTA CLARA  
CALIFORNIA 95054  
Tel.: 408-496-0706  
Fax.: 408-727-9817

8465 ROYAL OAKS DRIVE  
GRANITE BAY  
CALIFORNIA 95661  
Tel.: 916-797-0414  
Fax.: 916-456-6001

#### GEORGE RUSSEL & ASSOC.

8030 CEDAR AVE. SOUTH,  
SUITE 114  
MINNEAPOLIS  
MINNESOTA 55420  
Tel.: 612-854-1168

#### LANDA & ASSOC.

1518 COTNER AVE.  
LOS ANGELES  
CALIFORNIA 90025  
Tel.: 213-879-0770  
Fax.: 213-478-0190

1616 E. 4TH ST.  
SANTA ANA  
CALIFORNIA 92701  
Tel.: 714-543-7805  
Fax.: 714-543-1380

662 NARDO AVE.  
SOLANA BEACH  
CALIFORNIA 92075

---

## LOCATIONS

---

### US REPRESENTATIVES (continued)

#### M.E.C.

700 W. HILLSBORO BLVD., BLDG. 4,  
#204  
DEERFIELD BEACH  
FLORIDA 33441  
Tel. : 305-426-8944  
Fax : 305-426-8799

830 N. ATLANTIC BLVD., SUITE B401  
COCOA BEACH  
FLORIDA 32931  
Tel. : 407-799-0520  
Fax : 407-799-0923

511 CARRIAGE ROAD  
INDIAN HARBOUR BEACH  
FLORIDA 32937  
Tel. : 407-332-7158  
Fax : 407-830-5436

1001 45TH AVE., NE  
ST. PETERSBURG  
FLORIDA 33703  
Tel. : 813-522-3433  
Fax : 813-522-3933

#### N.E. COMPONENTS

155 GRANDVIEW LANE  
MAHWAH  
NEW JERSEY 07430  
Tel. : 201-825-0233  
Fax : 201-934-1310

22 LAWRENCE AVE.  
SMITHTOWN  
NEW YORK 11787  
Tel. : 516-724-3485

#### PHOENIX SALES

257 MAIN ST.  
TORRINGTON  
CONNECTICUT 06790  
Tel. : 203-496-7709  
Fax : 203-496-0912

#### SW MARKETING ASSOC.

10940 ALDER CIRCLE  
DALLAS  
TEXAS 75238  
Tel. : 214-341-8631  
Fax : 214-340-5870

13006 KELLIES FARMLANE  
AUSTIN  
TEXAS 78727  
Tel. : 512-255-8010

400 FM 1960 WEST, SUITE 100-15  
HOUSTON  
TEXAS 77090  
Tel. : 713-537-8166  
Fax : 713-537-9738

6713 E. 54TH ST.  
TULSA  
OKLAHOMA 74145  
Tel. : 918-663-7536

#### SYNERGISTIC SALES

501 MITCHELL ROAD  
GLENDALE HEIGHTS  
ILLINOIS 60139  
Tel. : 312-858-8686  
Fax : 312-790-9799

#### TECH SALES ASSOC.

EXEC. MEWS, RJ-52, 2300  
COMPUTER AVE.  
WILLOW GROVE  
PENNSYLVANIA 19090  
Tel. : 215-784-0170  
Fax : 215-784-9201

#### THORSON CO. n.w.

12340 N.E. 8TH ST., SUITE 201  
BELLEVUE  
WASHINGTON 98005  
Tel. : 206-455-9180  
Fax : 206-455-9185

8700 S.W. 105TH AVE.  
BEAVERTON  
OREGON 97005  
Tel. : 503-644-5900  
fax : 503-644-5919

#### TRUE NORTH TECH. LTD.

100 WESTMORE DR., SUITE 12E  
REXDALE, ONTARIO  
CANADA M0V 5C3  
Tel. : 416-744-2233  
Fax : 416-744-3376

1883 LONGMAN CRESCENT  
GLOUCESTER, ONTARIO  
CANADA K1C 5G7  
Tel. : 613 824-8957  
Fax : 614-745-0315

#### WEST, INC.

1740 PLATTE SR. #200  
DENVER  
COLORADO 80202  
Tel. : 303-477-1134

460 EAST 100 SOUTH  
CENTERVILLE  
UTAH 84014-5087  
Tel. : 801-292-8787  
Fax : 801-298-0788

---

### US DISTRIBUTORS

#### ADDED VALUE ELECTRONIC DISTRIBUTION, INC.

1512 PARKWAY LOOP, UNIT G  
TUSTIN, CA 92680  
Tel. : (714) 259-8258  
Fax : (714) 259-0828

31194 LA BAYA DRIVE, SUITE 100  
WESTLAKE VILLAGE, CA 91362  
Tel. : (805) 643-2101  
(818) 889-2861  
Fax : (818) 889-2472

7741 E. GRAY ROAD, SUITE 9  
SCOTTSDALE, AZ 85260  
Tel. : (602) 951-9788  
Fax : (602) 951-4182

A.V.E.D. - ROCKY MOUNTAIN, INC.  
1836 PARKWAY BLVD.  
WEST VALLEY CITY, UT 84119  
Tel. : (801) 975-9500  
Fax : (801) 977-0245

A.V.E.D. - ROCKY MOUNTAIN, INC.  
4090 YOUNGFIELD ST.  
WHEAT RIDGE, CO 80033  
Tel. : (303) 422-1701  
Fax : (303) 422-2529

A.V.E.D. - SOUTHWEST INC.  
4470 SPRING VALLEY ROAD  
DALLAS, TX 75244  
Tel. : (214) 404-1144  
Fax : (214) 233-2614

#### ALL AMERICAN SEMICONDUCTOR CORP.

2360 QUME DRIVE, SUITE C  
SAN JOSE, CA 95131  
Tel. : (408) 943-1200  
Fax : (408) 943-1393

16251 N.W. 54TH AVENUE  
MIAMI, FL 33014  
Tel. : (305) 621-8282  
(800) 228-7459  
Fax : (305) 620-7831

369 VAN NESS WAY, SUITE 701  
TORRANCE, CA 90501  
Tel. : (213) 320-0240  
(800) 669-8300  
Fax : (213) 320-7207

---

## LOCATIONS

---

### US DISTRIBUTORS (continued)

---

#### ALL AMERICAN SEMICONDUCTOR CORP. (continued)

5009 HIATUS ROAD  
SUNRISE, FL

107 AUDUBON ROAD, SUITE 104  
WAFEFIELD, MA 01880  
Tel.: (617) 246-2300

1819 FIRMAN DRIVE, #127  
RICHARDSON, TX 75081  
Tel.: (214) 231-5300  
Fax: (214) 437-0353

14636 ROTHGEB DRIVE  
ROCHVILLE, MD 20850  
Tel.: (301) 251-1205  
Fax: (301) 251-8574

711-2 KOEHLER AVENUE  
RONKONKOMA, NY 11779  
Tel.: (516) 981-3935  
(800) 874-2830  
Fax: (516) 931-3947

11409 VALLEY VIEW ROAD  
EDEN PRAIRIE, MN 55344  
Tel.: (800) 342-7364  
Fax: (612) 944-9803

#### BELL INDUSTRIES

1031 PUTNAM DRIVE, SUITE A  
HUNTSVILLE, AL 35816  
Tel.: (205) 837-1074  
Fax: (205) 830-5598

306 E. ALONDRA BLVD.  
GARDENA, CA 90247  
Tel.: (213) 515-1800  
Fax: (213) 777-3111 X306

11812 SAN VINCENTE BLVD., #300  
LOS ANGELES, CA 90049  
Tel.: (213) 826-6778  
Fax: (213) 258-6932

1705 W. 4TH ST.  
TEMPE, AZ 85281  
Tel.: (602) 966-7800  
Fax: (602) 967-6584

11095 KNOTT AVE., SUITE E  
CYPRESS, CA 90630  
Tel.: (714) 891-4570

4311 ANTHONY COURT, #100  
ROCKLIN, CA 96677  
Tel.: (916) 652-0414  
Fax: (916) 652-0403

7450 RONSON ROAD  
SAN DIEGO, CA 92111  
Tel.: (619) 268-1277  
Fax: (619) 268-3733

638 SO. MILITARY TRAIL  
DEERFIELD BEACH, FL 33442  
Tel.: (305) 421-1997  
Fax: (305) 421-5705

3020 A BUSINESS PARK DRIVE  
NORCROSS, GA 30071  
Tel.: (404) 662-0923  
Fax: (404) 449-6901

130 KILLARNEY  
URBANA, IL 61801  
Tel.: (217) 328-1077  
Fax: (217) 328-1148

5230 WEST 79TH ST.  
INDIANAPOLIS, IN 46268  
Tel.: (317) 875-8200  
Fax: (317) 875-8219

1161 NO. FAIROAKS AVE.  
SUNNYVALE, CA 94089  
Tel.: (408) 734-8570  
Fax: (408) 734-8875

12421 W. 49TH AVENUE  
WHEATH RIDGE, CO 80033  
Tel.: (303) 424-1985  
fax: (303) 424-0932

10810 72ND ST. NORTH, SUITE 201  
LARGO, FL 33541  
Tel.: (813) 541-4434  
Fax: (813) 546-6418

515 BUSSE AVENUE, UNIT D-I  
ELK GROVE VILLAGE, IL 60007  
Tel.: (312) 640-1910  
Fax: (312) 640-0474

3433 E. WASHINGTON BLVD.  
FT. WAYNE, IN 46803  
Tel.: (219) 423-3422  
Fax: (219) 424-2433

1221 PARK PLACE, N.E.  
CEDAR RAPIDS, IA 52402  
Tel.: (319) 395-0730  
Fax: (319) 395-9761

100 BURTT ROAD? #106  
ANDOVER, MA 01810  
Tel.: (508) 474-8880  
Fax: (508) 474-8902

814 PHOENIX DRIVE  
ANN ARBOR, MI 48404  
Tel.: (313) 971-9093  
Fax: (313) 971-9178

444 WINDSOR PARK DRIVE  
DAYTON, OH 45459  
Tel.: (513) 435-8660  
Fax: (513) 435-6765

6024 SOUTHWEST JEAN ROAD  
LAKE OSWEGO, OR 97034  
Tel.: (503) 241-4115  
Fax: (503) 635-6500

6912 SOUTH 185 WEST, SUITE B  
MIDVALE, UT 84044  
Tel.: (801) 255-9611  
Fax: (801) 255-2477

W. 227N, 913 WESTMOUND DRIVE  
WAUKESHA, WI 53186  
Tel.: (414) 547-8879  
Fax: (414) 547-6547

6979 WASHINGTON AVE. SO.,  
SUITE 200  
EDINA, MN 55435  
Tel.: (612) 941-1493  
Fax: (612) 941-2964

11728 LINN, N.E.  
ALBUQUERQUE, NM 87123  
Tel.: (505) 292-2700  
Fax: (505) 275-2819

118 WESTPARK ROAD  
DAYTON, OH 45459  
Tel.: (513) 434-8231  
Fax: (513) 434-8103

1701 GREENVILLE, #306  
RICHARDSON, TX 75081  
Tel.: (214) 690-0466  
Fax: (214) 690-0822

8553 154TH AVE. N.E.  
REDMOND, WA 98052  
Tel.: (206) 885-9963  
Fax: (206) 867-5159

30101 AGOURA COURT, SUITE 118  
AGOURA HILLS, CA 91301  
Tel.: (818) 706-2608  
Fax: (818) 891-7695

## LOCATIONS

### US DISTRIBUTORS (continued)

#### CAM RPC ELECTRONICS

2975 BRIGHTON HENRIETTA  
TOWN LINE RD.  
ROCHESTER, NY 14623  
Tel. : (716) 427-9999  
Fax : (716) 427-7559

749 MINER ROAD  
CLEVELAND, OH 44143  
Tel. : (216) 461-4700  
Fax : (216) 461-4329

620 ALPHA DRIVE  
PITTSBURGH, PA 15238  
Tel. : (412) 963-6202  
Fax : (412) 963-6210

7973-B WASHINGTON WOOD DRIVE  
DAYTON, OH 45459  
Tel. : (513) 433-5551  
Fax : (513) 461-4329

#### FALCON ELECTRONICS INC.

5 HIGGINS DRIVE  
MILFORD, CT 06460  
Tel. : (203) 878-5272  
Fax : (203) 877-2010

CATON RESEARCH CENTER,  
SUITE Q  
1520 CATON CENTER DRIVE  
BALTIMORE, MD 21227  
Tel. : (301) 247-5800  
Fax : (301) 247-5893

1383 VETERAN'S MEMORIAL HWY.  
HAUPPAGE, NY 11788  
Tel. : (516) 724-0980  
(800) 528-0016  
Fax : (516) 724-0993

#### HAMMOND ELECTRONICS, INC.

4411-B EVANGEL CIRCLE N.W.  
HUNTSVILLE, AL 35816  
Tel. : (205) 830-4764  
Fax : (205) 830-4287

2923 PACIFIC AVE.  
GREENBORO, NC 27420  
Tel. : (919) 275-6391

5680 OAKBROOK PKWY., SUITE 160  
NORCROSS, GA 30093  
Tel. : (404) 449-1996  
(800) 241-5437  
Fax : (404) 424-9834

6600 N.W. 21ST AVE., 8AY D  
FT. LAUDERDALE, FL 33309  
Tel. : (305) 973-7103  
(FT LAUDERDALE)  
Fax : (305) 973-7601

1230 WEST CENTRAL BLVD.  
ORLANDO, FL 32802  
Tel. : (407) 841-1010 (ORLANDO)  
Fax : (407) 648-8584

#### NU HORIZONS ELECTRONICS CORP.

151 ANDOVER ST.  
DANVERS, MA 01923  
Tel. : (617) 777-8800  
Fax : (617) 777-8806

39 U.S. ROUTE 46  
PINE BROCK, NJ 07058  
Tel. : (201) 882-8300  
Fax : (201) 882-8398

100 BLUFF DRIVE  
EACH ROCHESTER, NY 1445  
Tel. : (716) 248-5980  
(203) 265-0162  
Fax : (716) 248-9132

6000 NEW HORIZONS BLVD.  
AMITYVILLE, NY 11701  
Tel. : (516) 226-6000  
Fax : (516) 226-6262

2002C GREENTREE EXECUTIVE  
CAMPUS  
MARLTON, NJ 08053  
Tel. : (609) 596-1833  
Fax : (609) 596-0612

#### SEMAD/DGW ELECTRONICS CORP.

85 SPY COURT  
MARKHAM, ONTARIO  
CANADA L3R 4Z4  
Tel. : (416) 475-3922  
Fax : (416) 475-4158

8563 GOVERNMENT ST.  
BURNABY, B.C.  
CANADA V3N 4S9  
Tel. : (604) 420-9889  
Fax : (604) 420-0124

6120 THIRD ST., SE UNIT #G  
CALGARY, ALBERTA  
CANADA T2H 1K4  
Tel. : (403) 252-5664  
Fax : (403) 255-0966

1827 WOODWARD DRIVE,  
SUITE 303  
OTTAWA, ONTARIO  
CANADA K2C 0R3  
Tel. : (613) 727-8325  
Fax : (613) 727-9489

243 PLACE FRONTENAC  
POINTE CLAIRE, PQ  
CANADA H9R 4Z7  
Tel. : (514) 694-0860  
Fax : (514) 694-0965

15

MATRA MHS products are sold by description only. MHS reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders.

Information contained in application notes is intended solely for general guidance ; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

Copyright © MHS 1989 - (All rights reserved) - Printed in France JOUVE Paris

Typesetting and lay-out using Desktop-Publishing means - AZIMUT - France - 21.75.01.75

